

Chapter 1

Introduction

The first integrated circuits date back to the 1950s. From that moment, humanity witnessed an impressive growth of the presence of electronics in everyday life. This growth is not going to stop, and will also involve innovative applications that, contrary to most product nowadays, will not be based on high computational power or ultra-fast mobile data communication.

Many of these new applications will indeed demand e.g. large-area, mechanical flexibility, fast prototyping, customization and ultra-low-cost production. Examples include surfaces allowing human-machine interaction (tactile, visual, etc.) and bringing internet connection even to very cheap objects (thus widening the concept of “internet of things” to everything around us).

New electronic technologies, devices, circuits and systems are being created to empower this future. A first glimpse at this emerging electronics is given in this chapter, and a deeper insight will be provided in this whole book.

1.1 Silicon and Plastic

In 1965, Moore reported in his famous paper [1] that the number of transistors on an integrated circuit between 1958 and 1965 doubled every two years. He predicted the same trend to continue for at least ten years after his paper but his prediction turned out to be pessimistic. As a matter of fact, the integrated circuit industry adopted the well-known law named after him as the roadmap for its research and development, therefore Moore’s trend has been followed till our days.

The exponential growth in the number of transistors per IC, fuelled by an impressive effort in device miniaturization and by outstanding achievements in the manufacturing processing, is tightly coupled to an exponential decrease of the unity cost of the transistor, which has enabled a pervasive presence of electronics in human lives. The downscaling of the feature size of silicon technologies does not allow only more integration, but also higher speed, reduced power-delay product, and improved reliability of the integrated circuits.

On the other hand, there are many applications of electronics that do not require high computational power, and cannot be addressed by standard IC technologies due to the high cost per area and to mechanical limitations. The typical example of such applications is a flat-screen display. Displays are intrinsically large-area. Their remarkable growth and irresistible commercial success are based on the development of a specific electronic technology, TFTs (Thin-Film Transistors) on glass, which aims at decreasing the cost per unit area (and not the cost per transistor, as it is the case in IC technology). TFTs are transistors manufactured on large glass carriers using thin semiconductor films deposited on the glass surface (amorphous or poly-crystalline silicon, in most cases).

In the last 15 years a clear trend towards lowering the processing temperature of large-area TFT processes has also been emerging. Lower temperatures indeed enable the use of thin, *flexible plastic substrates* that are much more attractive than the fragile and expensive glass sheets used nowadays. These developments have been fuelled by research on semiconductor materials that can be processed at near-to-ambient temperature, like organic and metal oxide semiconductors [3, 4].

Large-area electronics processed at low temperature on flexible substrates enable two sorts of innovative applications: on the one hand, applications that exploit together large area, flexibility and ruggedness, like touch screens, Braille displays [5], pedometers [6], strain gauges, artificial skin [7, 8] and more [9, 10]; on the other hand, applications that exploit these technologies for their simplicity and high throughput, aiming at achieving cost competitiveness with silicon for very cost-sensitive applications with low computational intensity. To this latter category belong, for instance, item-level Radio-Frequency Identification (RFID) tags [11] augmented with sensors, able to monitor the storage and distribution chain of food, pharmaceuticals or expensive chemicals.

Unfortunately large-area electronic processes on foil are still in an initial state of development, and the design of circuitry exploiting this technology must cope today with several drawbacks in terms of variability, ageing and low-performance. In this book, large-area technologies will be used to design building blocks suitable for smart sensors (which integrate electronics along with the actual sensor), with particular focus on the techniques adopted to face the several limitations that still affect the manufacturing process and the transistors on foil.

1.2 Challenges in Electronics on Flexible Substrates

Processing TFTs on large area at near-to-ambient temperatures is normally associated with poor control on the thickness of the single layers, on the spot temperature during the process, and other boundary conditions. For this reason, the variability among different TFTs is very pronounced, and it is difficult to match devices even if they are identical and close-by [12].

The variability and poor matching on the foil are not only due to process parameters varying from point to point, but also to the solid state structure of semiconductors

suitable for low temperature processing. These materials are indeed normally disordered micro or nano-crystalline materials, rather than perfectly uniform mono-crystals like in Silicon ICs. Another source of variability is the contact resistance between source/drain contacts and the semiconductor film [13, 14].

The intrinsic poor performance of semiconducting films processed at low temperature is closely related to their disordered packing. Disorder in the periodicity of the lattice prevents the charge transport from taking place in extended states; on the contrary charge carriers are in localized energy states [15] or “hop” [16] among them. For this reason, mobility typically ranges between 0.1 and 10 cm²/V s [17], which is two or three orders of magnitude smaller than in crystalline silicon.

The reduced mobility translates in small TFT transconductance, while the output resistance is strongly limited by short-channel effects [18–20]. Indeed, in standard thin-film transistor technologies on flexible foils, the gate insulator cannot be scaled down to very thin layers and the control of the gate on the channel is heavily affected by the longitudinal electric field. These two aspects of large-area TFTs result in a maximum intrinsic gain typically ranging between 20 and 26 dB.

All these intrinsic TFT limitations are not the only issues concerning low-temperature semiconductor materials and their process technology. Indeed another important aspect of large-area TFT technologies on foil is the availability of p-type, n-type or complementary transistors. Traditionally, low-temperature processes have been using only p-type organic semiconductors and thus p-type TFTs only [3]. Later on, also n-type TFTs have been processed at low temperature using organic materials [21] or metal oxides (like ZnO [15] or InGaZnO [22]). Even though metal-oxide semiconductors are rapidly becoming a standard technology in display backplane [23], their use in circuits is still in its early infancy.

Only recently, complementary processes have been demonstrated [24, 25] combining two organic materials or exploiting “hybrid technologies” that combine organic p-type with inorganic n-type semiconductors [26]. These processes are inherently more complex than unipolar ones, and typically result in higher defectivity. The most reliable (low defectivity and variability) TFT technologies fabricated at low temperature nowadays still offer, at the state of the art, only p-type normally-on organic TFTs and capacitors. State of the art p-type-only organic TFT circuits have reached a complexity level of 4000 transistors [27], while printed complementary organic technologies offer a maximum complexity of about 100 TFTs in functional circuits [28].

P-type TFTs in low-temperature technologies are typically normally-on devices. Semiconductors with such property are preferred since higher gain, better noise margins and thus higher circuit complexity can be achieved using a logic gate when the active load is implemented with a Zero-V_{gs} connected load (i.e. shorting gate and source of the TFT), compared to the diode-connected load which is the only viable solution for normally-off TFTs. However, normally-on TFTs represent a poor solution for switches or pass-transistors and do not necessarily work in saturation when diode-connected. Therefore, the design of current mirrors is not trivial on one supply rail (V_{DD} for p-type and gnd for n-type), and it is impossible at all on the other. The availability of only one type TFT poses strong limitations to the freedom

of design for analog and digital circuits, and makes the design of reliable digital functions extremely challenging.

A final important issue, which has been only partially solved till now with material research, is the sensitivity of large-area low-temperature TFTs to aging and bias stress in air.

1.3 Book Aims and Overview

The aim of this book is to investigate the diverse major issues relevant to analog, digital and mixed-signal circuit design in large-area TFT technologies. Our first steps move from the modeling and the characterization of the devices and their implementation in a Computer Aided Design (CAD) environment. A clear understanding of the limitations posed by the technology is paramount to developed technology aware solutions applied at different abstraction levels: architectural, circuitual, layout, or device.

Facing each issue at the right abstraction level allows pursuing the optimal solution which is not the one simply fulfilling all the electronic specifications required by the target application, but the one that guarantees high yield and good robustness to enable ultra-low-cost even for low-volume production. Also an increased technology complexity could represent a problem, as it invariably will translate into higher production costs. It is thus important to achieve as much as possible exploiting only unipolar technologies, which will always be cheaper than the complementary counterpart.

The work presented in this book focuses on circuit and system solutions for smart sensors manufactured using low-temperature large-area TFTs. The “smart sensor” is herewith defined as a system capable of physical measurements, first analog signal conditioning, data conversion and wireless data communication to a base station (Fig. 1.2).

Among the required building blocks, the sensor and the RF transceiver fall out of the scope of this book, while circuits necessary to the sensor frontend, as it is

Smart sensor

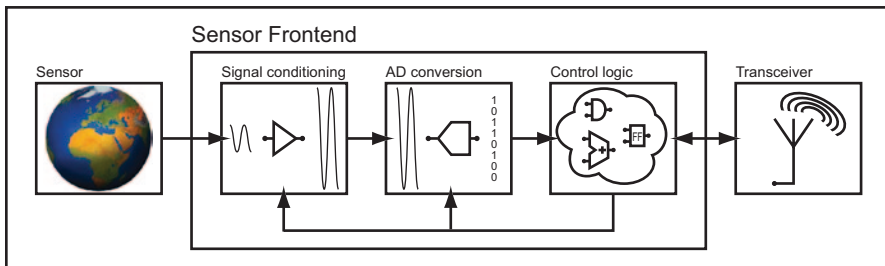


Fig. 1.2 Smart sensor schematic

defined here, have been studied and compared to the literature. More specifically, this book discusses circuits for analog signal conditioning, circuits for data conversion, and a new logic style to implement all the required control logic.

The main design goal is to improve the performance of analog, mixed-signal and digital circuits, and to increase their robustness against process variations and mismatch. In particular, we pursued the improvement of AD and DA converters' accuracy and the robustness of the digital logic.

In order to design the aforementioned sensor front-ends, two different technologies have been employed: the first is an organic double-gate p-type-only technology exploiting pentacene as semiconductor; the second one is a metal-oxide n-type-only technology.

Since the circuit complexity of analog, digital and mixed-signal blocks made with emerging technologies can appear trivial to the eye of a silicon IC designer, the book begins introducing, with Chaps. 2 and 3, large-area applications and technologies, and the state of the art in circuit design for these technologies. The comparison with standard electronics based on silicon clarifies the advantages and the limitations of both. Highlighting these differences is fundamental to understand the challenges imposed by low-cost low-temperature high-throughput manufacturing.

The electrical characterization and modeling of a double-gate p-type TFTs is presented in Chap. 4 with general remarks on process variations, mismatch, bias stress and ageing.

Chapter 5 illustrates the main building blocks necessary to build a smart sensor frontend and the architectural choices made for each taking into account features and drawbacks of the technology.

Chapters 6–8 deal with the design of the sensor frontend at a circuit level: from the analog signal conditioning, through the analog to digital data conversion, to the design of a new logic style suitable for robust digital processing in unipolar technologies.

Finally, conclusions are presented in Chap. 9.

References

1. G.E. Moore. Cramming more components onto integrated circuits. *Electronics* **38**, 114–117 (1965)
2. [Online] Moore's law, http://en.wikipedia.org/wiki/Moore's_law
3. G.H. Gelinck, T.C.T. Geuns, D.M. de Leeuw, High-performance all-polymer integrated circuits. *Appl. Phys. Lett.* **77**(10), 1487–1489 (2000)
4. A.K. Tripathi et al., Low-voltage gallium-indium-zinc-oxide thin film transistors based logic circuits on thin plastic foil: Building blocks for radio frequency identification application. *Appl. Phys. Lett.* **98**(16), 162102 (2011)
5. Y. Kato et al., Sheet-type Braille displays by integrating organic field-effect transistors and polymeric actuators. *IEEE Trans. Electron Devices* **54**(2), 202–209 (2007)
6. K. Ishida et al., Insole pedometer with piezoelectric energy harvester and 2 V organic circuits. *IEEE J. Solid-State Circuits* **48**(1), 255–264 (2013)
7. P. Cosseddu et al., Inkjet printed organic thin film transistors based tactile transducers for artificial robotic skin, in *IEEE RAS and EMBS International Conference on Biomedical Robotics and Biomechatronics*, pp. 1907–1912, 2012

8. T. Hoshi, H. Shinoda, Robot skin based on touch-area-sensitive tactile element, in *IEEE International Conference on Robotics and Automation*, pp. 3463–3468, 2006
9. K. Ishida et al., A 100-V AC energy meter integrating 20 V organic CMOS digital and analog circuits with a floating gate for process variation compensation and a 100 V organic pMOS rectifier. *IEEE J. Solid-State Circuits* **47**(1), 301–309 (2012)
10. T. Yokota et al., Sheet-type flexible organic active matrix amplifier system using pseudo-CMOS circuits with floating-gate structure. *IEEE Trans. Electron Devices* **59**(12), 3434–3441 (2012)
11. E. Cantatore et al., A 13.56 MHz RFID system based on organic transponders. *IEEE J. Solid-State Circuits* **42**(1), 82–92 (2007)
12. H. Fuketa et al., 1 μ m-thickness 64-channel surface electromyogram measurement sheet with 2 V organic transistors for prosthetic hand control, in *IEEE International Solid-State Circuits Conference*, San Francisco, pp. 104–105, 2013
13. P.V. Pesavento, K.P. Puntambekar, C.D. Frisbie, J.C. McKeen, P.P. Ruden, Film and contact resistance in pentacene thin-film transistors: dependence on film thickness, electrode geometry, and correlation with hole mobility. *J. Appl. Phys.* **99**(9), 094504 (2006)
14. R.J. Chesterfield, Variable temperature film and contact resistance measurements on operating n-channel organic thin film transistors. *J. Appl. Phys.* **95**(11), 6396 (2004)
15. F. Torricelli, J. Meijboom, Transport physics and device modeling of zinc oxide thin-film transistors Part I: Long-channel devices. *IEEE Trans. Electron Devices* **58**(8), 2610–2619 (2011)
16. M. Vissenberg, M. Matters, Theory of the field-effect mobility in amorphous organic transistors. *Phys. Rev. B* **57**(20), 964–967 (1998)
17. C.D. Dimitrakopoulos, P.R.L. Malenfant, Organic thin film transistors for large area electronics. *Adv. Mater.* **14**(2), 99–117 (2002)
18. N.H. Toudjen, F. Mansour, Modeling kink effect in the poly-Si TFTs under charge sheet approach, in *International Conference on Advances in Computational Tools for Engineering Applications*, pp. 407–410, 2009
19. L. Mariucci et al., Polysilicon TFT structures for kink-effect suppression. *IEEE Trans. Electron Devices* **51**(7), 1135–1142 (2004)
20. C.R. Wie, Nonsaturating drain current characteristic in short-channel amorphous-silicon thin-film transistors. *IEEE Trans. Electron Devices* **57**(4), 846–854 (2010)
21. A. Facchetti et al., Organic-inorganic flexible and transparent electronics, in *Flexible Electronics and Displays Conference and Exhibition*, pp. 1–7, 2008
22. H. Hosono, M. Yasukawa, H. Kawazoe, Novel oxide amorphous semiconductors: transparent conducting amorphous oxides. *J. Non-Cryst. Solids* **203**, 334–344 (1996)
23. L.G. 55-inch OLED TV, [Online], <http://reviews.cnet.co.uk/tvs/lg-55-inch-oled-tv-review-50006604/>
24. T. Zaki et al., A 3.3 V 6-bit 100 kS/s current-steering digital-to-analog converter using organic p-type thin-film transistors on glass. *IEEE J. Solid-State Circuits* **47**(1), 292–300 (2012)
25. S. Jacob et al., High performance printed N and P-type OTFTs for complementary circuits on plastic substrate, in *IEEE European Solid-State Device Research Conference*, pp. 173–176, 2012
26. K. Myny et al., Bidirectional communication in an HF hybrid organic/solution-processed metal-oxide RFID tag, in *IEEE International Solid-State Circuits Conference*, pp. 312–314, 2012
27. K. Myny et al., An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil. *IEEE J. Solid-State Circuits* **47**(1), 284–291 (2012)
28. S. Abdinia et al., A 4b ADC manufactured in a fully-printed organic complementary technology including resistors, in *IEEE International Solid-State Circuits Conference*, pp. 106–107, 2013

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