

## Chapter 2

# Background on Time-to-Digital Converters

**Abstract** Time-to-digital converters (TDCs) are key building blocks in time-based mixed-signal systems, used for the digitization of analog signals in time domain. Some commonly used TDC structures are summarized in this chapter. By carefully analyzing their advantages and performance constraints, it has been concluded that in order to design a megagray radiation-tolerant TDC, an innovative and reliable architecture must be developed. More technical details regarding the investigation of this new TDC type will be given in Chap. 4. In order to obtain a fair comparison between the TDC proposed in this book and other state-of-the-art TDCs, performance measures of TDCs are also given in this chapter.

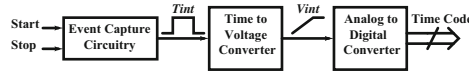
### 2.1 Introduction

Recently, high resolution time-to-digital converters (TDCs) have gained more and more interest due to their increasing implementation in digital phase-locked loops (PLLs), analog-to-digital converters (ADCs), jitter measurement, and time-of-flight (TOF) range finders. A TDC is a device used to measure a time interval and convert it into digital output. In its simplest implementation, a TDC can be simply a high-frequency counter that increments every clock cycle. However, the time resolution of this type of TDC is practically limited by the highest available clock frequency.

In the next section, an overview of other state-of-the-art fine time measurement methods with much better accuracy but smaller measuring range is given. Performance measures of different TDCs are also discussed in this chapter.

### 2.2 TDC Topologies

Quantizing the time interval between a start signal and a stop signal, and representing it as a digital code, is the basic task of a TDC. The first TDCs were actually performing in two steps: time-to-voltage conversion (TVC), followed by voltage-to-digital conversion (VDC), as in [69, 86] (Fig. 2.1). The time signal is mapped into an analog voltage in the first phase, by using a charge pump. The amplitude of the voltage corresponds to the width of the time frame. In the second step, this voltage is translated into a digital code by a conventional ADC. A 30 ps resolution is the



**Fig. 2.1** Block diagram of the TVC–VDC architecture. *TVC* time-to-voltage conversion, *VDC* voltage-to-digital conversion

best that has ever been reported based on this configuration [69]. The performance is mainly limited by the nonlinearity in the TVC unit and the resolution of the ADC. Moreover, as technologies scale down, this approach becomes less attractive. The strongly scaled supply voltage but relatively unchanged threshold voltage, raises significant challenges in the design of a high-performance ADC, and restricts the input range of the TDC.

As opposed to the traditional analog method, a TDC could be also designed in time domain, where a circuit gains most profits from technology downscaling in terms of speed, power consumption, and area. The simplest time domain TDC is a counter. By using a high-speed low-jitter reference clock, the counter can digitize a time signal with moderate resolution. However, when the requirement for the TDC resolution is increased to a few picoseconds, the reference clock frequency becomes unreasonably high ( $> 100$  GHz) with respect to power consumption and system complexity. Therefore, a real TDC employs phase-aligned parallel counting clocks to achieve high resolution rather than using a single external reference clock. A complementary metal–oxide–semiconductor (CMOS) gate delay line can serve this purpose. Many TDC architectures based on a delay line core are reported in the past decade, and some achieve better than 10 ps resolution. They can be summarized into following categories:

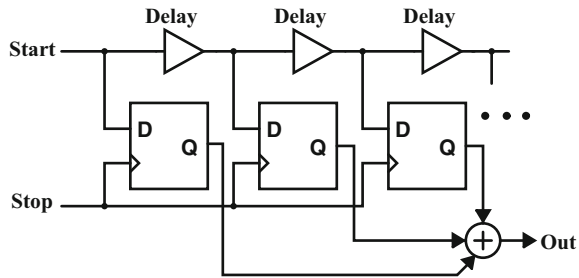
- Flash TDC [25, 37, 38, 41, 82, 95].
- Pipeline TDC [49, 74].
- Successive approximation TDC [53].
- Noise-shaping TDC [83].

Similar to their ADC counterparts, each type of TDC performs well in one area, e.g., resolution, bandwidth, robustness, or power consumption, and lacks in another, as will be discussed below.

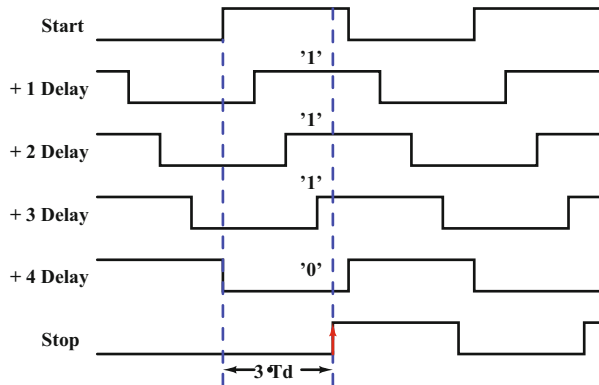
### 2.2.1 Flash TDC

A flash TDC uses a linear delay-cell ladder with a D flip-flop (DFF) at each rung of the ladder to compare the input time signal to successive reference time units [82], as shown in Fig. 2.2. A start signal propagates along the delay line, and the state of each delay element is sampled on the rising edge of the stop signal. A thermometer code is then generated at the DFFs' output, which represents the time difference between the start and stop signals. The timing and waveforms at the input of each DFF are illustrated in Fig. 2.3. The advantages of this circuit are obvious. It employs a very simple structure with only delay cells and DFFs. Hence, it is very area efficient. The

**Fig. 2.2** Basic structure of a delay-line-based flash TDC.



**Fig. 2.3** Timing of the delay-line-based flash TDC.

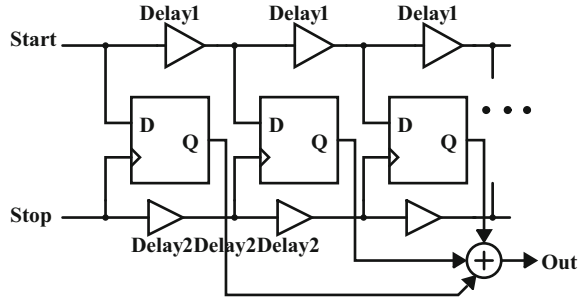


resolution is determined by the intrinsic CMOS gate delay, which scales according to the technology scaling factor. But practically, the TDC resolution does not continue to improve with technology downscaling, due to the worsened mismatch problem between delay cells. Therefore, the finest achievable resolution of the basic delay-line TDC is limited to around 20 ps.

In order to obtain sub-gate-delay resolution, the Vernier method [25] is commonly used, as shown in Fig. 2.4. Instead of using only one delay chain, the Vernier TDC utilizes two independent delay lines on both start and stop signal paths to improve the time resolution. The delay elements on the stop path are designed slightly faster than those on the start path. Both start and stop signals propagate along two delay lines with an initial time difference of  $T_{in}$ . The conversion is completed only after the stop signal outruns the start signal. The resolution of the Vernier TDC is then given by  $t_{\text{delay}1} - t_{\text{delay}2}$ . However, along with the resolution, the sensitivity of the Vernier TDC to mismatch has also been amplified. Although calibration can be applied to compensate for this error [37], significant efforts are needed since each delay element in the TDC has to be corrected individually.

Another technique to improve TDC resolution below that of a gate delay is to subdivide the coarse time interval given by an inverter delay line. This concept can be realized by placing a resistor divider between two nodes of an inverter, as presented in [38]. The divider interpolates the input and output signals of the digital gate, and creates new intermediate signals which effectively divide the gate delay into smaller intervals. The improvement in resolution for the interpolation architecture over the

**Fig. 2.4** Basic structure of a Vernier delay-line TDC. TDC time-to-digital converter



gate delay is similar to that of the Vernier architecture, and is practically limited by the nonlinear impedance of the delay elements during signal transients.

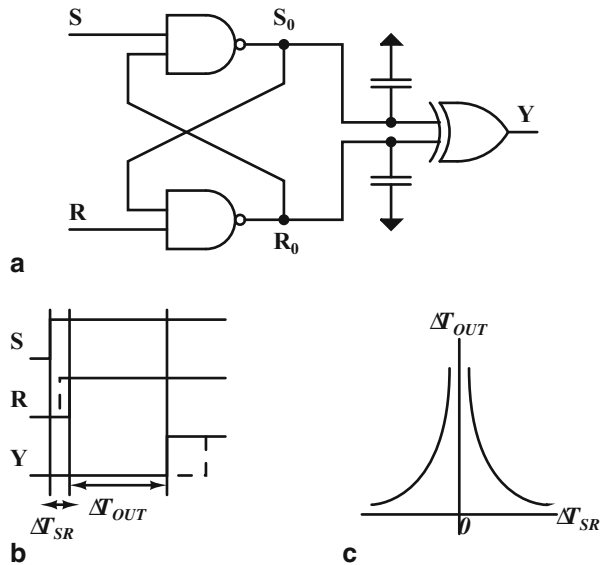
Since a flash TDC works at the Nyquist conversion rate, a large signal bandwidth can be obtained. High resolution is achievable at the cost of increased power consumption and area penalty. In practice, the random variations among delay elements set up an upper bound for the resolution of a flash TDC. To obtain well-controlled delay cells, the basic delay line core can be placed in a delay locked loop (DLL), as suggested in [41].

### 2.2.2 Pipeline TDC

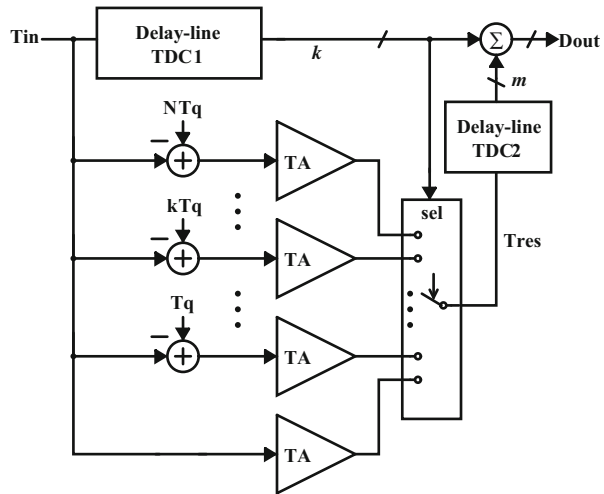
It is well-known that, a pipeline ADC uses two or more steps of subranging and residue amplification technique to achieve high resolution. The same idea can also be realized in the design of TDCs, with the help of a time amplifier (TA). The working principle of the TA is illustrated in Fig. 2.5. An set–reset (SR) latch followed by an exclusive-OR (XOR) gate, is the main building block of the TA. If rising edges are applied to S and to R at almost the same time, the latch will be metastable. The initial voltage difference developed at the output of the SR latch is proportional to the input initial time difference  $\Delta T_{SR}$ . The positive feedback in the latch forces the outputs of both NAND gates eventually to a binary level, which toggles the XOR gate to 1, and complete the regeneration process. The relationship of the regeneration time and the initial time difference is a logarithmic function as shown in Fig 2.5c.

Figure 2.6 shows the conceptual diagram of a pipeline TDC, which was proposed in [49]. First, the input time signal is digitized by a coarse flash TDC. The conversion result is then converted back to a reference time and subtracted from the original input. The residue time is then applied to another flash TDC after amplification. The effective resolution of the second flash TDC is thereby improved by a factor of the gain of the TA. However, unlike voltage, the residue time cannot be stored unless it is transformed to other forms such as voltage or current. Therefore, in a pipeline TDC, every possible time residue must be created and amplified separately. This significantly increases the system latency, and limits the input range of the TDC, since the linear working region of the TA is quite restricted. Moreover, the gain of the TA is also very sensitive to its working environment, mismatch, and process variation.

**Fig. 2.5** **a** Basic architecture, **b** timing diagram, and **c** relationship between the regeneration time and the initial time difference of the time amplifier

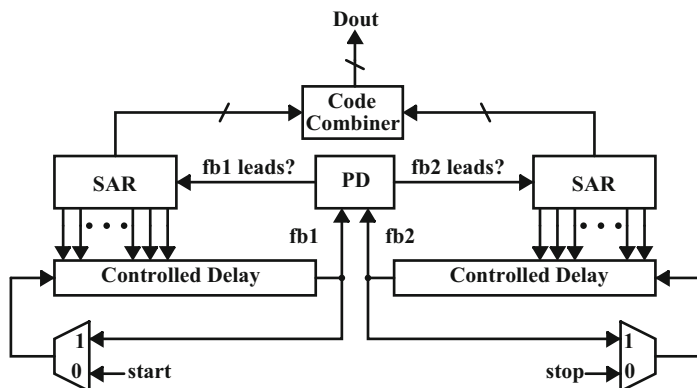


**Fig. 2.6** Conceptual diagram of the TA-based pipeline TDC. TA time amplifier, TDC time-to-digital converter



### 2.2.3 Successive Approximation TDC

Successive approximation has been widely used in the design of ADCs to reach high resolution at the cost of conversion time. In the time domain, a successive approximation TDC [53] resolves the time difference between the start and stop signal one bit at a time in  $N$  cycles using binary search, as illustrated in Fig. 2.7. Due to the irretrievable nature of a time signal, the bidirectional adjustment required by the binary search is implemented by making both signal paths adjustable, rather than



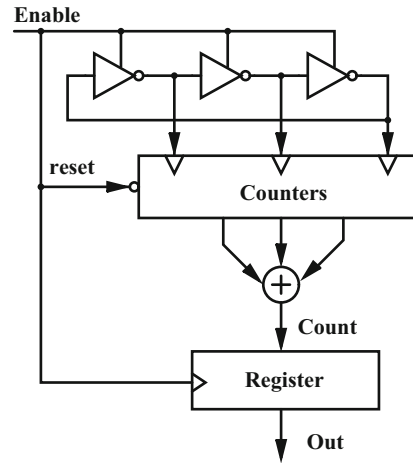
**Fig. 2.7** Signal flowchart of the successive approximation TDC. *TDC* time-to-digital converter

adjusting only one signal back and forth. The two delayed versions of input signals, *fb1* and *fb2*, propagate cyclically in two separate loops formed by digital-to-time converters (DTCs), whose delays are controlled by the successive approximation register (SAR). At the beginning of the conversion, the DTC at the start path has a delay of  $T_{REF}/2$ . The relative timing of *fb1* and *fb2* is compared with a phase detector (PD) to determine which signal is lead. The SAR will adjust its value according the output of the PD. Whenever the signals *fb1* and *fb2* are aligned within one LSB, the conversion is complete. The fine resolution of the SAR TDC is obtained by interpolation. For an 8-bit operation, 128 unit interpolators (e.g., capacitors) are needed in one DTC, which occupies large area. In order to achieve wide input range, the SAR TDC has to be configured as a coarse–fine architecture, which has more severe matching problems and consumes more power.

## 2.2.4 GRO TDC

A gated ring oscillator(GRO) TDC with first-order noise shaping has been reported in [83]. It can be considered as a first-order  $\Delta\Sigma$  TDC. In the GRO TDC, the input time signal is used to enable/disable a ring oscillator, as illustrated in Fig. 2.8. One single measurement is done by counting all the phase transitions in the oscillator during the enabling phase. The quantization error, which refers to the intermediate state of the oscillator, is preserved between measurements. This results in a first-order noise shaping on the quantization noise. After digital low-pass filtering, the signal can be reconstructed with strongly reduced quantization error. The theory of time domain noise shaping will be discussed more in detail in Chap. 4. One issue in the GRO TDC, which could completely disrupt the noise-shaping behavior, is the existence of large skew error, as shown in Fig. 2.9. Caused by the charge redistribution during the “silent” phase of the TDC, the skew error results in imperfect preservation of the

**Fig. 2.8** Basic structure of the GRO TDC. *GRO* gated ring oscillator

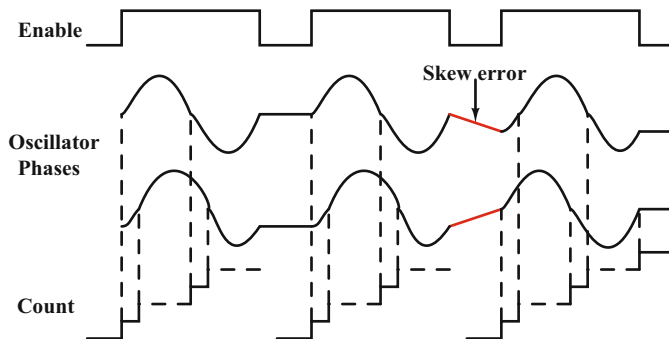


quantization error. Another drawback of the GRO TDC, is the difficulty of achieving high-order noise shaping with this structure, which could principally further improve the TDC resolution and reduce the need for fast delay elements.

## 2.3 Performance Measures

### 2.3.1 Raw Resolution

The raw resolution of a TDC is the minimum quantization step of the system. In delay-line-based flash TDCs, this is equal to the delay time of one single delay cell,  $T_d$ . In counter-based TDCs, the raw resolution equals to one period of the counting clock,  $T_{OSC}$ .



**Fig. 2.9** Timing diagram of the GRO TDC. *GRO* gated ring oscillator

### 2.3.2 *Single-Shot Precision*

If a constant time interval is measured repeatedly, the digital output values vary with a standard deviation that is called single-shot precision. In certain circumstances, a very small single-shot precision is of importance when repeated measurement is not possible. For instance, in the CMS experiment mentioned in Chap. 1, the time of-arrival of generated particles after a collision event needs to be measured. Apparently, there is only one chance to conduct an accurate measurement before the particle has fled out.

However, for many other industrial applications, repeated measurement of the same time interval is feasible as soon as the repeating frequency is much higher than the varying frequency of the input time signal's amplitude. In the LIDAR experiment, this is mostly the case. Therefore, the single-shot precision is not focused during the design of the radiation-tolerant  $\Delta\Sigma$  TDC for LIDAR application.

### 2.3.3 *Sampling Rate*

In order to achieve a stable measurement of the input coming signal, a TDC is often configured in a closed-loop system. For instance, in a basic flash TDC, the delay line is placed in a DLL, which reduces nonlinear errors caused by mismatch. In such a closed-loop structure, the system is refreshed at a fixed frequency, which is defined as the sampling rate ( $F_s$ ) of the TDC.

### 2.3.4 *Bandwidth*

The bandwidth of a TDC is the range of input signal frequencies it can measure. For flash TDCs, this is mostly half of their sampling frequency according to Nyquist theorem. For oversampling TDCs, it is equal to  $F_s/(2 \cdot \text{OSR})$ , where OSR is the oversampling ratio.

### 2.3.5 *Effective Resolution*

The effective resolution is the actual resolution of a TDC when circuit noise and mismatch effects are taken into account. In flash TDCs, the effective resolution is usually worse than its raw resolution. However, in  $\Delta\Sigma$  TDCs, the raw resolution can be further improved by oversampling and noise shaping. Therefore, within the interested signal bandwidth, the noise-free effective resolution of a first-order  $\Delta\Sigma$



TDC can be expressed as

$$T_{\text{eff}} = \frac{\pi \cdot T_d}{6 \cdot \sqrt{\text{OSR}^3}}, \quad (2.1)$$

where OSR is the oversampling ratio, and  $T_d$  is the raw resolution. Of course, when circuit noises are added into the figure, the real effective resolution will be worse.

### 2.3.6 SNDR and ENOB

SNDR is defined as the signal to noise plus distortion ratio within the interested signal bandwidth. It is the major figure which is used to measure a TDC's dynamic performance:

$$\text{SNDR} = \frac{P_{\text{signal}}}{P_{\text{quantizationerror}} + P_{\text{radomnoise}} + P_{\text{distortion}}}, \quad (2.2)$$

where  $P$  is the average power of the signal, quantization error, circuit random noise, and distortion components.

Effective number of bits (ENOB) specifies the number of bits in the digitized signal above the noise floor. SNDR (in dB) is related to ENOB by the following equation:

$$\text{SNDR} = \text{ENOB} \cdot 6.02 + 1.76. \quad (2.3)$$

### 2.3.7 Dynamic Range

Similar to an ADC, the dynamic range (DR) of a TDC is defined as the maximum time interval that can be measured without any saturation effects. In the LIDAR experiment, a large DR is more preferred since the system's detection range needs to go over 30 m, meanwhile, the required resolution is 1 mm. It turns to a DR of

$$\text{DR} = 20 \cdot \log \left( \frac{A_{\text{fullrange}}}{A_{\text{noise,rms}}} \right) = 20 \cdot \log \left( \frac{30}{1 \times 10^{-3}} \right) = 90 \text{ dB!} \quad (2.4)$$

Radiation-Tolerant Delta-Sigma Time-to-Digital  
Converters

Cao, Y.; Leroux, P.; Steyaert, M.

2015, XIX, 114 p. 86 illus., 30 illus. in color., Hardcover

ISBN: 978-3-319-11841-3