

Chapter 2

Analysis of Quantization Noise Reduction Techniques for Fractional-N PLL

2.1 Background

High performance phase locked-loops (PLL) are widely used in wireless communication systems to provide low noise local oscillation (LO) signals for digital modulation and demodulation. It has large applications in electronic devices such as cell phones, remote control devices, laptops, and alarm systems. Usually a simple integer-N PLL consists of phase-frequency detector (PFD), charge pump, loop filter, VCO, and dividers. One drawback of integer-N PLL is that its frequency resolution is limited to the reference frequency. Thus, an integer-N PLL has to use low reference frequency to achieve fine frequency tuning step, which leads to large loop division ratio and degraded phase noise. Unlike integer-N PLL, fractional-N PLL can achieve a frequency step much smaller than its reference and still maintain reasonably high reference frequency, which is the key for achieving the low phase noise performance. However, the fractional control module used in a fractional-N PLL produces quantization noise and spurs at the PLL output, which deteriorates the spectral purity of the synthesized signals.

A classic fractional-N PLL usually contains an accumulator or sigma-delta ($\Sigma\Delta$) modulator as the fractional control module to dynamically control the divider ratio. The instantaneous division ratio of the divider can only be an integer number, but its long-term average of the divide ratio is $N+\alpha$, whereas α is a fractional number. Therefore, the instantaneous phase error appearing at the input of the PFD is not always zero. This phase error modulates the tuning line of a VCO and thus creates spurious tones at the PLL output. The loop bandwidth can be reduced to filter out the quantization noise and spurs resulted from the fractional control module. However, it is highly desirable to increase the loop bandwidth of a PLL to remove the VCO noise and to speed up the lock-in time for applications that requires fast switching speed, such as Bluetooth. In this chapter, phase error compensation techniques are developed to help address these problems.

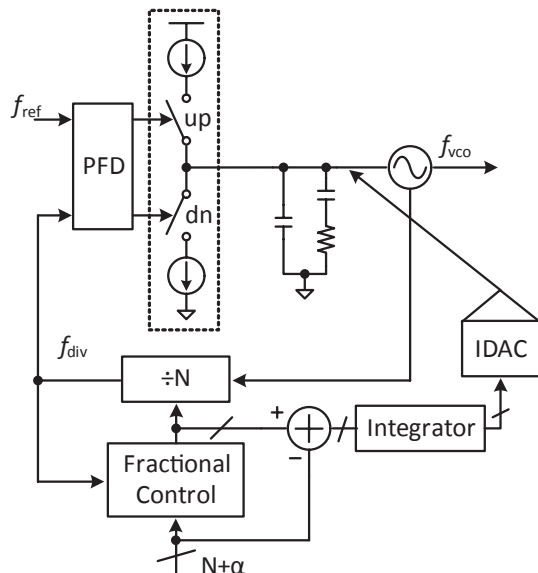
Accumulator-based fractional-N PLL structure is simple but it has very large fractional spurs at the PLL output. Therefore, $\Sigma\Delta$ modulator structures have been proposed to implement the fractional-N frequency synthesis [1, 2, 3]. Quantization

noise generated at the output of a $\Sigma\Delta$ modulator will be pushed to high frequency offset which can be filtered by the low-pass loop filter of the PLL. The higher the order a $\Sigma\Delta$ modulator is, the better the noise shaping effect will be. Even though the PLL loop can provide some filtering effect to the high-pass shaped quantization noise, the filtered noise may still dominate the out-of-band noise, especially for higher order $\Sigma\Delta$ modulator. In addition, the nonlinearity of the PLL, mainly caused by the nonlinear transfer function of the charge pump, will fold the shaped noise into low frequency offset [4, 5]. In this case, the loop filter cannot filter the noise folded back into the low frequency offset. The in-band noise can become worse when a very nonlinear charge pump is used. A charge pump linearization technique is proposed to improve the phase noise performance [5].

However, the abovementioned charge pump linearization technique does not remove the quantization noise source. Thus, to reduce the fractional control module noise, several noise cancelling techniques have also been proposed for fractional-N PLL. A pulsed amplitude-modulated current can be injected into the loop filter to compensate the phase error [6, 7]. Figure 2.1 shows such a PLL system with the quantization noise cancelling technique. The current is generated from a current DAC with fixed pulse width. The quantization noise existing at the output of a $\Sigma\Delta$ modulator can be compensated with an opposite current pulse. But the mismatch between the phase error and the compensation DAC may lead to inadequate cancellation. The minimum achievable noise is usually limited by the DAC resolution and mismatch between the forward path through DAC and the feedback path through PFD.

Another noise compensation technique for an accumulator-based fractional-N PLL [8] achieves better noise cancellation results by using PFD/DAC due to its embedded charge pump in the compensation path. However, the proposed technique can only be used to for accumulator or first order $\Sigma\Delta$ modulator-based PLL since

Fig. 2.1 System diagram of fractional-N PLL with quantization noise cancelling



this technique only compensates a phase error within 0–1 VCO period. However, $\Sigma\Delta$ modulators with orders of two or three have an accumulated phase error in the range of -2 to $+2$ VCO period. It is highly desirable to develop structure that is able to compensate phase error larger than one VCO period.

This chapter will analyze several different $\Sigma\Delta$ modulator structures and the properties of their quantization noise. Section 2.2 introduces different types of $\Sigma\Delta$ modulator structures and their noise-shaping effects. Noise degradation resulted from loop nonlinearity and corresponding model is discussed for $\Sigma\Delta$ modulator-based PLL. A noise cancelling technique for higher-order fractional-N PLL with its implementation details is described in Sect. 2.3. Finally, conclusion is given to end this chapter.

2.2 $\Sigma\Delta$ Modulators and Noise Folding from Nonlinearity

2.2.1 Introduction of Different $\Sigma\Delta$ Modulators

In order to avoid the spurious tone in the PLL phase noise spectrum, the $\Sigma\Delta$ modulator is usually of orders equal or higher than two. However, the modulators with orders higher than three are not so popular since their out-of-band noise may be much higher than the VCO noise and cannot be efficiently filtered by the loop. On the other hand, higher order will increase the hardware complexity of digital implementation. Therefore, the most popular $\Sigma\Delta$ modulators are of second or third order. MASH1-1, as shown in Fig. 2.2a, is a very classic second order $\Sigma\Delta$ modulator, which consists of two cascade accumulators [9]. It provides second-order noise shaping for the quantization noise with a noise transfer function of $(1 - z^{-1})^2$.

Figure 2.2b shows a third-order MASH1-1-1 $\Sigma\Delta$ modulator. It is simple and unconditionally stable because it does not have feedback path [10]. The overflow at the output of the accumulator is usually of one bit, i.e., either 0 or 1, so the output of MASH1-1-1 is in the range of -3 to $+4$ while that of MASH1-1 is in the range of -1 to $+2$. The MASH structure is suitable for very high clock frequencies because of its pipeline operation.

Another popular third order $\Sigma\Delta$ modulator is single-stage multiple feedforward (SSMF) structure as shown in Fig. 2.2c. The coefficient a , b , c in the figure can be Riley- $(2, 1, 0.25)$ or Rhee- $(2, 1.5, 0.5)$, but with different noise transfer function expressed as [1, 2]:

$$H_{\text{Riley}}(z) = \frac{(1 - z^{-1})^3}{1 - z^{-1} + 0.25z^{-3}} \quad (2.1)$$

$$H_{\text{Rhee}}(z) = \frac{(1 - z^{-1})^3}{1 - z^{-1} + 0.5z^{-2}} \quad (2.2)$$

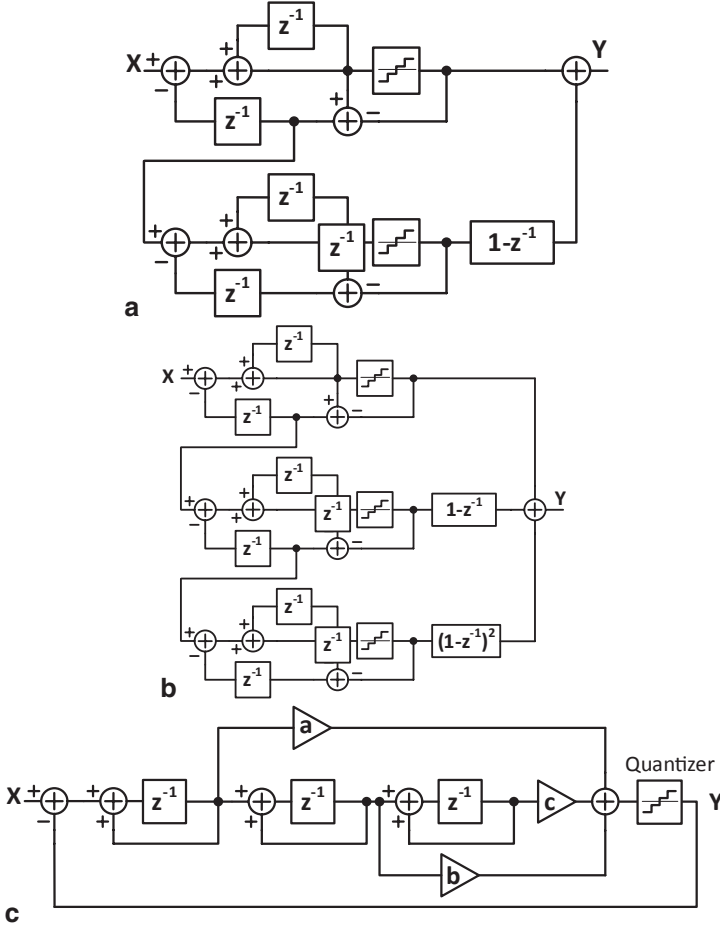


Fig. 2.2 $\Sigma\Delta$ modulator structures: **a** MASH1-1, **b** MASH1-1-1, and **c** SSMF

The output range of the SSMF structure is smaller than that of the MASH1-1-1 structure. The PLL with SSMF structure also shows smaller instantaneous phase error at the input of PFD. The output noise spectrum should be compared to find the optimum $\Sigma\Delta$ modulator structure for a specific application. Figure 2.3 shows the output spectrum of the abovementioned four $\Sigma\Delta$ modulators. It is obvious that the third-order $\Sigma\Delta$ modulators provide better noise shaping effect than the second-order modulator. Among the third-order $\Sigma\Delta$ modulators, MASH1-1-1 structure has the minimum noise at low frequency offset but highest noise at high frequency offset. The choice of $\Sigma\Delta$ modulator topology depends on the specifications in its real applications. Ideally if better in-band noise is the goal, then MASH1-1-1 would be the best option. On the contrary, SSMF structure should be selected if the noise specification at half the sampling frequency is important. However, this intuitive choice is not always true when considering the nonlinearity of PLL loop, which will be discussed later.

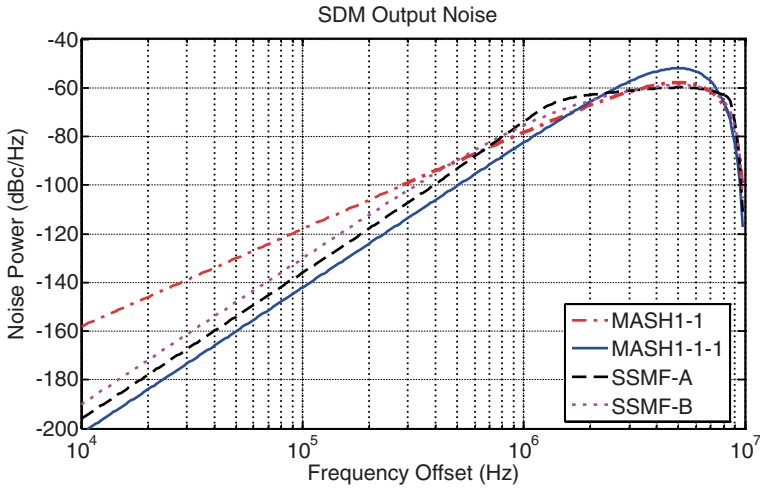


Fig. 2.3 Noise power of different $\Sigma\Delta$ modulators with 10 MHz sampling clock frequency

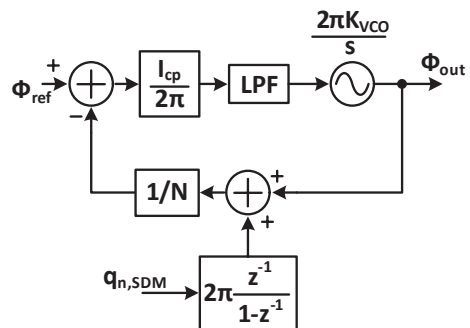
The quantization noise power shown in Fig. 2.3 is actually the shaped noise at the output of the $\Sigma\Delta$ modulators. To evaluate the impact of $\Sigma\Delta$ modulator noise, the quantization noise is converted to the phase noise spectrum at the PLL output. A $\Sigma\Delta$ modulator-based fractional-N PLL constantly dithers the divider value at a high rate compared to the bandwidth of the loop. An integrator is included before adding to the PLL loop as shown in Fig. 2.4 to convert the frequency domain noise to phase domain signals, whereas the control signal from $\Sigma\Delta$ modulator causes an instantaneous change in the frequency of the divider output.

By including the effect of integrator, the phase noise spectrum for MASH1-1-1 structure should be expressed as [11]

$$N_{\text{MASH111}}^2(f) = \frac{\pi^2}{3} \left[2 \sin \left(\pi \frac{f}{f_s} \right) \right]^{2(3-1)} \quad (2.3)$$

where white quantization noise spectra is assumed. Then, the phase noise contribution from quantization noise is low-pass filtered before reaching the PLL output.

Fig. 2.4 PLL model including $\Sigma\Delta$ modulator noise



2.2.2 Nonlinearity Analysis for $\Sigma\Delta$ Modulators

The previous analysis is based on linear-time invariant model. The nonlinear effects of the PLL loop, especially gain mismatch of the charge pump caused by channel length modulation or dynamic switching, is not included in the model. However, the loop nonlinearity has very significant impact on the PLL phase noise caused by $\Sigma\Delta$ modulator. A phase-domain behavioral model as shown in Fig. 2.5 is used to analyze the nonlinear effect on $\Sigma\Delta$ modulator noise contribution.

Figure 2.6 shows the simulated phase noise spectrum of the four types of $\Sigma\Delta$ modulators with 3% absolute gain mismatch in the nonlinear transfer function whereas the gain mismatch is defined as

$$\delta = \frac{I_{pos} - I_{neg}}{I_{pos} + I_{neg}} \quad (2.4)$$

Fig. 2.5 Behavioral model to examine the nonlinearity effect on the $\Sigma\Delta$ modulator quantization noise

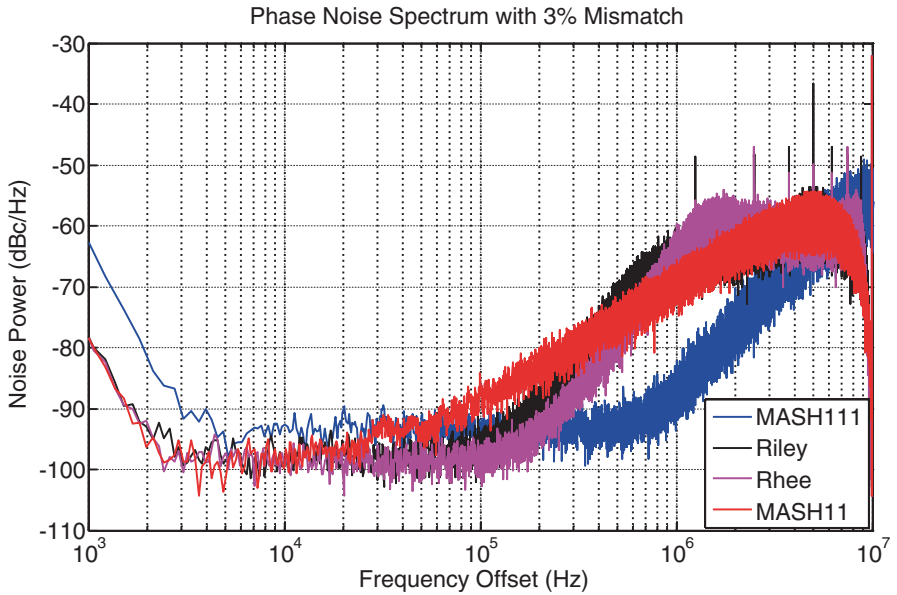
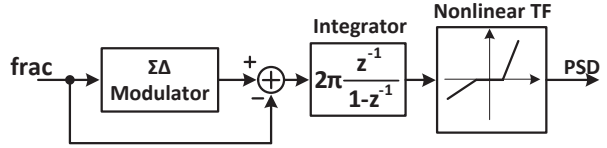


Fig. 2.6 Phase noise spectrum of MASH1-1 and MASH1-1-1 with 3% gain mismatch in the transfer function

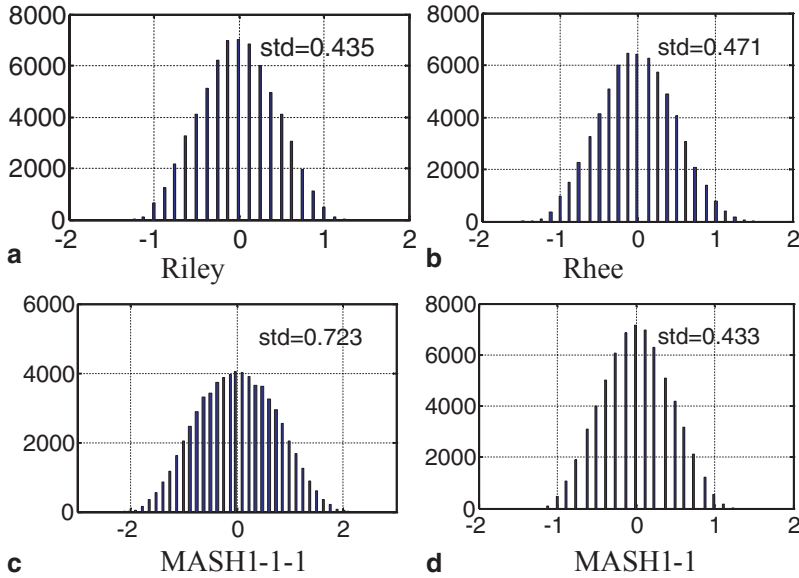


Fig. 2.7 Distribution of phase error at the input of PFD for different $\Sigma\Delta$ modulators

where I_{pos} and I_{neg} are the absolute positive gain and negative gain, respectively. From the simulation results, we can see that the in-band noise degradation for MASH1-1-1 modulator is higher than all the other three structures. This disadvantage is caused by its large output range from -3 to $+4$. The noise folding at low frequency offset for the two SSF structures are very close to each other because their output range is similar. Both the two SSF structure have fractional spurs above 1-MHz frequency offset while Riley's structure shows less spurious tones. Therefore, the choice of $\Sigma\Delta$ modulator structures is highly dependent on the noise specifications of the real application.

As a matter of fact, the in-band noise degradation can also be explained by observing the standard deviation of the $\Sigma\Delta$ modulator output range. Figure 2.7 shows the distribution and standard deviation of the four $\Sigma\Delta$ modulator structures. MASH1-1-1 structure exhibits an instantaneous phase error range of $-2 \sim +2$ while the other three structures show an error range around $-1 \sim +1$. The standard deviation for MASH1-1-1 is largest among the four structures, which explains why it has the highest in-band noise degradation due to the loop nonlinearity. The larger the output range, the worse the noise folding at low frequency offset. Therefore, it is highly desirable to improve the linearity of charge pump circuit since the noise folding is directly affected by its nonlinearity.

2.2.3 Quantization Noise Reduction Techniques

One of the simplest techniques used to reduce the nonlinearity is to improve the linearity of the charge pump circuit. The best achievable linearity is limited by the technology process and charge pump structure. A popular charge pump linearization

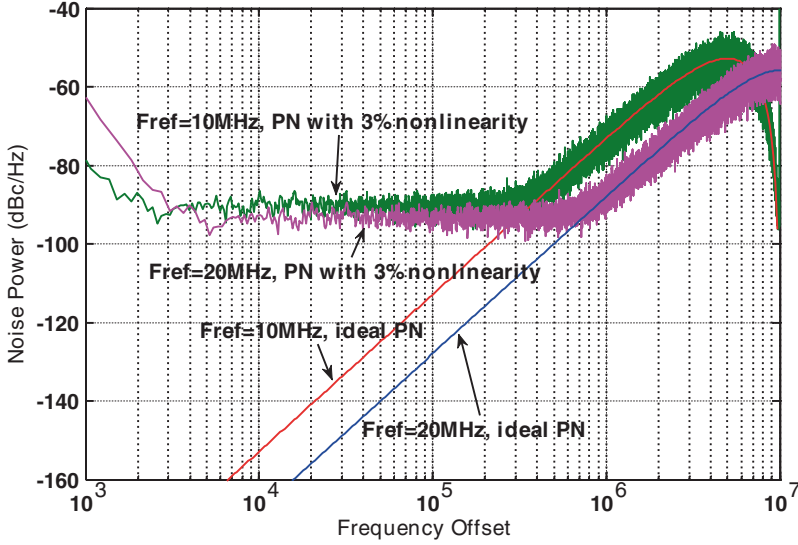


Fig. 2.8 Simulated noise improvements by doubling the clock frequency under 3% gain mismatch

technique is to add a constant offset current into the charge pump and shift the transfer function [12]. Then, the PLL will allow the charge pump operating at only its positive or negative transfer function which has very good linearity performance.

Another simple but efficient technique for phase noise improvement is to double the reference frequency [13]. Ideally the phase noise can be improved by

$$\Delta_{PN} = 6n - 3\text{dB} \quad (2.5)$$

where n is the order of the $\Sigma\Delta$ modulator. At far-away frequency offset, the improvement follows Eq. (2.5). However, the noise improvement for the in-band noise is less than the expected value because of the nonlinearity. It has only 3 dB improvement at low frequency offset as shown in Fig. 2.8.

2.3 A Novel Noise Cancellation Technique for Fractional-N PLL

This section discusses a new quantization noise cancellation technique for high-order $\Sigma\Delta$ modulator-based fractional-N PLL. Similar to conventional compensation technique with DAC currents, the proposed noise cancellation technique also injects current pulses into the loop filter. Usually the phase error can be compensated in three ways: (a) pulse-width modulated (PWM) current pulses; (b) pulse-amplitude modulated (PAM) current pulses; (c) combination of PWM and PAM.

The conventional fractional-N PLL can be modified by adding only a small cost of digital control logic to implement the proposed noise compensation technique. Typically a multi-modulus divider is used to divide the high-speed VCO signal to reference frequency. The divider in the fractional-N PLL will up or down count N-cycle of VCO period to implement the N-divider. This feature can be utilized to produce PWM current. With an auxiliary counter, a current pulse with X VCO cycles can be injected into the loop filter and compensate the instantaneous phase error. The main limitation for this technique is that X should be smaller than the division ratio of N. Moreover, the PLL in-band noise may increase because the long on-time of the DAC current injects more thermal noise into loop filter.

Another technique using PAM current pulses can also be implemented with current DAC. This technique is useful for fractional-N PLL with phase error in the range of 0~1 VCO periods. However, it requires large area of current DAC circuit to compensate phase error in the range of -2~2 VCO periods for high-order $\Sigma\Delta$ modulators. Therefore, a compensating circuit that can generate both positive and negative phase error is preferred to cancel the quantization noise.

Figure 2.9a shows the system diagram of the proposed fractional-N PLL using the combination of PAM and PWM current pulses for high-order $\Sigma\Delta$ noise cancellation. The charge pump produces PAM signal while the PWM signal is produced by the pulse generation module. The PFD block, as shown in Fig. 2.9b, produces up and down control signal for the switches in the charge pump.

One detailed implementation of pulse control module is illustrated in Fig. 2.10. Only 2-bit pulse width control is used in this compensation scheme, other lower bits are implemented by DAC current. For example, if 6-bit DAC current is used, then the compensation algorithm can achieve an accuracy of 8-bit resolution by combining the pulse width control and DAC current injection. The area cost is relatively smaller than compensating techniques using only DACs.

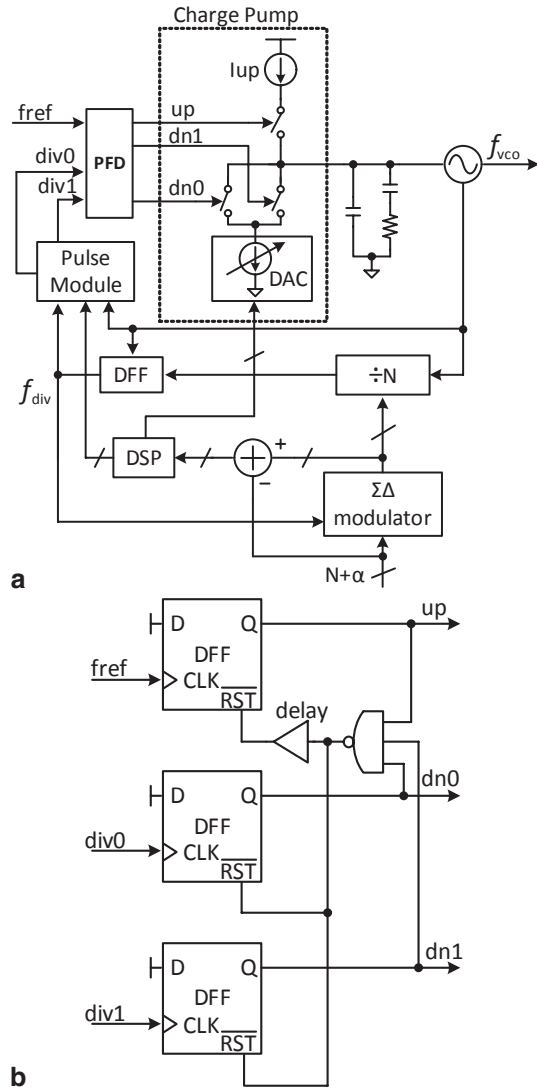
Figure 2.11 illustrates the operating principles of the proposed noise compensation algorithm with phase error in the range of $(-2, 2)$ times T_{VCO} . The turn-on time of the down current equals to $T_X + 2T_{VCO}$ under locked condition. Take the second cycle for example, the phase error equals to $1 + \varepsilon T_{VCO}$, then integrated current in that comparison period can be expressed as

$$\begin{aligned} Q_{p2} &= -I \cdot [T_X + (1 + \varepsilon)T_{VCO} - 4T_{VCO} + (1 - \varepsilon)T_{VCO}] + I \cdot t_d \\ &= I \cdot (T_X - 2T_{VCO} + t_d) \end{aligned} \quad (2.6)$$

Similarly, the integrated current in the fourth comparison period can be expressed as

$$\begin{aligned} Q_{p4} &= -I \cdot [T_X - (1 + \varepsilon)T_{VCO} - T_{VCO} + (1 - \alpha)T_{VCO}] + I \cdot t_d \\ &= I \cdot (T_X - T_{VCO} + t_d - \varepsilon T_{VCO} - \alpha T_{VCO}) \end{aligned} \quad (2.7)$$

Fig. 2.9 **a** System diagram of the proposed fractional-N PLL with quantization noise cancellation technique;
b PFD circuit



To completely remove the quantization noise caused by the $\Sigma\Delta$ modulator, the integrated charge should be constant and equal to zero. Therefore, we can arrive at the following equations:

$$\alpha = 1 - \varepsilon \quad (2.8)$$

$$T_x - 2T_{vco} + t_d = 0 \quad (2.9)$$

Fig. 2.10 Pulse control module used to generate PWM signal

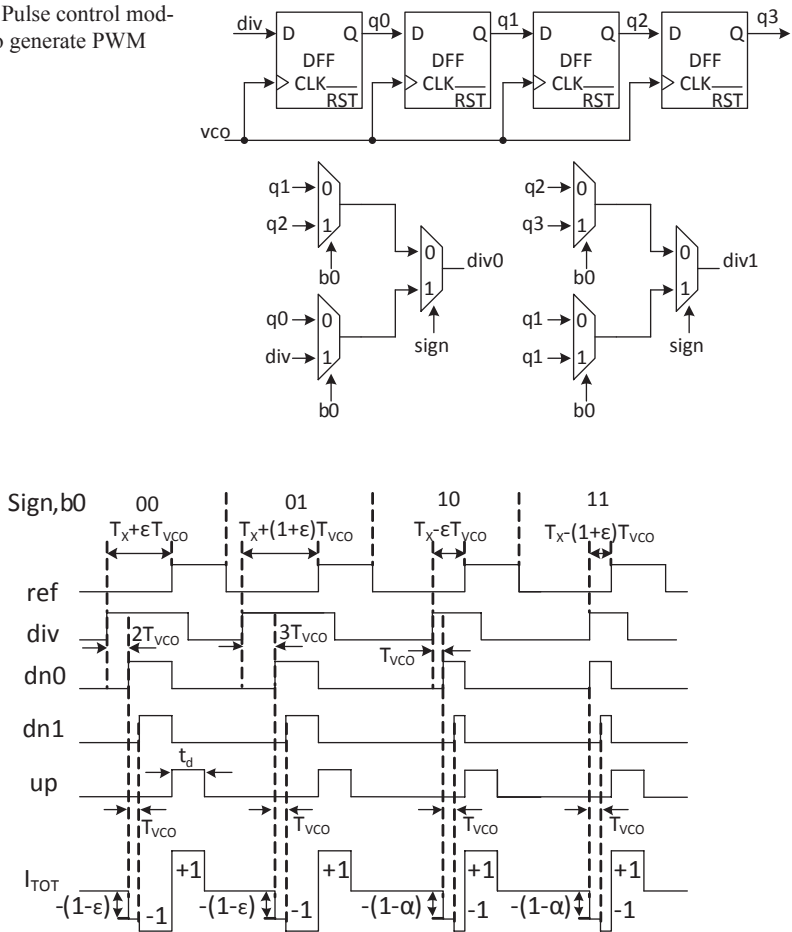


Fig. 2.11 Waveform example for phase error compensation

where α is defined in Fig. 2.11, T_x is the intrinsic delay in the PLL loop, and t_d is the delay introduced in the reset path of up control flip-flop. Typically, we can choose t_d slightly larger than twice the VCO period to allow correct compensation. With the proposed noise cancellation technique, the noise contribution from $\Sigma\Delta$ modulator can be eliminated under ideal condition.

2.4 Conclusion

This chapter reviewed several quantization noise reduction techniques for $\Sigma\Delta$ modulator-based fractional-N PLL. Analysis of quantization noise and nonlinearity effect is given for MASH1-1, MASH1-1-1, and two SSMF $\Sigma\Delta$ modulators. Several

quantization noise reduction techniques have been discussed and it shows that the most efficient way of reducing $\Sigma\Delta$ quantization noise is frequency doubling. A novel noise cancelling technique and its implementation for second-and third-order $\Sigma\Delta$ modulator has been proposed to compensate the phase error between $-2 \sim 2$ VCO period.

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