

Preface

This book covers unique design techniques for phase-locked-loop (PLL) frequency synthesizers, including quantization noise reduction, low power design methodology for dividers, and high-performance multi-phase clock generation techniques.

PLL is a critical building block for frequency synthesis in wired and wireless communication systems. This book first introduces fundamentals about fractional-N PLL design. It analyzes the quantization noise of $\Sigma\Delta$ modulator based fractional-N PLL. $\Sigma\Delta$ modulation is a commonly used technique for fractional spur reduction. However, quantization noise caused by $\Sigma\Delta$ modulator degrades the phase noise performance at the PLL output. The noise degradation becomes worse when the loop is nonlinear. In this book, noise reduction and cancellation techniques are presented to solve the problems associated with noise degradation due to $\Sigma\Delta$ modulation. Also analyzed is the impact of charge pump nonlinearity on phase noise performance. System-level behavioral model is developed for the analysis of charge pump nonlinearity.

For low power PLL design, a wideband integer-N PLL with power optimized dividers is presented. An intuitive, yet efficient power optimization methodology is introduced for optimizing divider power consumptions using both bipolar and CMOS technologies.

Quadrature signals are needed in image-rejection transceivers. This book presents the analytical results and design details of two quadrature voltage-controlled oscillators (QVCO) with capacitive-coupling technique. Capacitors are used to couple the two voltage-controlled oscillator (VCO) cores. The proposed capacitive-coupling QVCO (CC-QVCO) architecture has the advantage of low phase noise performance and it is free from the bi-modal oscillation, which causes the quadrature phase ambiguity. Unlike conventional quadrature-coupling scheme using active devices, CC-QVCO utilizes noiseless capacitors to form QVCO, allowing phase-shifted coupling signals that lead to reduced phase noise.

A differential Colpitts CC-QVCO with enhanced swing is proposed to offer excellent phase noise performance under low power supply. It achieves lower phase noise than its single-phase counterpart. Optimized capacitive coupling combined with source inductive enhance-swing technique achieves low power and low phase noise simultaneously. Due to the inherent phase shift in the proposed quadrature-coupling path, the problem associated with $\pm 90^\circ$ phase ambiguity between the quadrature outputs is eliminated.

Capacitive-coupling technique can also be applied to multi-phase clock generation for improved phase noise performance. A QVCO prototype using classic NMOS cross-coupled VCO with current tail is implemented to demonstrate the advantages of capacitive-coupling comparing to other coupling techniques. The problem of phase ambiguity for this QVCO is also avoided by the intrinsic leading phase shifting through the capacitive coupling paths. Circuit implementations and measurement results of this CC-QVCO and another class-C mode top-series QVCO (TS-QVCO) used as a comparison are presented with details. This book is organized as follows:

Chapter 1 introduces several critical techniques for high performance PLL designs.

Chapter 2 explores several quantization reduction techniques for fractional-N PLL designs.

Chapter 3 describes a wideband PLL with power optimization methodology for low power divider designs.

Chapter 4 presents a capacitive-coupling technique for multi-phase clock generation using NMOS VCO with current tail. The proposed structure demonstrates excellent phase noise and accurate quadrature phases over a wide frequency range.

Chapter 5 discusses the design of a capacitive-coupling quadrature VCO with emphasis on phase noise reduction and elimination of phase ambiguity under a super low supply voltage.

Chapter 6 provides a summary for this book.

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Multi-Phase High-Performance Oscillators

Zhao, F.; Dai, F.F.

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