Chapter 2
CMOS at Millimeter Wave Frequencies

In the past, mm-wave integrated circuits were always designed in high-performance RF technologies due to the limited performance of the standard CMOS transistors [Hun88]. However, the continuous scaling of the CMOS process toward gate lengths of several tens of nanometers has resulted in a considerable increase of the MOSFET performance at mm-wave frequencies. Despite this evolution of the devices, the performance of a single MOSFET is still limited, so advanced analog and RF design techniques are required. Low available gain of the nMOS is one of the most restrictive properties which has a severe impact on all other design parameters. Another big problem is the parasitic Miller capacitance in the MOSFET which results in potentially unstable behavior. These problems, together with the techniques to analyze them and design techniques to solve them, are discussed in this chapter.

2.1 Properties of MOS Transistors at Millimeter Wave Frequencies

In this first section, a brief overview of the most important parameters of the nMOS transistor at mm-wave frequencies is given. The basic techniques to analyze and quantify these parameters are also discussed.

2.1.1 High Frequency Gain

The latest nanometer-scale CMOS transistors, with a maximum frequency of current gain (f_t) and maximum frequency of power gain (f_{max}) exceeding 100 GHz, enable the implementation of fully integrated CMOS mm-wave frontends. To understand what the limitations of the transistor are at these high frequencies, the expressions for f_t and f_{max}, respectively, given in 2.1 and 2.2 are analyzed more in detail [Nik07]. Equation 2.1 shows that f_t is only dependent on technology parameters, and its dependency on the transistor layout is rather limited. f_{max} on the contrary, is highly dependent on the parasitic resistors of the transistor terminals and the channel.

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These parameters, and more in particular the gate resistance, are determined by the transistor layout

$$f_t \approx \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})} \tag{2.1}$$

$$f_{max} \approx \frac{f_t}{2 \cdot \sqrt{R_g \cdot (g_m \cdot \frac{C_{gd}}{(C_{gs}+C_{gd})}) + (R_g + r_{ch} + R_s) \cdot g_{ds}}}. \tag{2.2}$$

In Fig. 2.1a and b, two layouts are shown of a 65nm nMOS transistor. To make a fair comparison between the two layouts, the total width is fixed at 16 µm. In the first layout, four fingers, each with a fingerwidth of 4 µm are used. The second layout has 25 fingers, resulting in a fingerwidth of 640 nm. In both cases, the two major parasitic resistance contributions to the gate resistance are indicated: the poly-silicon gate resistance, and the metal distribution resistance. Due to the large fingerwidth, the poly-silicon gate resistance is determining the overall gate resistance in the first layout. In the second layout, the increase of the number of fingers results in an increase of the distribution line, and thus in an increase of the metal distribution resistance.

The effect of the fingerwidth on the gain curves of a 65nm nMOS transistor is shown in Fig. 2.2a and b. Figure 2.2a shows the gain curves for a fingerwidth of 4 µm and Fig. 2.2b shows the gain curves for a fingerwidth of 640 nm. The frequency at which the current gain (H_{21}) is 0 dB is denoted as f_t. The frequency at which the maximum available power gain (MAG) crosses the 0 dB line is denoted as $f_{\max}$. Above $f_{\max}$, no power gain is available so the transistor turns into a passive component above f_{max}. For this reason, $f_{\max}$, rather than f_t, is determining the limits of active mm-wave circuit design.

The dependency of f_t and f_{max} on the fingerwidth is shown in Fig. 2.3a for a fixed total width. As expected, for larger fingerwidths, f_{max} increases when the fingerwidth decreases. As long as the poly-silicon gate resistance determines the largest part of the total gate resistance, f_{max} will increase with decreasing fingerwidth. When the number of fingers is increased even more, the decrease in poly-resistance will be less than the increase of the metal distribution resistance, leading to a decreasing f_{max}. This trade-off between the poly-resistance and the metal distribution resistance results in an optimal fingerwidth of approximately 1 µm, leading to a peak f_{max} of 215 GHz for this 65 nm nMOS transistor.

Equations 2.1 and 2.2 also show that the transistor transconductance (g_m) has an impact on f_t and f_{max}. f_t increases with g_m, but f_{max} shows an optimum as g_m also appears in the denominator of the equation. As g_m is directly related to the bias current of the transistor and the bias current gives more information in terms of power consumption, reliability, and efficiency, f_t and f_{max} are typically expressed as a function of the bias current density (bias current divided by the transistor width) rather than the transistor transconductance. Figure 2.3b shows the impact of the bias conditions on f_t and f_{max}. The bias current density for peak f_{max} is approximately 0.8 mA/µm, however, f_{max} does not vary much within a bias range from 0.5 mA/µm up to 1.2 mA/µm. To limit the DC power consumption, and also the overall efficiency of the mm-wave system, bias currents are chosen as low as possible within this range.

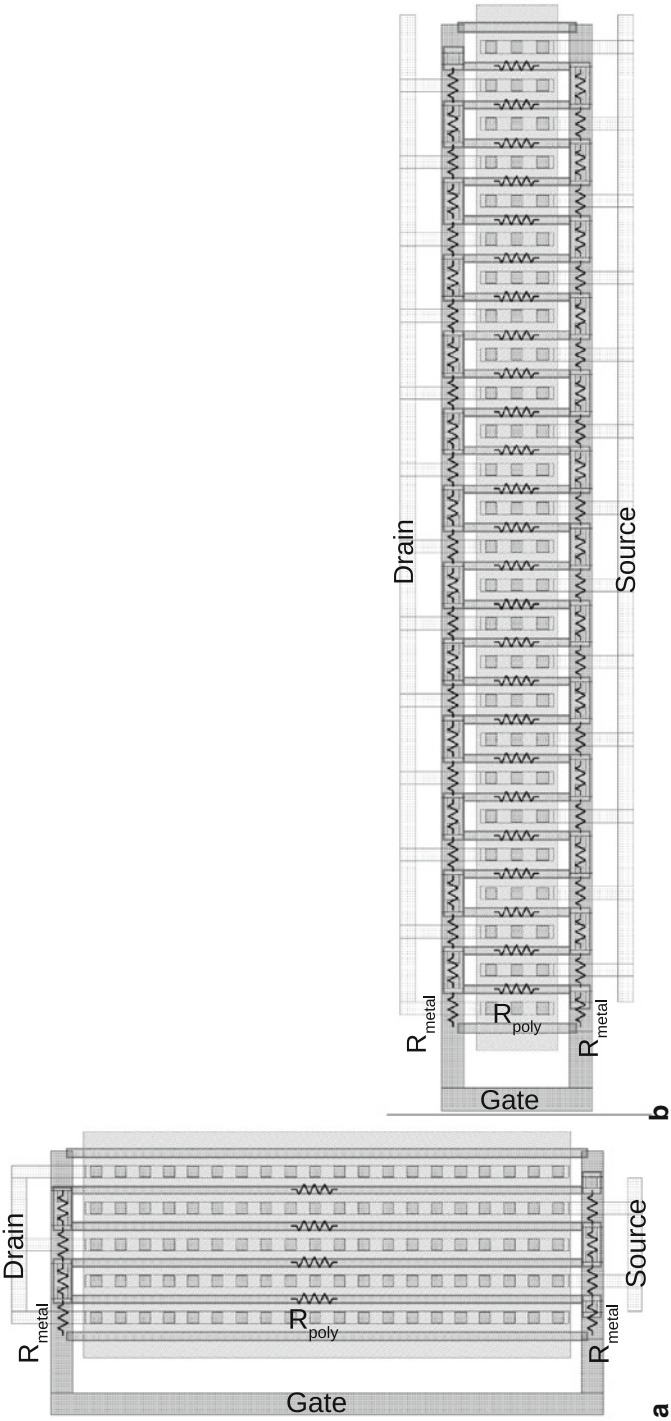

Fig. 2.1 Indication of the gate resistance which is a combination of the metal interconnect and the poly resistance for a 65 nm, 16 µm nMOS transistor with 4 fingers (**a**) and 25 fingers (**b**)

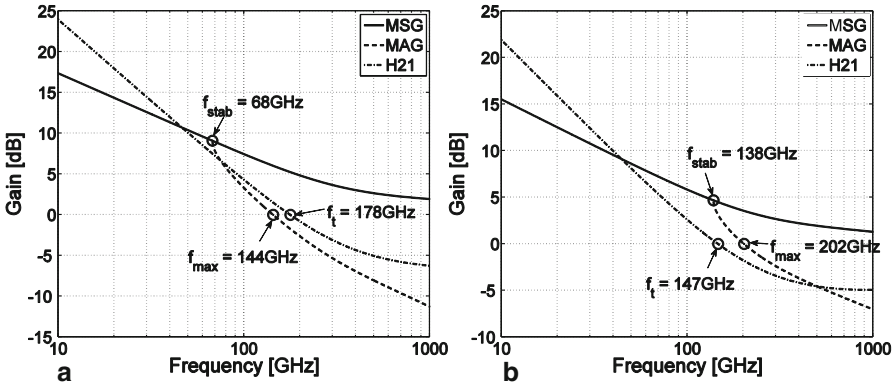

Fig. 2.2 Maximum stable gain, maximum available gain and current gain of a 16 µm, 65 nm nMOS transistor with 4 fingers (**a**) and 25 fingers (**b**)

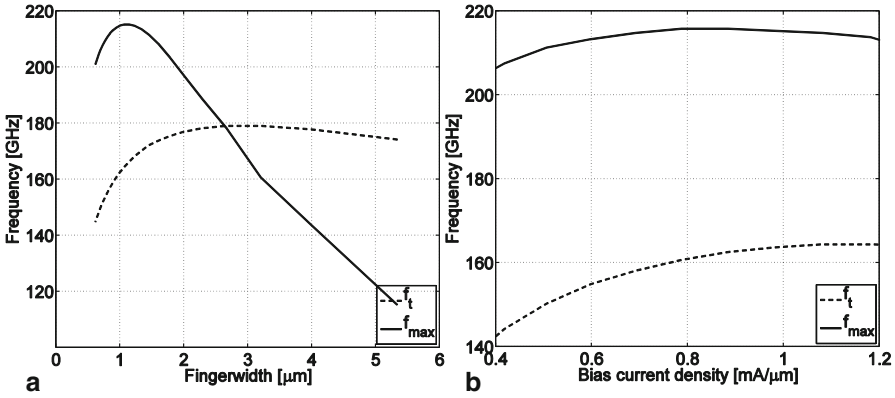

Fig. 2.3 f_t and f_{max} for different fingerwidths (**a**) and bias current densities (**b**) of a 65 nm nMOS transistor with a total width of 16 µm

2.1.2 Stability Considerations

In the previous section, mainly the impact of different transistor parameters and layout on the power gain, or alternatively, f_{max} was discussed. However, next to the limitations on the gain, the MOS transistor also suffers from potential unstable behavior leading to unwanted oscillations. To understand this stability behavior at mm-wave frequencies, the impact of the different parasitic components will be investigated more in detail. In this investigation, the Rollett stability factor (K) plays an important role. Unconditional stability of a two-port network is ensured when the following conditions are satisfied [Gon96]:

$$K > 1 \tag{2.3}$$

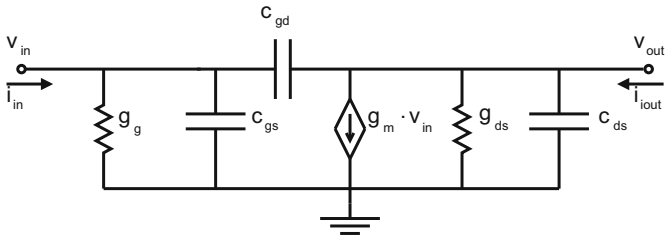

Fig. 2.4 Small signal schematic of an nMOS transistor

Table 2.1 Component and signal description of the small signal equivalent schematic of an nMOS transistor

Variable	Description
v_{out}	Output voltage of the nMOS transistor
v_{in}	Input voltage of the nMOS transistor
g_g	Parasitic gate conductance of the nMOS transistor
g_m	Transconductance of the nMOS transistor
c_{gd}	Parasitic gate-drain capacitance of the nMOS transistor
c_{gs}	Parasitic gate-source capacitance of the nMOS transistor
g_{ds}	Drain-source conductance of the nMOS transistor
c_{ds}	Drain-source capacitance of the nMOS transistor

$$|\Delta_S| < 1. \tag{2.4}$$

Or alternatively [Pla93]:

$$K > 1 \tag{2.5}$$

$$Re\{y_{11}\} > 0 \tag{2.6}$$

$$Re\{y_{22}\} > 0. \tag{2.7}$$

The latter three equations will be used in the stability analysis as these are easy to evaluate based on the y-parameters of the small signal equivalent circuit of the nMOS transistor (Fig. 2.4); Table 2.1.

Notice that in the schematic, a shunt representation of the gate impedance is used to reduce the complexity of the y-parameter calculations. Accordingly, y-parameters of this two-port network are given in Eqs. 2.8–2.11 [Den10]:

$$y_{11} = g_g + s \cdot c_{gs} + s \cdot c_{gd} \tag{2.8}$$

$$y_{12} = -s \cdot c_{gd} \tag{2.9}$$

$$y_{21} = gm - s \cdot c_{gd} \tag{2.10}$$

$$y_{22} = g_{ds} + s \cdot c_{ds} + s \cdot c_{gd}. \tag{2.11}$$

The K-factor can be expressed in terms of these y-parameters and after substitution, K can be expressed in terms of the circuit components of the small signal representation of the nMOS transistor (Eq. 2.13):

$$K = \frac{2 \cdot \Re\{y_{11}\} \cdot \Re\{y_{22}\} - \Re\{y_{12} \cdot y_{21}\}}{|y_{12} \cdot y_{21}|} \tag{2.12}$$

$$= \frac{2 \cdot g_g \cdot g_{ds} + \omega^2 c_{gd}^2}{\omega \cdot c_{gd} \cdot \sqrt{\omega^2 \cdot c_{gd}^2 + g_m^2}}. \tag{2.13}$$

Under the assumption that conditions 2.6 and 2.7 are fulfilled, which is typically the case for an nMOS transistor configured as common-source amplifier, the frequency in the millimeter wave frequency band at which K equals 1 indicates the boundary between the unconditionally and conditionally stable region. This point is denoted as the stability break point (f_{stab}). At frequencies below f_{stab}, K is smaller than 1 and the transistor is conditionally stable. In this case, the source and load impedance will determine the occurrence of oscillation. The figure of merit used to indicate the power gain of the transistor in the conditionally stable region is the maximum stable gain (MSG). Equation 2.14 gives an expression for the MSG as a function of the y-parameters. Substitution of Eqs. 2.9 and 2.10 into this equation yields an expression in terms of the transistor circuit components (Eq. 2.15). Notice that c_{gd} is an important parameter in this gain expression. A more detailed analysis of the impact of c_{gd} on the transistor gain and stability performance will be discussed in Sect. 2.2. At frequencies above f_{stab}, the transistor is unconditionally stable and oscillation will never occur without the addition of an external feedback circuit. In the unconditionally stable region, the power gain is limited by the maximum available gain (MAG). Equation 2.16 gives the expression for the maximum available gain. As K is a part of this equation, the transistor parameters determining K will also determine the MAG:

$$MSG = \frac{|y_{21}|}{|y_{12}|} \tag{2.14}$$

$$= \frac{|gm - s \cdot c_{gd}|}{|-s \cdot c_{gd}|} \tag{2.15}$$

$$MAG = MSG \cdot \left(K - \sqrt{K^2 - 1}\right). \tag{2.16}$$

As already discussed, the gate resistance has a large impact on the $f_{\max}$ of the transistor. As $f_{\max}$ is directly related to the MAG (i.e., MAG($f_{\max}$) = 0 dB), the

resistance will also influence the MAG. Figure 2.2a and b shows that when the gate resistance is decreased, the MAG (and accordingly f_{max}) will increase. Also notice that f_{stab} shifts to higher frequencies, which increases the frequency region of potential instability. The destabilization of the transistor due to the decrease of the gate resistance can also be seen from the expression of K. To understand this, the shunt representation of the transistor input impedance has to be rewritten in terms of the series gate resistance. A first order approximation of the series gate resistance is given in Eq. 2.18. For high frequencies, the term $\omega^2 \cdot c_{gs}^2$ in the denominator becomes dominant and the expression can be approximated by Eq. 2.19. Substitution of this equation in Eq. 2.13 shows that the decrease of the gate resistance results in a decrease of K, which confirms the destabilization of the transistor:

$$R_g \approx \frac{\frac{1}{g_g}}{1 + \omega^2 \cdot c_{gs}^2 \cdot \frac{1}{g_g^2}} \tag{2.17}$$

$$= \frac{g_g}{g_g^2 + \omega^2 \cdot c_{gs}^2} \tag{2.18}$$

$$\approx \frac{g_g}{\omega^2 \cdot c_{gs}^2} \quad for \ \ \omega \gg 0. \tag{2.19}$$

2.2 Capacitive Neutralization

In previous sections, it became clear that decreasing the gate resistance leads to maximization of the power gain. Unfortunately, minimizing the gate resistance also results in a reduction of the K-factor and an increase of f_{stab}, leading to a potentially unstable behavior over a wider frequency range. To improve the stability without compromising the gain of the nMOS transistor, the internal feedback in the transistor, caused by the parasitic gate-drain capacitor, has to be reduced. An elegant technique to accomplish this is to neutralize c_{gd} in a differential pair (Fig. 2.5a).

The impact on the MSG, MAG, f_{stab}, and f_{max} as a result from subsequently decreasing the gate resistance and applying capacitive neutralization in a differential pair is shown in Fig. 2.5b. In this graph, the MSG/MAG curves of a 65 nm, 16 µm transistor are plotted for a fingerwidth of 4 µm and the optimal fingerwidth of 1 µm. Also, the MSG/MAG curve of a neutralized differential pair with nMOS transistors with a fingerwidth of 1 µm is shown. As already mentioned, decreasing the fingerwidth to the optimal value yields an increase of the MAG and f_{max}. f_{stab} is also increased, leading to destabilization over a wider frequency range. The addition of the cross-coupled capacitor C_N compensates for this destabilization and even improves the stability compared to the initial situation with a fingerwidth of 4 µm. The MAG is increased and f_{stab} is also shifted to lower frequencies which results in an increase of the unconditionally stable region without decreasing f_{max}. Unfortunately, the addition of these cross-coupled capacitors also has an impact on the common mode behavior of the differential amplifier. An elaborate stability analysis, both for common mode and differential mode [Def14b], is discussed in this section.

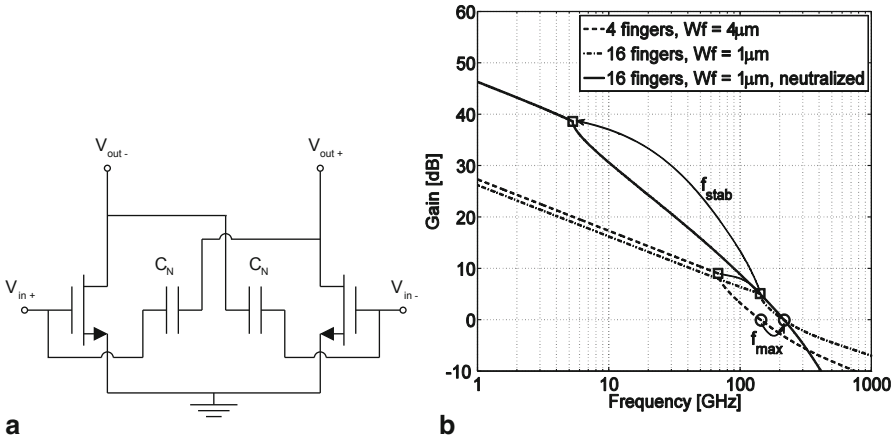

Fig. 2.5 Pseudo differential pair with capacitive neutralization (**a**) and impact of fingerwidth and neutralization on MSG, MAG, f_{stab} and f_{max} (**b**)

2.2.1 Differential Mode Stability

In this section, the small signal differential stability behavior of a differential pair with capacitive neutralization is analyzed. The 45 nm nMOS transistors in the differential pair in which the capacitive neutralization technique is applied have a width of 40 µm and have 40 fingers. Ideally, perfect neutralization leads to an unconditionally stable differential pair over a wide frequency band, down to DC. The necessary and sufficient conditions for unconditional stability were already given in Eqs. 2.3 and 2.4 or alternatively Eqs. 2.3, 2.6, and 2.7.

In the first step of the analysis, the impact of the neutralization capacitor (C_N) on the Rollet stability factor (K), $\Re\{y_{11}\}$, and $\Re\{y_{22}\}$ or alternatively Δ_S in differential mode is discussed. The y-parameters of the small signal equivalent circuit schematic of the neutralized differential pair (Fig. 2.6) are given in Eqs. 2.20–2.23:

$$y_{11} = g_g + s \cdot c_{gs} + s \cdot \left(c_{gd} + C_N\right) \tag{2.20}$$

$$y_{12} = -s \cdot \left(c_{gd} - C_N\right) \tag{2.21}$$

$$y_{21} = gm - s \cdot \left(c_{gd} - C_N\right) \tag{2.22}$$

$$y_{22} = g_{ds} + s \cdot c_{ds} + s \cdot \left(c_{gd} + C_N\right). \tag{2.23}$$

Substitution of these equations in Eq. 2.12 leads to expression 2.24. When C_N approximates c_{gd}, K goes to infinity

$$K = \frac{2 \cdot g_g \cdot g_{ds} + \omega^2 \cdot \left(c_{gd} - C_N\right)^2}{\omega \cdot \left|c_{gd} - C_N\right| \cdot \sqrt{\omega^2 \cdot \left(c_{gd} - C_N\right)^2 + g_m^2}}. \tag{2.24}$$

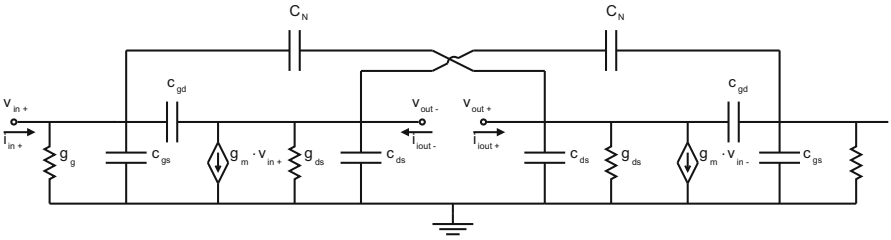

Fig. 2.6 Small signal schematic of a neutralized nMOS differential pair in differential mode

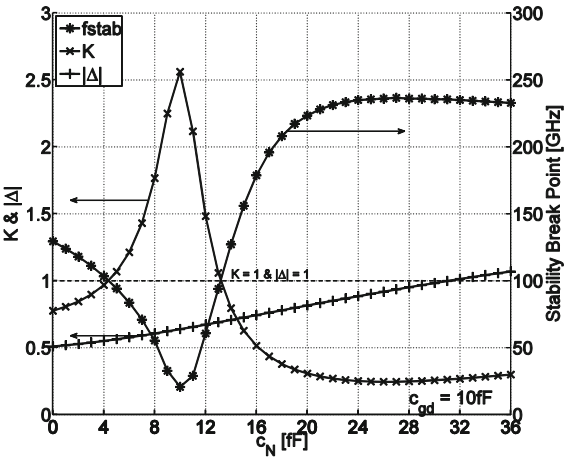

Fig. 2.7 Simulated K, Δ_S and stability break point as a function of C_N in differential mode. When c_{gd} equals C_N K reaches its maximum and the stability break point frequency is minimized

Solving the equation for K = 1 results in the interval edges of the values of C_N for which unconditional stability is guaranteed, under the assumption that condition 2.4 is satisfied. An expression for these extreme values of C_N is given in Eq. 2.25

$$C_N = c_{gd} \pm \frac{2}{\omega} \cdot \frac{g_g \cdot g_{ds}}{\sqrt{g_m^2 - 4 \cdot g_g \cdot g_{ds}}}. \tag{2.25}$$

Figure 2.7 depicts the behavior of K and Δ_S as a function of C_N at 100 GHz. As predicted by Eq. 2.24, K peaks when C_N equals c_{gd} and is larger than 1 for values of C_N ranging from approximately 4.5 fF up to 13 fF. For these values of C_N, $|\Delta_S|$ is also smaller than 1, so unconditional stability is guaranteed at 100 GHz. The presented results are obtained from a small signal scattering parameter (s-parameter) simulation of the differential pair. The nMOS transistor frequency behavior is described by the PSP model.

Although both conditions for unconditional stability are met for C_N ranging from approximately 4.5 fF up to 13 fF, a better understanding of the stability can be achieved by analyzing the poles of the system as a function of C_N. Of course, the overall differential mode transfer function and thus also the poles and zeros of a differential amplifier are influenced by the source and load impedances. Figure 2.8 shows

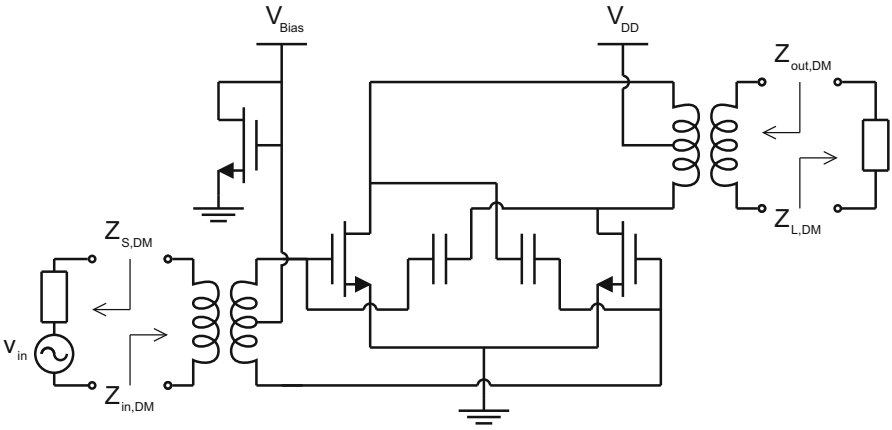

Fig. 2.8 Schematic representation of the differential source and input impedance as well as the differential load and output impedance

the schematic of a complete amplifier stage with its matching networks, source and load impedance in differential mode. Integrated transformers are used in the matching networks to perform the impedance transformation. Both input and output matching networks are tuned to a conjugate match at 100 GHz under perfect neutralization i.e., $C_N = c_{gd}$.

Jugo et al. [Jug01] proved that all the closed loop transfer functions defined from a linear system, share the same denominator. To analyze the poles of the closed loop transfer function, a transfer function $H_{DM}(s)$ is introduced which is described as the input admittance of the system (Eq. 2.26). The analysis of the poles of this transfer function will give an accurate description of the stability behavior of the differential pair. Figure 2.9 explains how v_{in}, i_{in}, and load and source impedance are defined. $Z_{DP,DM}$ represents the differential impedance between input and output of the differential pair, including matching networks. The source impedance is the output impedance of the previous stage of the amplifier which can be represented by $R_{S,DM}$ and $C_{S,DM}$. The load impedance is the input impedance of the next differential pair, represented by $R_{L,DM}$ and $C_{L,DM}$

$$\begin{aligned} H_{DM}(s) &= \frac{i_{in}}{v_{in}} \\ &= \frac{1 + s \cdot C_{S,DM} \cdot Z_{TF,DM}(s)}{Z_{TF,DM}(s) + R_{S,DM} \cdot \left(1 + s \cdot C_{S,DM} \cdot Z_{TF,DM}(s)\right)} \end{aligned} \tag{2.26}$$

where,

$$Z_{TF,DM}(s) = Z_{DP,DM}(s) + R_{L,DM} + \frac{1}{s \cdot C_{L,DM}}.$$

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