

# Preface

## Overview

A video signal, which is composed of a sequence of still frames of pixels, contains significant amount of redundant information in spatial and temporal domain. Elimination of this redundant information is achieved by efficient video compression methods. To provide interoperability between video encoder and decoder, MPEG-X (1, 2 and 4) and H.26X (261, 262, 263, 264 and 265) video coding standards have been defined by the ITU-G and VCEG. To reduce the temporal redundancy between adjacent frames, the majority of the existing coding standards have adopted Block Matching Algorithms (BMA) for Motion Estimation (ME). BMA calculates motion vector for an entire block of pixels instead of individual pixels. The same motion vector is applicable to all the pixels in the block. This reduces the computational requirement and also results in a more accurate motion vector since the objects are typically a cluster of pixels.

In general, out of all the components of a video encoder, the ME module consumes the major share of overall power. A very simple arithmetic computation is required for ME. However, frequent memory access associated with ME affects the overall speed of operation and the power consumption. The present work has therefore focused on design and development of VLSI architectures for several fast ME architectures characterized by high processing speed, low power, and low area making them suitable for portable video application devices that are typically operated by battery power and involve real time operation.

## Organization and Features

This book primarily focuses on low-power VLSI implementation of ME architectures and efficient data reuse technique along with other techniques that have been used to make a high performance ME architecture. In addition, the concept of

scalable video coding based on in-band motion compensated temporal filtering has also been presented.

Chapter 1 gives a brief introduction to the concept of video compression and motion estimation. Chapter 2 provides the background of ME and different fast search techniques for motion estimation and a brief survey of the literature related to the scalable video coding. Chapter 3 explains the design of VLSI architecture for realizing Fast Three Step Search algorithm (FTSS). Chapter 4 explains the implementation of VLSI architecture for Successive Elimination algorithm (SEA). Chapter 5 provides details of fast ME based on a combination of Diamond Search and 1-bit transformation and its architecture. Chapter 6 introduces a new two stage fast algorithm for Variable Block Size Motion Estimation (VBSME) based on pixel truncation and its low power architecture. Chapter 7 gives the fundamentals of Scalable Video Coding based on In-band Motion Compensated Temporal Filtering (IB-MCTF). Finally, Chap. 8 presents a few suggestions for extensions of the present work.

Programs have been developed in Matlab and Verilog to implement the research ideas discussed in depth from Chap. 3 through Chap. 7. Some of these programs have been provided in the two appendices of this book for the benefit of the reader.

## **Audience**

This book presents material that is appropriate for courses at the senior undergraduate level and graduate level in the areas of Video processing and VLSI architectures. It is also suitable for research students who are working on design of VLSI architectures for Video processing applications. Practicing engineers in the area of hardware implementation of video CODEC will also find the book to be immensely useful. Basic familiarity with logic design and hardware description languages is considered adequate to follow the material presented in this book.

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