

Structural Characterization of Layers for Advanced Non-volatile Memories

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Abstract Non-volatile memory cells are the devices with the most aggressive scaling on the market. For this reason the accurate characterization of their layer stacks is of great importance. We present a review of our recent work on a large variety of such stacks, for charge-trap and resistive memories, which have been characterized structurally with Transmission Electron Microscopy and Conducting Atomic Force Microscopy; we discuss the features of their structure on their function as memory elements.

1 Introduction

The technology for creating advanced memory cells plays a central role in the miniaturisation of electronic devices; new process nodes usually enter production with the manufacturing of memory cells. At this moment the 16 nm memory cells are in production. The recent slowdown of the transistor scaling has partially been compensated by the improvements in memory performance and by their integration on various chips. There is a fierce competition between memory manufacturers which is governed by their ability to introduce new processes on time that are improving the speed, the reliability and the density of the memory cells, while keeping the production and development cost at a low level.

Non-volatile memories are at the centre of this technology and during the last years Solid State Disks have become mainstream computer components. Flash memories have dominated this vast field for a long time, and because their scaling

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has also been slowed down, the interest of the scientific community is shifting increasingly towards other technologies, such as the Resistive Memories. The resistive memory is currently the most promising non-volatile memory technology, as it offers low-power, reliable and denser memory cells with the option to exploit not only single level cell storage (storing one bit of information) but also multilevel cells, a feature that multiplies the effective information density storage.

From a Materials Science point of view, advanced non-volatile memories consist of nanometer scale stacks that can be processed with a large number of methods, in order to achieve the best balance of their electrical properties. Insulating, semiconducting and metallic properties are pushed to their limits while there is a constant search for new materials and device geometries. Of course, the introduction of new materials and process is not easily welcomed by the manufacturers, as it may lower the production yield and therefore increase significantly the cost of the devices. They prefer to work with “CMOS compatible” materials and processes, i.e. materials that they know better, such as Si and its compounds (Silicon Dioxide, Silicon Nitride) that can be integrated in the existing processes and that will not cause cross-contamination concerns in their ultra-clean production environments.

Whatever the approach for creating non-volatile memories, structural characterization is a critical part of the research effort that is required for their development. Because of the complicated nature of their functional properties (retention time, write/erase speed etc.), the structural and morphological data of these devices must be combined with other materials’ properties and esp. the electrical, in order to understand their operation.

2 Flash Memories

Flash memories consist of at least 3 layers that are deposited on a semiconducting substrate (usually Si) covered by an electrode (or gate) where the write/erase voltage (VG) is applied (Fig. 1). In these 3 layers, the middle layer is the charge storage layer (floating gate or charge trap layer), where the charge is being stored and the other two layers are the insulating layers that block the transfer of electrons to and from the middle layer. The insulating layer next to the substrate (called “tunneling” layer) is thin enough to allow the control of the tunneling of the charges to the substrate, i.e. the charging and discharging of the charge storage layer; the tunneling layer is usually SiO₂ (thermally grown on the Si) because of the unique stability of this material, a crucial property for this position in the stack. The second insulating layer, the “blocking” or “control” oxide, has also very critical properties for the operation of the memory cell, as this is the medium through which the current may flow to the gate electrode. The device operates with the application of a voltage to the top electrode; charge is then injected from the substrate into the charge storage layer. The presence of charge near the Si substrate affects its local conductivity; if we replace the gate stack of a Field Effect Transistor (FET) with this stack, we have a transistor that can also store a bit permanently (see Fig. 1); it will

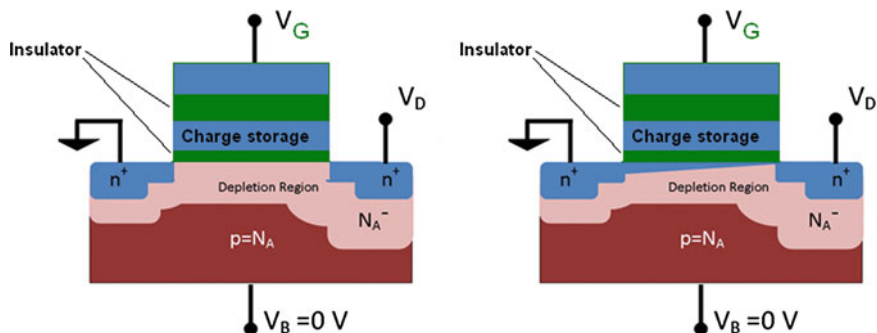


Fig. 1 The geometry of a Flash memory: *Blue* are the conducting areas, *green* are the insulators; on the right sketch there is charge stored near the channel so it is now conducting

not be erased until a voltage with an opposite sign is applied on the electrode. Until then, the charges will be stored there for a very long time (long “retention time”).

If the charge storage layer is composed of a conducting material, then it is called “floating gate”; if it is an insulator, then it is called “charge-trap layer”. The composition, the structure, the morphology, the crystallinity of the charge storage layer and the control layer have been an area of intensive research during the last few years, not only because we want to improve them for further miniaturization, but also because they can be engineered in order to tune the performance and the electrical characteristics of the memory cell, i.e. the amount of charge stored, the leakage currents, the charge retention time, the write/erase speed, its endurance etc.

We have worked on a large variety of materials and processes for the control and the charge storage layers. Because of the small volume of the layers, their structural characterization can be done by a limited number of techniques, with the TEM (Transmission Electron Microscopy) standing out of the rest. Of course, XRR (X-Ray Reflectivity), XPS (X-ray Photoelectron Spectroscopy), Grazing Incidence X-Ray Diffraction (GIXRD) provide also very important information; moreover they probe a much larger volume of the material than TEM.

The layers in our study are usually grown on full sheet wafers and are usually processed in relatively high temperatures (i.e. more than 200 °C), so the TEM samples can be thinned down to electron transparency by conventional means, that is, mechanical thinning followed by Ar ion milling at room temperature, without any effect on their structure. TEM of the layers was performed at plan view and cross sectional geometries with a Philips CM 20 HRTEM (High Resolution TEM) with a LaB₆ filament, equipped with an EDS (Energy Dispersive X-ray Spectroscopy) system and a GIF (Gatan Imaging Filter); the instrument is located at NCSR Demokritos. TEM has been able to provide the deeper inside view needed in this work and to resolve many open issues. Thickness, roughness, composition, intermixing of layers, defects (implantation damage etc.) and crystallite size, being the most critical, as these can affect seriously the electrical properties.

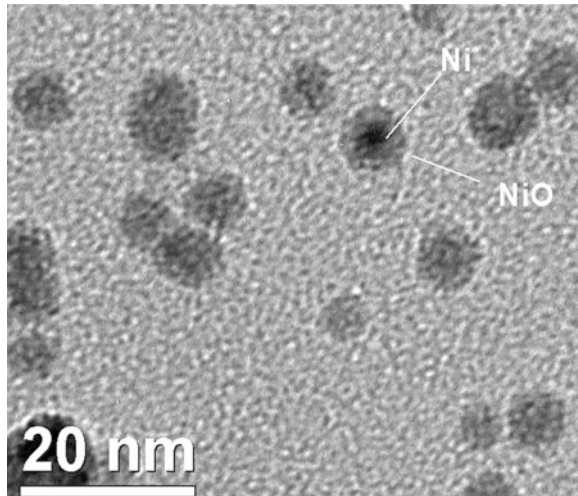
To overcome the problem of scaling of flash memories and to decrease the thickness of the tunneling oxide we worked on nanoparticle memories, where the charge storage layer (floating gate) is replaced by separate nanoparticles that are not in electric contact with each other. The reasoning behind this was that with conventional floating gates (single layers), the charging/discharging occurs through a single spot at the tunneling oxide; the oxide's temperature increases dramatically there and therefore it gets easily damaged. As a consequence, the tunneling oxide needs to be relatively thick. By fractioning the single floating gate into many parts we were able to distribute the conductive paths in the tunneling oxide over a wide area, and therefore reduce damages there. We managed to reduce the tunneling oxide thickness in a reliable way, and therefore to lower also the memory cell's power consumption. To achieve this we worked on the deposition of a large variety of metallic nanoparticles by e-gun evaporation on SiO_2/Si and covered them with a control oxide (SiO_2 or HfO_2). With the help of plan view TEM we managed to find the right parameters to create isolated self-assembled nanoparticles of various metals with a range of sizes. We used Pt [1–6], Pd [7], Au [4, 6, 8–10]. The TEM cross sections confirmed that the particles were located after processing on the interface between the control and the tunneling oxide and that they were covered completely by the control oxide; the retention time measurements and the other electrical characteristics confirmed the low voltage operation of these memory stacks and they showed that 1 or 2 electrons were stored per particle.

In another effort to create nanoparticle memories we used an innovative nanoparticle source to deposit Ni particles with much more accurate sizes than before, because the particles in this source are self-assembled in a low-vacuum pre-chamber. TEM played a crucial role in calibrating the operation of the nanoparticle source and confirmed the excellent size distribution of the particles, their purity, and their random distribution after their deposition, while the electrical measurements demonstrated their charge trapping properties. For Fig. 2 we deposited Ni particles on a Carbon support film used for TEM observation in order to avoid the Si thinning process and the related artifacts. For this particular type of particles, there is an oxide layer forming on the surface as it is clear on the diffraction contrast that arises; in actual memory stacks, Ni particles are embedded into the control layer immediately after their deposition, without any exposure to air [11, 12].

Besides charge storage in metals we used also a semiconductor, Si for this purpose. Amorphous Si was deposited by LPCVD (Low Pressure Chemical Vapor Deposition) on SiO_2/Si and was then annealed and oxidized. Si nanocrystals with various sizes and orientations were therefore embedded between 2 SiO_2 layers. As the crystals were very close to each other we were unable to confirm that they were not in contact, as the electrical measurements were suggesting. Nevertheless, this approach showed good charge trapping properties and a CMOS compatible method to create memory stacks [13, 14].

Charge trapping memory structures that use an insulator Si_3N_4 for their charge storage layer are now used in a number of applications, one example being the V-NAND structure; this is a 3D memory, currently on the market, introduced in 2013 by Samsung.

Fig. 2 Ni Nanoparticles deposited with a nanoparticle source



In order to engineer the properties of such memory cells SONOS (Silicon/silicon diOxide/silicon Nitride/silicon diOxide/Silicon) structures were fabricated by depositing Si_3N_4 on SiO_2/Si , followed by Si, N and Ar implantation and then by wet oxidation (to form the control oxide). The TEM and electrical characterization showed that the control oxide grows thicker on the Si-implanted samples and that the deep traps created by the implantation process provide an interesting option for such memories [15].

The replacement of the SiO_2 at the control oxide by alumina was studied with the growth of MANOS (Metal/Alumina/silicon Nitride/silicon Oxide/Silicon) structures. Alumina offers an alternative oxide to SiO_2 , as it has larger band gap and permittivity.

Several processes for the optimization of these memories, see for example [16], were studied and especially those that affect the properties of the Alumina (Al_2O_3) layer. ALD (Atomic Layer Deposition) was used with trimethylaluminum (TMA) and water (or ozone) at 300 °C for the Al_2O_3 deposition; the structure was then annealed (PDA, Post Deposition Annealing) in nitrogen ambient. Without the PDA, Al_2O_3 is amorphous with very high leakage currents. PDA condensed the Al_2O_3 layer without any loss of mass, as confirmed by XRR and turned it into a polycrystalline material (see Fig. 3); its crystallites increase with the PDA temperature. There is an interfacial layer between Al_2O_3 and Si_3N_4 which is formed right after the ALD deposition that is present also after the PDA. The leakage currents of the Al_2O_3 layer after PDA are reduced significantly.

Ion implantation of the ALD alumina control layer by low energy N atoms was another way of optimizing the function of the MANOS memory stacks. Amorphous alumina was implanted and then a post implantation annealing was performed (see Fig. 4). It was found that the implantation retards the crystallization of alumina. XPS data indicates that at the implanted area, Aluminum oxynitride is formed. By

Fig. 3 MANOS stack after PDA

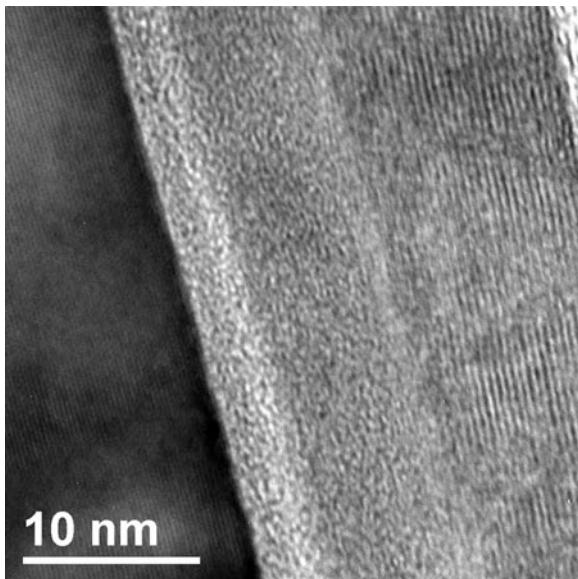
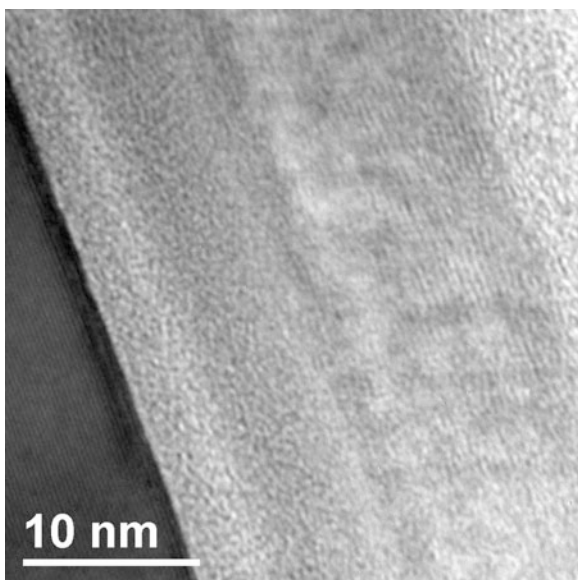


Fig. 4 HRTEM image of N ion beam implanted $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$ stack (at 1 keV, fluence 10^{16} ions/cm²), Al_2O_3 was grown in ALD with TMA and water before the implantation. PDA: 1050 °C for 15 min



selecting the right implantation and annealing conditions the retention time of the memory stacks was improved by 25 %, when compared to the non-implanted layers.

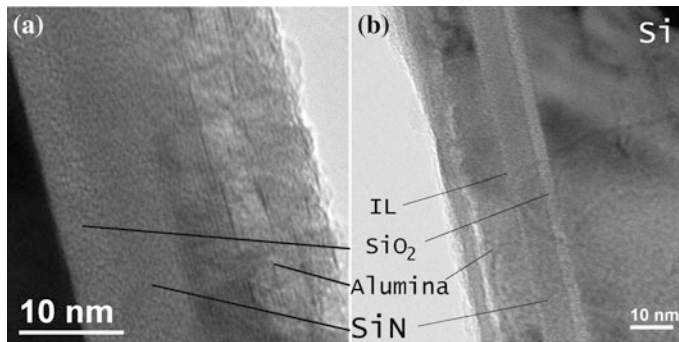


Fig. 5 **a** and **b** TEM images of N ion beam implanted $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$ stack; Al_2O_3 has been grown in ALD with TMA and ozone. PDA: 850 °C for 15 min

In Fig. 5 we can notice the interfacial layer (IL) between the alumina and the nitride layer as well as the large variation in the position of the implanted volume (the area with the smaller density inside the alumina); we can see also the presence of polycrystalline areas around it.

Besides Al_2O_3 , other high-k materials were deposited by ALD for the replacement of the SiO_2 of the control oxide over the $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$; these were ZrO_2 and HfO_2 [17–19]. An improved write/erase performance ($>3 \times 10^5$, in the 10/–11 V, 10 ms regime) was achieved by the appropriate selection of the ALD precursors; this meant that different deposition temperatures were used that affected the nature of the $\text{Si}_3\text{N}_4/\text{HfO}_2$ and the $\text{Si}_3\text{N}_4/\text{ZrO}_2$ interfaces.

3 Resistive Memories

Resistive memories have a much simpler structures than charge-trap memories. They usually consist of 2 electrodes that are separated by a sub-stoichiometric material, such as an oxide, e.g., TiO_{2-x} . When applying sufficiently high voltages the material enters a low resistivity state; when applying a voltage of the opposite polarity the material returns to a high resistivity state; such materials can switch between resistivity states thousands of times. The exact nature of this phenomenon is not yet clearly understood with a large part of the scientific community speculating that it is a result of filamentary vacancy migration.

This does not stop semiconductor companies from introducing the first Resistive RAMs (Random Access Memories) to the market, with very low power consumption. This technology has a huge potential for commercialization, also because its simplicity means relatively simple growth processes and patterning.

CAFM (Conducting Atomic Force Microscopy) is a technique that can simultaneously measure the surface structure of a layer and its relative resistivity. In these

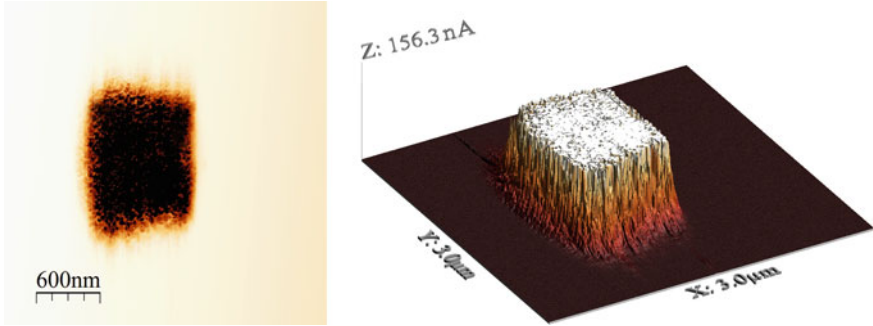


Fig. 6 C-AFM image (*left*) and its 3D representation (*right*) taken with a tip voltage of +4 V (READ). The rectangular area is the low resistivity area; it was scanned (before) with 7 V (WRITE)

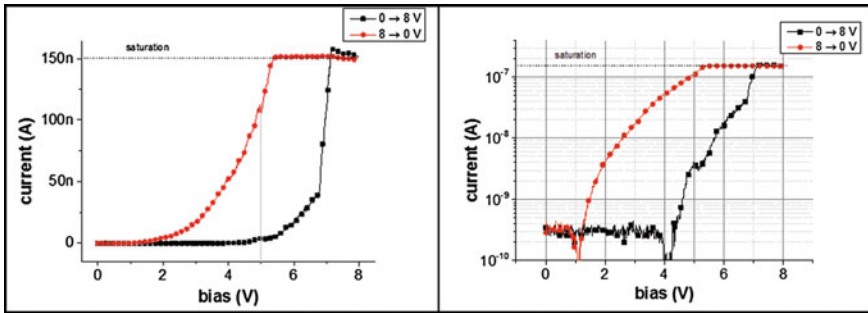


Fig. 7 I-V curve taken on the CAFM; Voltage is on the tip, the sample is grounded

materials it has been particularly helpful in the study of Ti (4 nm)/TiO_{2-x} (45 nm) layers that were sputtered on Au/SiO₂/Si.

CAFM was performed with a Veeco CP II AFM equipped with a DLPCA-200 low-noise linear amplifier by Femto. Bruker's SCM PIT tip (Pt/Ir coated, nominal radius of 35 nm, spring constant: 3 N/m), gave the best results among the 3 tips that we used.

In Fig. 6 we see a demonstration of a way to write and read a resistive memory with the CAFM. Note that the topographic images are not influenced by the write/erase process. Figure 7 shows an I-V curve recorded on certain spots, where the CAFM tip was resting; they demonstrate an on/off ratio of about 100; in our attempts to image with CAFM any of these isolated spots we were not able to locate them. When we "wrote" on several nearby spots we managed to image the low resistive area on the CAFM. This indicates that the low resistive area that is formed by the tip is smaller than the resolution of the CAFM measurements. Therefore we have a direct indication that in this particular material our tip writes an area smaller than ~ 50 nm. This can be critical for the scaling of memory cells.

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