

Chapter 2

Memristor: Models, Types, and Applications

2.1 The Missing Element History

The first concept and realization of memory resistor device was proposed by Widrow in 1960 [1]. It was named memistor and had three terminals. The resistance of this memistor was variable and could be controlled and sensed using the control (DC current) and sensing (AC current) terminals. The significant difference between the transistor and the memistor is that the memistor resistance is controlled by the instantaneous time integral of the control current, which is the accumulated charge passing through the memistor. However, the memistor was not linked to the fundamentals of circuit theory because it is an “ill-posed” element, a 3-terminal device is said to be well posed if it has sufficient information to predict the current and voltage associated with all the three terminals when the device is connected to an arbitrary external circuit [2]. Moreover, in 1968, through the Electromagnetic theory, Fano et al. listed that there are four fundamental circuit elements: resistor, capacitor, inductor, and an unknown element [3].

However, the first practical mathematical concept and realization was introduced by the father of nonlinear circuits, Prof. Leon Chua, in 1971 in his seminal paper [4]. It is well known that the four main fundamental circuit variables are current, i , voltage, V , charge, q , and flux, φ . For linear elements, $f(V, i) = 0$, $f(V, q) = 0$ where $i = dq/dt$, and $f(\varphi, i) = 0$ where $V = d\varphi/dt$, which represent the linear resistor ($v = iR$), the capacitor ($q = CV$), and the inductor ($\varphi = Li$), respectively. Chua predicted mathematically that there is a device representing the missing relation characterized by $g(\varphi, q) = 0$ which he named the memristor. Moreover, he presented an electromagnetic interpretation of the memristor characteristics [4]. Also Chua defined two types of memristors; charge-controlled and flux-controlled based on their memristance relation. They are called charge-controlled and flux-controlled memristor, when the memristance relation is a single-valued function of the charge

q or flux linkage φ , respectively. The voltage across a charge-controlled memristor is given by:

$$v(t) = M(q(t))i(t) \quad (2.1a)$$

$$M(q) = dq(q)/dq \quad (2.1b)$$

Similarly, the current of a flux-controlled memristor is given by:

$$i(t) = W(\varphi(t))v(t) \quad (2.2a)$$

$$W(\varphi) = d\varphi(\varphi)/d\varphi \quad (2.2b)$$

where $M(q)$ and $W(q)$ have units of resistance (Ω) and conductance (\mathcal{U}). The instantaneous power dissipated by the memristor is given by

$$p(t) = M(q(t))i^2(t) \quad \text{or} \quad p(t) = W(\varphi(t))v^2(t) \quad (2.3)$$

Five years after the Chua's first paper on the memristor, Chua and his student, at this time, Kang published a paper and defined a wider class of systems called memristive systems in 1976 [5]. In this paper, they proposed a generic equation to describe the memristive devices and systems. This equation is

$$y = g(x, u, t)u \quad (2.4a)$$

$$\frac{dx}{dt} = f(x, u, t) \quad (2.4b)$$

where x is the state variable, u and y are the input and the output of the system, respectively, f is a continuous n -dimensional function and g is a continuous scalar function. This special structure was proposed to distinguish between memristive systems and dynamical systems.

2.2 HP Memristor

Since Chua postulated the existence of the memristor, scientists were observing pinched hysteresis characteristics in different materials and structures besides reporting the current–voltage characteristics. Until 2008, when HP Labs announced that they found the missing element and published their findings in Nature [6]. In addition, the HP team introduced the first basic model of memristor which is governed by the mathematical formulation of Chua's memristive systems [5, 6].

The HP memristor was built based on titanium dioxide, which is a stable compound. The memristor structure is composed of two chemically different layers; TiO_2

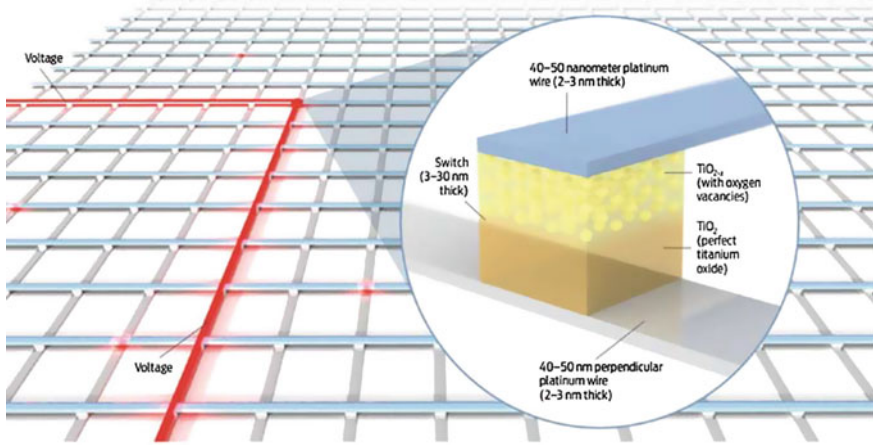


Fig. 2.1 How HP memristor works (adopted from [8])

(high impedance) adjacent to the molecules, and closer to the top platinum electrode, the titanium dioxide was missing around 2.5 % of its oxygen which is called oxygen-deficient titanium dioxide TiO_{2-x} (conductive) [7, 8]. The oxygen vacancies are donors of electrons, so the vacancies are positively charged as shown in Fig. 2.1. When applying a positive voltage to the top electrode of the device, it will repel the oxygen vacancies in the TiO_{2-x} layer (doped region) down into the pure TiO_2 layer (undoped region). Transferring the oxygen vacancies from the TiO_{2-x} layer to TiO_2 layer which increases the width of TiO_{2-x} layer and decreases the width of TiO_2 . But, applying a negative voltage has the opposite effect where the oxygen vacancies are attracted to the electrode making the undoped layer wider and decreases the doped layer.

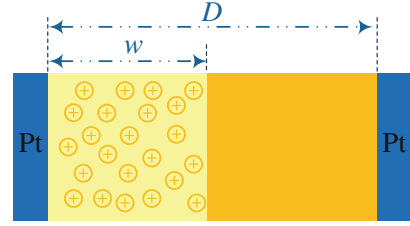
According to the previous description, the HP team presented a mathematical model for their memristor. This model is based on two series resistors R_{on} and R_{off} where R_{on} and R_{off} are the doped and the undoped region resistances. It is assumed that the physical device is of width, D , and the doped region of width, w , as shown in Fig. 2.2. Note that the doped region with width, w , is the state variable which changes depending on the charge [6].

$$M(t) = R_{on} \frac{w(t)}{D} + R_{off} \left(1 - \frac{w(t)}{D} \right) \quad (2.5a)$$

$$\frac{dw}{dt} = \frac{\mu_v R_{on}}{D} i(t) \quad (2.5b)$$

where μ_v is the average ion mobility.

Fig. 2.2 HP memristor model



2.3 Basic Memristor Fingerprints

There are three characteristic fingerprints, memristors should exhibit [9, 10]:

- The device must exhibit a pinched hysteresis loop in the voltage–current plane for any bipolar periodic signal excitation as Chua said “If it is pinched, it is a memristor” [11].
- The pinched hysteresis lobe area should decrease monotonically as the excitation frequency increases.
- The pinched hysteresis loop should shrink to a single-valued function when the frequency tends to infinity.

2.4 Memristor Models

This element is very important due to its potential in life applications, thus it should be properly modeled in order to be used in the analysis, design, and simulation of memristor-based circuits. In 2008, the first practical model was described by HP Labs in [6], then later several models were proposed. In this section a brief summary is presented.

2.4.1 Linear Ion Drift Model

The year 2008 witnessed the solid-state memristor existence by the HP Labs team [6]. Strukov et al. published their results that described the memristor device in which the pinched hysteresis existed between the current and the voltage, described as illustrated in the second row of Table 2.1. The actual memristance is dependent on the ratio between the value of the dynamic state variable $w(t)$, representing the thickness of the oxygen-deficient titanium dioxide layer (TiO_{2x}) and the device thickness D . Strukov et al. included some basic equations for an ideal model of the memristor, where this model assumes that the vacancies have freedom to move around the entire length of the device. But it is not true, since vacancies slow down a lot at the boundary because if they move through the entire device, it means that there will be no physical

Table 2.1 Mathematical equations of memristor's models

Model	Current–voltage relation	State variable derivative
Linear ion drift	$v(t) = \left(R_{on} \frac{w(t)}{D} + R_{off} \left(1 - \frac{w(t)}{D} \right) \right) i(t)$	$\frac{dw(t)}{dt} = \frac{\mu_v R_{on}}{D} i(t)$
Nonlinear ion drift	$i(t) = w^n(t) \beta \sinh(\alpha v(t)) + \chi [\exp(\gamma v(t)) - 1]$	$\frac{dw(t)}{dt} = a v^n(t) f(w)$
Simmons tunneling barrier	$i(t) = \tilde{A}(x, v_g) \phi_1(v_g, x) \times \exp(-B(v_g, x) \cdot \phi_1^{0.5}(v_g, x)) -$ $\tilde{A}(x, v_g) (\phi_1(v_g, x) + e v_g) \times \exp(B(v_g, x)(\phi_1(v_g, x) + e v_g)^{0.5})$ $v_g = v - i(t)R_s$	$\frac{dx(t)}{dt} =$ $\begin{cases} c_{off} \sinh(\frac{i}{i_{off}}) \exp[-\exp(\frac{x - a_{off}}{w_c} - \frac{ i }{b}) - \frac{x}{w_c}] & i > 0 \\ c_{on} \sinh(\frac{i}{i_{on}}) \exp[-\exp(\frac{x - a_{on}}{w_c} - \frac{ i }{b}) - \frac{x}{w_c}] & i < 0 \end{cases}$
TEAM	$v(t) = [R_{on} + \frac{R_{off} - R_{on}}{x_{off} - x_{on}} (x - x_{on})] i(t) \text{ or}$ $v(t) = R_{on} \exp(\frac{\lambda}{x_{off} - x_{on}} (x - x_{on})) i(t)$	$\frac{dx(t)}{dt} = \begin{cases} k_{off} (\frac{i(t)}{i_{off}} - 1)^{\alpha_{off}} \cdot f_{off}(x) & 0 < i_{off} < i \\ 0 & i_{on} < i < i_{off} \\ k_{on} (\frac{i(t)}{i_{on}} - 1)^{\alpha_{on}} \cdot f_{on}(x) & i < i_{on} < 0 \end{cases}$

oxygen vacancies in the device and the length of the doped region is zero, which does not make sense. Similarly, the doped region cannot take up all the device length; since it will leave no undoped region and the device will not work. In order to overcome the boundary problem, a window function ($f(w)$ or $f(x)$) is adopted and added to the state variable derivative.

2.4.2 Nonlinear Ion Drift Model

The linear drift model produces the hysteresis characteristics of the memristor, but it also has some limitations regarding basic electrodynamics. Studies and experiments have proved that the behavior of the implemented memristors are quite nonlinear and the linear ion drift model is not accurate enough. This model assumes that the memristor is a voltage-controlled element having nonlinear dependency between the voltage and the state derivative. Moreover, asymmetric switching behavior is considered. Lehtonen et al. [12] proposed a model based on the results of [13]. The current–voltage relationship and state variable derivative of this model are described in the third row of Table 2.1 where α , β , γ , χ , a and m are experimental fitting parameters, and n determines how the state variable can affect the current. Here, the state variable w is normalized within the interval $[0, 1]$. This model shows asymmetric switching behavior where during the ON state, the I–V curve follows a tunneling process (sinh part). But, during the OFF state, the I–V curve behaves similar to a PN junction (the exponential part). The exponential model presents a more reasonable description of a functional memristive device. The fact that this model is more sensitive to voltage levels gives it the flexibility to reconcile stable reading with fast writing. A low voltage level can be used during the read process which will lead to a very long switching time that translates into a more stable device. On the other hand, a higher voltage level can be used for writing the memristor in much smaller time intervals.

2.4.3 Simmons Tunnel Barrier Model

A more accurate physical model was proposed by [14] where this device is modeled as a resistor in series with an electron tunnel barrier. But in the previous models, the device is modeled as two series resistors for doped and undoped oxide regions. This model assumes nonlinear and asymmetric switching behavior due to an exponential dependence of the movement of the ionized dopants. Besides, this model exhibits nonlinear and asymmetric switching characteristics. The width of Simmons tunnel barrier is the state variable x [15]. The relationship between the current and the voltage is shown as an implicit equation based on the Simmons tunneling model [14]. Fourth row in Table 2.1 shows the state variable derivative relation where C_{off} , C_{on} , a_{off} , a_{on} , i_{off} , i_{on} , and b are fitting parameters. C_{on} is an order

of magnitude larger than C_{off} , and they both have an effect on the magnitude of the change of x . i_{on} and i_{off} confine the current threshold in an effective way. These current thresholds are useful in digital applications. The values of a_{off} and a_{on} force the upper and the lower bound for x , respectively, so there is no need for a window function. This model is the most accurate model for the memristor but it suffers some problems; (1) it is complicated, (2) the relationship between current and voltage is not explicit, and (3) it is not a generic model, since it describes a specific type of memristor. A complicated SPICE model of Simmons tunnel barrier is proposed in [16].

2.4.4 Threshold Adaptive Memristor Model

In Kvatsinsky et al. [17], introduced a simple and a generic model which fits the aforementioned models even the physical model with acceptable error. This simple model is built based on a couple of assumptions for analysis simplification and computational efficiency; (1) no change in the state variable below a certain threshold, and (2) instead of exponential dependence, there is a polynomial dependence involved between the memristor current and the internal state drift derivative. The dependence of the internal state derivative on current and the state variable itself is modeled by multiplying two degenerate functions: one is a function of current and the other is dependent on state variable x as obvious in the fifth row in Table 2.1. Where k_{off} , k_{on} , α_{off} , and α_{on} are constants ($k_{off} > 0$, $k_{on} < 0$). i_{off} and i_{on} are current thresholds and x is the internal state variable. The functions $f_{off}(x)$ and $f_{on}(x)$ act as the window functions, constraining x to the bounds $[x_{on}, x_{off}]$. Moreover, two current–voltage relationships to fit the previous models (written in Table 2.1). In the first relation, the memristance is linearly proportional to the state variable x which fits the first two models. However, the second relation is built to fit Simmons tunnel barrier where the memristance is exponentially proportional to the state variable x where λ is a fitting parameter and should satisfy $\lambda = \ln(R_{OFF}/R_{ON})$. R_{ON} and R_{OFF} are effective memristances at bounds x_{on} and x_{off} , respectively.

As stated in [17], the TEAM model is accurate enough with a mean error of 0.2% and can boost the simulation runtime by 47.5%. It also satisfies the convergence conditions, computational efficiency required by simulation engines and also the requirements of a memristive system. The conditions for the previous model induction is introduced in details in [17]. A comparison between the different memristive device models is listed in Table 2.2.

2.4.5 Window Functions

Each model has a certain region which can work entirely. For example, the linear ion drift model can work only in the interval of $[0, D]$. So to prevent the state variable from getting out of the bound, and also to add more nonlinear behavior close to the

Table 2.2 Comparison of different memristor adopted from [17]

Model	Linear ion drift	Nonlinear ion drift	Simmons tunneling barrier	TEAM
State variable	$0 \leq w \leq D$	$0 \leq x \leq 1$	$a_{off} \leq x \leq a_{on}$	$x_{on} \leq x \leq x_{off}$
Control mechanism	Current	Voltage	Current	Current
I–V relation	Explicit	Explicit	Ambiguous	Explicit
Memristance relation	Explicit	Ambiguous	Ambiguous	Explicit
Generic	No	No	No	Yes
Accuracy	Lowest	Low accuracy	Highest	Sufficient
Threshold exists	No	No	Yes	Yes

bounds, the derivative of the state variable is multiplied by a window function. So, the window functions should give two things; (1) a state variable working interval, and (2) the nonlinearity near boundaries to force it to reach zero when the state variable is at the bounds. In the following, some of the window functions that have been proposed are introduced in the next sections. Moreover, a comparison between different window functions is listed in Table 2.3.

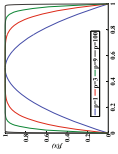
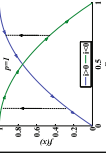
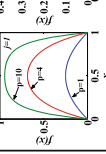
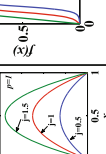
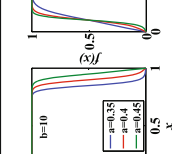
2.4.5.1 HP

In Strukov et al. [6, 18], proposed a simple window function $f(w)$ that reaches its maximum at the center of the device, $w = 0.5D$, and decreases toward the boundaries where it will reach zero speed at the terminal states $w = 0$ or $w = D$. This simple function $f(w)$ is $w(D - w)/D^2$, $0 < w < D$ in which the boundary conditions are $f(0) = f(D) = 0$. This function has a symmetric behavior which does not describe the real nonlinearities of the memristor. All the properties of this window function are shown in Table 2.3.

2.4.5.2 Joglekar

Joglekar and Wolf have developed a generic symmetric window function [19]. The authors added a control parameter to control the nonlinearity of the function, which is $f(x) = 1(2x1)^{2p}$ in which p is a positive control parameter and $x = w/D$. The function looks similar to the rectangular window function when p increases, and the nonlinear drift phenomenon decreases. Moreover, the boundary conditions are simple as $f(0) = f(1) = 0$. Also, the state variable function will approximate the linear drift assumption $f(0 < x < 1) \approx 1$ when $p \leq 5$ [19, 20]. On the other hand, the main disadvantage of HP's and Joglekar's window function is at the boundaries

Table 2.3 Comparison of available window functions

	Joglekar[65]	Biolek [67]	Prodromakis[69]	Piecewise[70]	TEAM [63]
$f(x)$	$1 - (2x - 1)^{2p}$	$1 - (x - sp(-i))^{2p}$	$j(1 - [(x - 0.5)^2 + 0.75]^p)$	$\begin{cases} (1 + (\frac{x-0.5}{a})^{2b})^{-1} & x_0 \leq x \leq 1 - x_0 \\ kx(1-x) & \text{otherwise} \end{cases}$	$\exp \left[-\exp \left(\frac{ x - x_{on,off} }{w_c} \right) \right]$
Symmetry	Yes	Yes	Yes	Yes	Not necessarily
Resolve boundary conditions	No	Discontinuities	Practically yes	Practically yes	Practically yes
Impose nonlinear drift	Partially	Partially	Partially	Partially	Yes
Scalable factor $f_{max} \leq 1$	No	No	Yes	Yes	No
Fits memristor model	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	TEAM for Simmons tunneling barrier fitting
					

where the state variable may cling at the boundary and it becomes difficult to change due to the zero value of the window function at either boundary.

2.4.5.3 Biolek

Biolek et al. introduced a window function with a solution for the modeling inaccuracy of Joglekar's window function and introduced the first PSPICE model for the memristor in [21]. This SPICE model is most commonly used to simulate the memristor in analog and digital circuits ideas. The presented window function is $f(x) = 1(x - \text{sgn}(-i))^{2p}$ where p is a positive integer, i is the memristor current and $\text{sgn}(i) = 1$ when $i \leq 0$ and $\text{sgn}(i) = 0$ when $i < 0$. Biolek et al. introduced this model to overcome the problem of Joglekar's window function (stuck at the boundary). Biolek's function is designed to resolve this problem by using $\text{sgn}(-i)$ which gives different values for approaching and receding the boundaries. But, this raises another problem which is the continuity condition at the boundaries. Also, It should be noted that Biolek's window function is a multivalued function which hardens the analysis of the memristor-based circuits [22].

2.4.5.4 Prodromakis

In Prodromakis et al. [23], handled a problem in the aforementioned window functions which is the scalability. The authors designed this window function to be scalable and include HP's window function. This window function is $f(x) = j(1 - [(x - 0.5)^2 + 0.75]^p)$ where p is a control parameter and is a positive real number unlike the constraint of the control parameter being an integer in the Joglekar's and Biolek's functions. Also, when $p = 1$, this model is reduced to HP's window function. The scalable factor j is used to adjust the maximum value of the window function f_{max} . The properties of this window function are shown in Table 2.3.

2.4.5.5 Piecewise

In [24], the piecewise window function is presented. This window function is continuously differentiable and consists of three nonlinear pieces. Also, a single-valued function between the memristance and the charge can be obtained. This window function is shown in Table 2.3 where $a \in (0, 0.5)$, $b \in \mathbb{Z}^+$, and $x_0, k \in \mathbb{R}^+$. But, there are certain conditions to ensure the continuous differentiability of this window function as given in [24].

2.4.5.6 TEAM

This window function is designed to fit the behavior of Simmon tunnel model barrier [17]. There are two functions for ON and OFF switching and do not have to be equal like the Simmons tunnel barrier model where the dependence on x is asymmetric. The parameters x_{on} , x_{off} , and w_c are fitting parameters. More details about this window can be found in [17].

2.5 Mathematical Modeling of HP Memristor

The transient response under any voltage supply $v_s(t)$ on the memristor based on the linear dopant HP's memristor model was discussed before in [20, 25, 26]. Assuming that the memristance value R_m is at an initial value R_i , then the current passing through the memristor is given by:

$$i(t) = \frac{v_i(t)}{R_m(t)} = \frac{1}{\eta k} \frac{dx}{dt} = \frac{-1}{\eta k R_d} \frac{dR_m(t)}{dt}, \quad (2.6)$$

where η reflects the memristor polarity, $k = \mu_n R_{on}/D^2$, and $R_d = R_{off} - R_{on}$. Therefore

$$R_{mc}^2(t) = R_i^2 - 2\eta k R_d \varphi(t), \quad R_m(t) = \min(\max(R_{mc}(t), R_{on}), R_{off}), \quad (2.7)$$

where $\varphi(t)$ is the flux at time t , $R_{mc}(t)$ is the calculated memristance, $R_m(t)$ is the final memristance value after the clipping conditions to make sure that $R_m(t) \in [R_{on}, R_{off}]$. Based on the HP's paper [6], let us assume that $R_{on} = 100 \Omega$, $R_{off} = 16,000 \Omega$, $\mu_n = 10^{-14}$, $D = 10 \text{ nm}$ for the upcoming examples. For example, if $v_s(t) = V_o$ (DC supply), the value of the memristance is given by [20]:

$$R_m(t) = \sqrt{R_i^2 - 2k\eta R_d V_o t}, \quad R_m \in [R_{on}, R_{off}], \quad (2.8)$$

Figure 2.3 illustrates the changes of the memristance value versus time, initial value R_i and also versus the voltage amplitude V_o . However, if $v_s(t) = t$, then the memristance value can be obtained as: $R_m(t) = \sqrt{R_i^2 - k\eta R_d t^2}$, $R_m \in [R_{on}, R_{off}]$ as shown in Fig. 2.4 where the memristance reaches its minimum value R_{on} at different times based on the initial value.

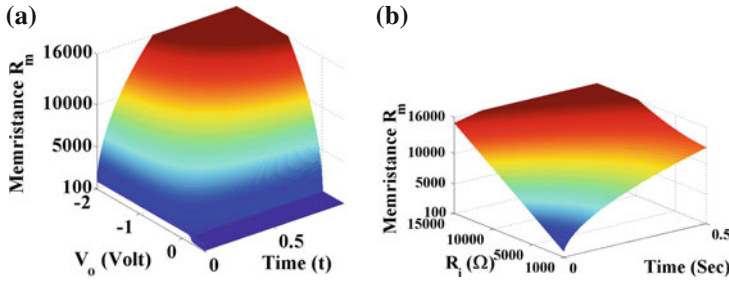
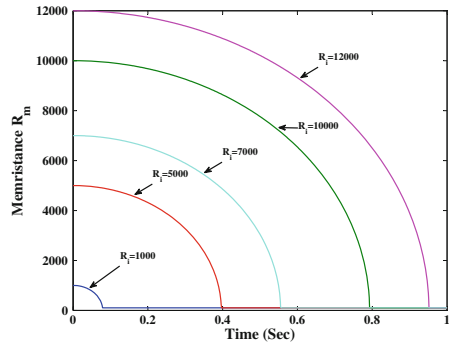


Fig. 2.3 The memristance value in case of step input voltage $v_s(t) = V_o$, $\eta = +1$ versus **a** time – V_o plane when $R_i = 1000 \Omega$, and **b** time – R_i plane when $V_o = -1 \text{ V}$

Fig. 2.4 The transient response of the memristance value under ramp input source $v_s(t) = t \text{ V}$, when $\eta = +1$ for different values of $R_i = 1, 5, 7, 10, 12 \text{ k}\Omega$



As discussed before, the basic characteristics of the memristor appear under sinusoidal input $v_s(t) = V_o \sin(\omega t + \theta)$, where the memristance value can be calculated as [25]:

$$R_m(t) = \sqrt{R_i^2 - \frac{2k\eta R_d V_o}{\omega} (\cos(\theta) - \cos(\omega t + \theta))}, \quad R_m \in [R_{on}, R_{off}], \quad (2.9)$$

Figure 2.5 shows the input voltage and memristance for two different frequencies $f = 0.5 \text{ Hz}$ and $f = 1 \text{ Hz}$ where the memristance reaches its maximum in the first case as the flux increases unlike the second case. Moreover, the effect of the angle θ is shown in Fig. 2.6. Figure 2.7 presents the time waveforms of the input voltage, current as well as the $i - v$ and $R - v$ characteristics for two different frequencies where the range of R_m decreases as the frequency increases. Also, Fig. 2.8 shows the rotation effect of the $i - v$ characteristic versus frequencies until the memristance effect disappeared at high frequency. The upper limit of the memristance versus the $V_o - f$ is shown in Fig. 2.9a which illustrates the resistance range for many case. From the previous discussion, the hysteresis loop should decrease as the frequency

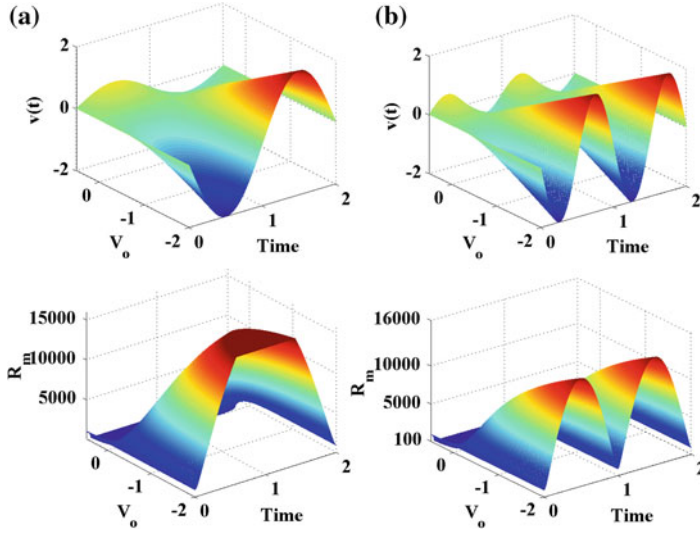


Fig. 2.5 The input voltage and the memristance value versus the $V_o - \text{time}$ plane when the input voltage is $v_s(t) = V_o \sin(2ft + \theta)$ when $R_i = 1 \text{ k}\Omega$ for two different frequencies; **a** $f = 0.5 \text{ Hz}$, and **b** $f = 1 \text{ Hz}$

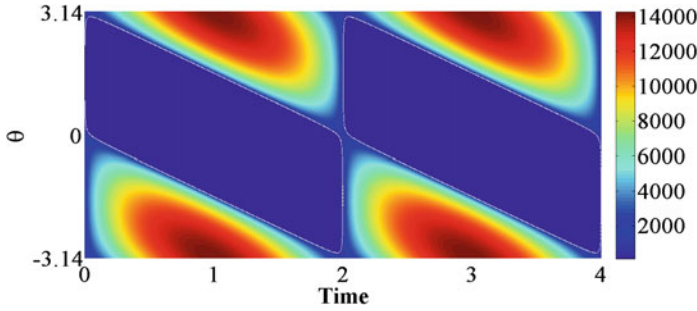


Fig. 2.6 The memristance contours versus $\text{time} - \theta$ plane when the input voltage is $v_s(t) = V_o \sin(2ft + \theta)$, $R_i = 1 \text{ k}\Omega$, and $f = 0.5 \text{ Hz}$

increases. Figure 2.9b shows the upper loop where A_1 and A_2 are the areas when the voltage increases and decreases, respectively. The area enclosing the $i - v$ hysteresis is inversely proportional to the frequency f which validates the previous figures. Moreover, the relationship between the charge and flux can be obtained by:

$$q = \int_0^t i(\tau) d\tau = \int_0^t \frac{v(\tau)}{\sqrt{R_i^2 - 2k\eta R_d \varphi(\tau)}} d(\tau) = \frac{\sqrt{R_i^2 - 2k\eta R_d \varphi} - R_i}{\eta k R_d}. \quad (2.10)$$

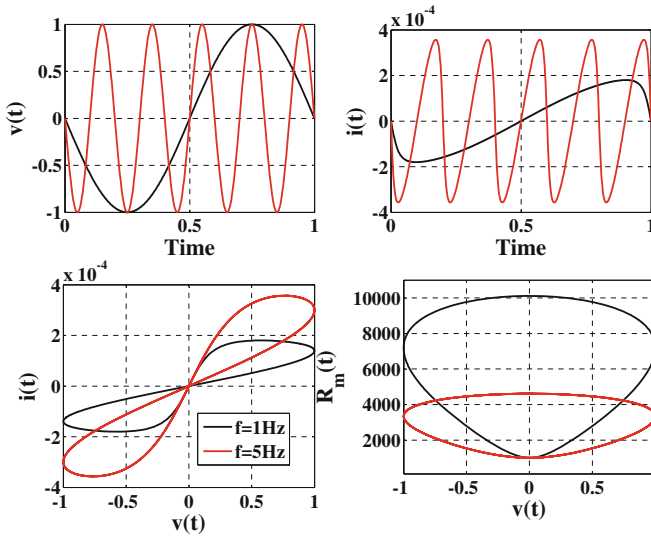


Fig. 2.7 The input voltage, current, $i-v$, and R_m-v responses when the input voltage is $v_s(t) = -\sin(2ft + \theta)$, $R_i = 1 \text{ k}\Omega$, $\theta = 0$, and for two different frequencies $f = 1$ and 5 Hz

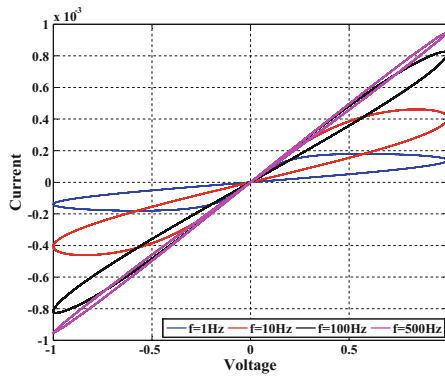


Fig. 2.8 The $i-v$ characteristics for sinusoidal input with $R_i = 1 \text{ k}\Omega$, $\theta = 0$, $V_o = -1 \text{ V}$ for four different frequencies $f = 1, 10, 100, 500 \text{ Hz}$

The flux-charge relationship is represented by a parabola centered at $(\varphi, q) = (\frac{R_i^2}{2\eta k R_d}, \frac{R_i}{\eta k R_d})$. More discussion about the periodic responses and sensitivity analysis of the flux were presented in [25].

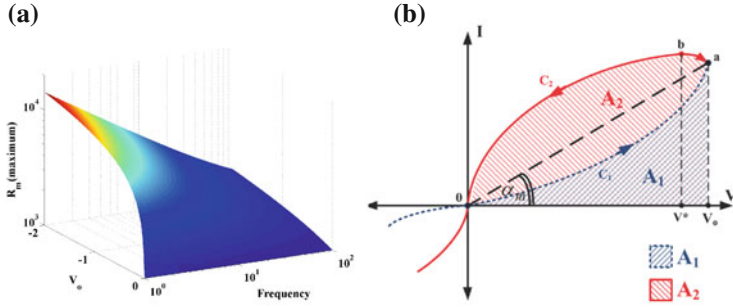


Fig. 2.9 **a** The upper limit of the memristance under sinusoidal input with $R_i = 1 \text{ k}\Omega$, $\theta = 0$ versus the V_o – frequency plan, and **b** the area inside the $i - v$ hysteresis loop

2.6 Mathematical Representations of Time-Invariant Memristor

In 2014 Chua [27], introduced three mathematical representations of time-invariant memristors, each one has two forms depending on whether the input signal is a current source (current-controlled memristor) or a voltage source (voltage-controlled memristor). In the following sections, we will present these three representations as follows:

2.6.1 Extended Memristor

An extended memristor is defined as:

- Current-controlled extended memristor

$$v = R(x, i)i, \quad (2.11a)$$

$$\frac{dx}{dt} = f(x, i), \quad (2.11b)$$

where $\lim_{i \rightarrow 0} R(x, i) \neq \infty$.

- Voltage-controlled extended memristor

$$i = G(x, v)v, \quad (2.12a)$$

$$\frac{dx}{dt} = g(x, v), \quad (2.12b)$$

where $\lim_{v \rightarrow 0} G(x, v) \neq \infty$.

For example [27], let us consider an extended memristor which is defined by the following equations:

$$v = R(x, i)i = 0.01x^2i^3, \quad (2.13a)$$

$$\frac{dx}{dt} = f(x, i) = -x^3 - 2x^2 + (3 + t^2)x. \quad (2.13b)$$

When $i = I$, the DC $V - I$ curve can be obtained by solving the DC equilibrium equation $\frac{dx}{dt} = 0$, then $f(x, I) = 0 = x(I^2 - (x - 1)(x - 3))$. Therefore, $x = 0$ is an equilibrium state independent of the value of I . The other two states are given by $x = -1 \pm \sqrt{4 + I^2}$.

Although there are three $V - I$ branches are $V = 0$ and $V = 0.01(-1 \pm \sqrt{4 + I^2})^2 I^3$ as shown in Fig. 2.10a but the first curve ($V = 0$) is unstable, while the other two curves are stable [27]. The pinched $i - v$ pinched characteristic when $i = 10\sin(2\pi ft)$ for two different frequencies $f = 5$ and 20 Hz are also shown in Fig. 2.10b.

It should be noted that satisfying (2.11) and (2.12) is not enough to obtain an extended memristor model. For example [27], let us assume the following system:

$$v = R(x, i)i, \quad R(x, i) = \frac{\alpha x}{i} \quad (2.14a)$$

$$\frac{dx}{dt} = \beta i. \quad (2.14b)$$

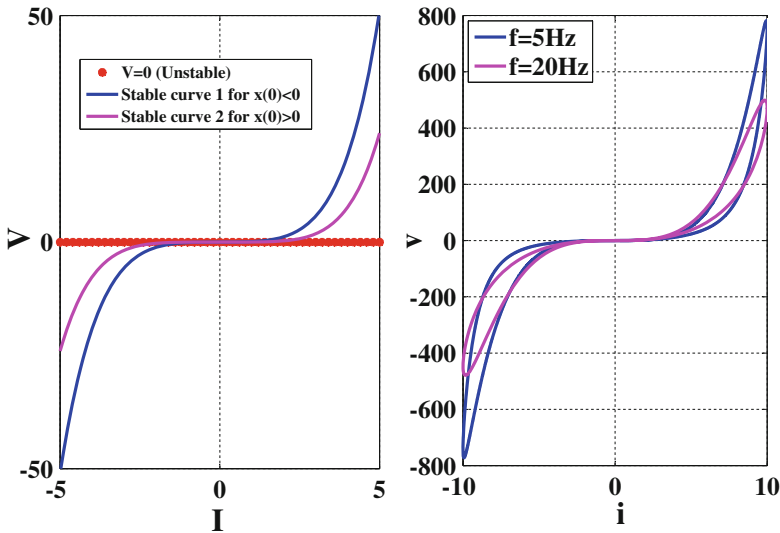


Fig. 2.10 a The $I - V$ DC curves, and b the $i - v$ characteristics for sinusoidal input

where α and β are constants. Let us apply current source, $i(t) = \cos(t)$, across this memristor. Thus, the state variable is $x(t) = x(0) + \beta \int_0^t \sin(\tau) d\tau = \sin(t)$ assuming zero initial conditions. Substituting into (2.14), we obtain $v = \alpha\beta \sin(t)$ so $i^2 + v^2 = \cos^2(t) + (\alpha\beta \sin(t))^2 = 1$ for $\beta = 1/\alpha$. This means that Lissajous figure in the $v - i$ plane is the unit circle which is not pinched at the origin $(v, i) = (0, 0)$. The previous system defines 1 Farad capacitor. So, we can reach a remark which is

If $v - i$ plane isn't pinched, it's not a memristor.

2.6.2 Generic Memristor

A generic memristor is defined in

- Current-controlled generic memristor

$$v = R(x)i, \quad (2.15a)$$

$$\frac{dx}{dt} = f(x, i), \quad (2.15b)$$

- Voltage-controlled generic memristor

$$i = G(x)v, \quad (2.16a)$$

$$\frac{dx}{dt} = g(x, v). \quad (2.16b)$$

2.6.3 Ideal Memristor

An ideal memristor is defined as

- Current-controlled ideal memristor

$$\varphi = \varphi_1(q). \quad (2.17)$$

Or

$$v = R(q)i, \quad (2.18a)$$

$$\frac{dq}{dt} = i, \quad (2.18b)$$

where $R(q) = \frac{d\varphi_1(q)}{dq}$ is called memristance in Ohm (Ω). The constitutive relation of current-controlled ideal memristor can be recovered to $\varphi_1(q) = \varphi_0 + \int_0^t R(q) dq$ where φ_0 is an arbitrary constant.

- Voltage-controlled ideal memristor

$$q = q_1(\varphi). \quad (2.19)$$

Or

$$i = G(\varphi)v, \quad (2.20a)$$

$$\frac{d\varphi}{dt} = v, \quad (2.20b)$$

where $G(\varphi) = \frac{dq_1(\varphi)}{d\varphi}$ is called memductance in Siemens (S). The constitutive relation of voltage-controlled ideal memristor can be recovered to $q_1(\varphi) = q_0 + \int_0^t G(\varphi) d\varphi$ where q_0 is an arbitrary constant.

2.6.3.1 Memristor Siblings

Every ideal memristor can be recast into a generic memristor with a scalar state variable x defined via a differentiable one-to-one function in the following steps:

For a given constitutive relation between y and u

$$y = y_1(u). \quad (2.21)$$

1. Choose any differentiable one-to-one function

$$x = x_1(u), \quad (2.22)$$

and calculate its inverse function as

$$u = x_1^{-1}(x). \quad (2.23)$$

2. Differentiate (2.21) relative to u then substitute by (2.23) to calculate $\frac{y}{u} = Z$ as follows:

$$Z(x) = \left. \frac{dy_1(u)}{du} \right|_{u=x_1^{-1}(x)}. \quad (2.24)$$

3. The relation between the state derivative $\frac{dx}{dt}$ and u is calculated by:

$$f(x, \frac{du}{dt}) = f_1(x) \frac{du}{dt}, \quad (2.25)$$

where

$$f_1(x) = \frac{dx_1(u)}{du} \Big|_{u=x_1^{-1}(x)}. \quad (2.26)$$

4. Define the memristor sibling as follows:

$$y = Z(x)u, \quad (2.27a)$$

$$\frac{dx}{dt} = f_1(x)u, \quad (2.27b)$$

The aforementioned are applicable for current- or voltage-controlled memristor siblings by setting (φ, q) or (q, φ) instead of (y, u) , respectively. Thus, $Z(\cdot)$ become $R(\cdot)$ or $G(\cdot)$ for current or voltage-controlled memristor.

Since the function $x = x_1(u)$ can be chosen to be any differentiable one-to-one function, it follows that every ideal memristor has an uncountable number of memristor siblings that would give the same voltage response to a given input current $i(t)$ (the same current response to a given input voltage $v(t)$). So as Chua said “Indeed, every Ideal Memristor is the mother of an infinite family of equivalent Generic Memristors” [27].

2.6.3.2 Ideal Generic Memristor

This is a small subclass of generic memristor where $F(x) = \int \frac{dx}{f_1(x)}$ is one-to-one function.

An example of creating an ideal generic memristor sibling [27] is given by assuming that the constitutive relation between (y, u) is

$$y = u + u^3/3 \quad (2.28)$$

by following the previous steps;

Step 1: the arbitrary differentiable one-to-one function is $x = u^3 = x_1(u)$. So the inverse relation is given by $u = x^{\frac{1}{3}} = x_1^{-1}(x)$.

Step 2: $Z(x) = \frac{dy_1(u)}{du} \Big|_{u=x^{\frac{1}{3}}} = 1 + x^{\frac{2}{3}}$.

Step 3: $f_1(x) = \frac{dx_1(u)}{du} \Big|_{u=x^{\frac{1}{3}}} = 3x^{\frac{2}{3}}$.

Step 4: The memristor sibling is given as follows:

$$y = (1 + x^{\frac{2}{3}})u, \quad (2.29a)$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}u. \quad (2.29b)$$

In case of current-controlled ideal generic memristor sibling is given by:

$$v = (1 + x^{\frac{2}{3}})i, \quad (2.30a)$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}i. \quad (2.30b)$$

But for current-controlled ideal generic memristor sibling is given by:

$$i = (1 + x^{\frac{2}{3}})v, \quad (2.31a)$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}v. \quad (2.31b)$$

It is worth to be noted that HP memristor is the trivial ideal generic Memristor [6] as proved in [27].

2.7 Memristor Implementation Types

This section describe briefly some recent implementations of the memristor based on different materials. Till now there is no data sheet for the memristor because it is not being available commercially. Since the hysteresis is an indicator of the memristive properties for any material, there are huge efforts using different materials for implementations where experimental results are obtained.

- Titanium dioxide memristor

The resistive switching characteristics of titanium dioxide were originally described in 1960 [28]. Then, around 300 papers were published on titanium dioxide until 2008 [8]. For example, IBM published an article in 2000 regarding structures similar to that described by HP [29], also Samsung has a U.S. patent for oxide-vacancy-based switches [30]. In 2008, HP reported that the memristor can be obtained based on the titanium dioxide [6] and published a U.S. patent application related to the memristor construction [31].

- Polymeric (ionic) memristor

Different realizations of a polymeric memristor have been published even before the HP memristor. For instance, in 2004, Krieger et al. proposed a structure of a passive layer between electrode and active thin films, which enhanced the extraction of ions from the electrode to create functioning nonvolatile memory cells [32]. Also in 2008, Erokhin and Fontana developed a polymeric memristor [33]. Then in 2009, Berzina et al. reported results on the improved performance of electrochemically controlled polymeric memristors [34].

- Ferroelectric memristor

The first ferroelectric memristor was proposed in 1963 [35] where the basic idea of this device is to perform the function of memory in ferroelectric material, and to control the field-effect conductance of a semiconductor by the permanent

polarization of the ferroelectric material. But in 2012, the ferroelectric memristor was proposed in [36] based on a thin ferroelectric barrier sandwiched between two metallic electrodes. Switching the polarization of the ferroelectric material by applying a positive or negative voltage across the junction can lead to two orders of magnitude resistance variation: $R_{OFF} \gg R_{ON}$ (an effect called Tunnel Electro-Resistance). In general, the polarization does not switch abruptly. The reversal occurs gradually through the nucleation and growth of ferroelectric domains with opposite polarization. During this process, the resistance is neither R_{ON} or R_{OFF} , but in between. When the voltage is cycled, the ferroelectric domain configuration evolves, allowing a fine-tuning of the resistance value. The ferroelectric memristor's main advantages are that the ferroelectric domain dynamics can be tuned, offering a way to engineer the memristor response, and that the resistance variations are due to a purely electronic phenomena, and aiding device reliability as no deep change to the material structure is involved.

- **Resonant-tunneling diode memristors**
Memristive properties have appeared in certain types of quantum well diodes with special doping designs of the spacer layers between the source and drain regions [37, 38].
- **Graphene Oxide memristors**
Choi and his team have made flexible memristors using thin graphene oxide films [39]. They use a similar design, swapping titanium dioxide for graphene oxide. After depositing 50-micrometer-wide aluminum wires on a 6.5 cm^2 piece of plastic, they spin a solution containing suspended graphene oxide flakes onto the surface. This forms a thin film of overlapping graphene oxide flakes over which the researchers deposit the top aluminum wire array. This results in 25 memristors, each $50 \text{ }\mu\text{m}$ wide. Also, in 2012, Williams and his team in Hewlett-Packard Development Company introduced a patent about fabricating the defective graphene-based memristor [40]. A graphene-based memristor includes a first electrode, a defective graphene layer adjacent to the first electrode, a memristive material that includes a number of ions adjacent to the defective graphene layer, a second electrode adjacent to the memristive material, and a voltage source that generates an electric field between the first and the second electrodes. Under the influence of the electric field ions in the memristive material form an ion conducting channel between the second electrode and the defective graphene layer is formed.
- **Silicon Oxide memristors**
In 2010, researchers developed silicon oxide memristive substrates that show promise for transitioning much of the worlds current fab and production infrastructure to memristor production [41]. Mehonic et al. reported a study of resistive switching in a silicon-based memristor device in which the active layer is silicon-rich silica. The resistive switching phenomenon is an intrinsic property of the silicon-rich oxide layer and does not depend on the diffusion of metallic ions to form conductive paths. Switching exhibits the pinched hysteresis I/V loop characteristic of memristive systems, and on/off resistance ratios of 104:1 or higher can be easily achieved. Scanning tunneling microscopy suggests that switchable

conductive pathways are 10 nm in diameter or smaller. Programming currents can be as low as 2 μA , and transition times are on the nanosecond scale [41].

- **Spin memristive systems**

Spin-based memristive systems, as opposed to molecular and ionic nanostructure-based systems, rely on the property of degree of freedom in electron spin. In these types of systems, electron spin polarization is altered, usually through the movement of a magnetic domain wall separating polarities, allowing for hysteresis-like behaviors to occur.

In 2009, Wang et al. described three examples of possible spintronic memristors [42]. These examples are based upon spin-torque-induced magnetization switching and magnetic domain wall motion. Also, they proved that the spintronic device can be designed to explore and memorize the continuum state of current and voltage based on interactions of electron and spin transport. Moreover, in 2011, an experimental proof of the spintronic memristor based on domain wall motion by spin currents in a magnetic tunnel junction was introduced [43].

Certain types of semiconductor spintronic structures exhibit memristive behavior [44]. The mechanism of the memristive behavior in such structures is based entirely on the electron spin degree of freedom which allows for a more convenient control than the ionic transport in nanostructures. When the external excitation is changed, the adjustment of electron spin polarization is delayed because of the diffusion and relaxation processes causing hysteresis.

2.8 Memristor-Based Applications

After HP invented the passive model of the memristor, researchers from all over the world have started significant experiments to demonstrate the applications of the memristor. Memristors have been proposed for a wide range of applications such as nonlinear analog circuit design, chaotic systems, nonvolatile memory, and neuromorphic systems as will be briefly discussed in this section.

2.8.1 Analog Circuits

2.8.1.1 Memristor-Based Sinusoidal Oscillators

The idea of memristor-based sinusoidal oscillators has been introduced in many recent publications [45–47] which depends on the replacement of some or all resistors with memristors in the most common oscillator circuits and investigating the response. For example, the four Wien oscillators family have been tested using memristors where sustained oscillations were reported and an approximated oscillation frequency is obtained in [46]. Figure 2.11 shows the four different Wien oscillators with the replacement of R_1 with memristor $R_m(t)$. These four cases have been

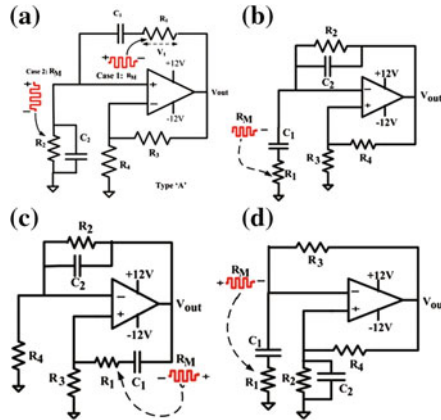


Fig. 2.11 Schematics of other members of Wien oscillator family. **a** Type A, **b** Type B, **c** Type C, and **d** Type D

discussed using PSPICE circuit simulations and Fig. 2.12a shows the output response and the memristance value for each case.

It is important to note that the sustained oscillation is achieved although the memristance value oscillates, which reflects the time-dependent oscillating poles as shown in Fig. 2.12b as a good example for parametric oscillation. The effect of the initial resistance R_i on the oscillation frequency using numerical and PSPICE simulations is also discussed in [48] as shown Fig. 2.14. Other circuits that validate the same concept for third-order oscillators were introduced in [49]. Moreover, a complete resistorless oscillator where all resistors are replaced with memristors was discussed as shown in Fig. 2.13 [50] where six resistors have been replaced with memristors and sustained oscillation has been achieved.

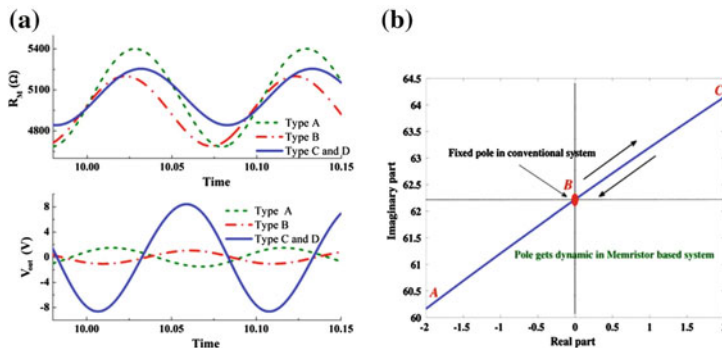


Fig. 2.12 **a** Transient response for the four Wien oscillator family and **b** oscillating poles in the s -plane of type "A"

Fig. 2.13 Resistorless memristor-based oscillator

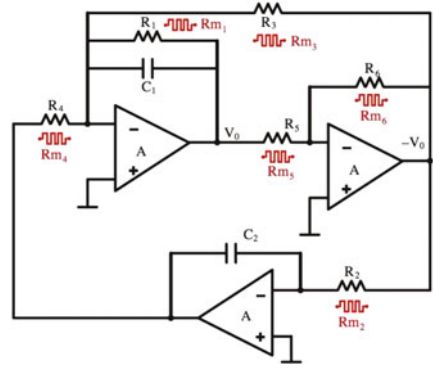
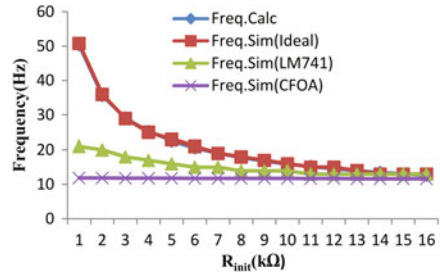


Fig. 2.14 Effect of R_i on the oscillation frequency



2.8.1.2 Programmable Analog Circuits

In many analog circuits such as amplifiers and filters, resistors need to be programmed for adaptation to particular applications or for compensation of PVT (Process, Voltage, and Temperature) variations. The programmable resistor with fine resolution and small parasitics is very useful in many analog and RF range differential circuits. By using the programmable resistance, it can be adopted for programmable attenuators, programmable gain amplifiers and programmable filters, among others.

The most popularly used method to realize programmable resistors takes the form of switch-controlled resistors composed of an array of weighted resistors and switches. However, it has a critical drawback due to the fact that these switches, typically MOS switches, introduce large parasitic capacitances and resistances. Furthermore, the parasitic values are dependent on the switch state. The state-dependent large parasitics limit the resolution and the number of bits of switching resistors. In particular, programming and control of the amount of charge on the floating gate require high voltages for the tunneling and injection to allow electrons with sufficient energy to tunnel through the insulating oxide from/to the floating gate, and thus leads to long-term reliability problems. Another problem with floating-gate devices is that the long-term charge storage capabilities are unreliable. The charge stored on the floating gate may slowly leak away with time and this problem will get worse, as the process scales down with reduced oxide thickness.

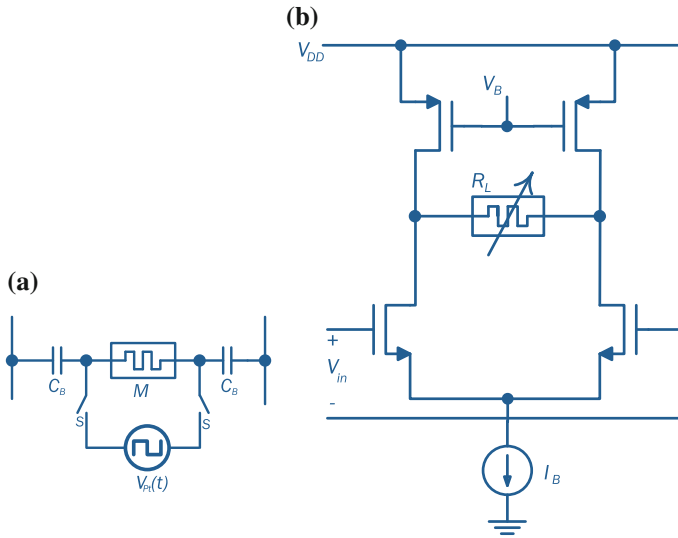


Fig. 2.15 Circuit schematic of **a** programmable resistor using memristor and **b** programmable gain amplifier using the programmable resistor [51, 52]

The authors in [51, 52] introduced a programmable resistor with fine resolution which is built using a memristor as shown in Fig. 2.15a. This programmable resistor consists of a floating memristor, simple series switches (S), provides very high impedances (R_{OFF}) during the normal mode operation and low impedances (R_{ON}) for the programming duration, and two blocking capacitors C_B to block DC mismatch or even order mismatches, which can cause unbalanced flux between the differential signals where this circuit suffers from any unbalanced flux amount across the memristor. Any kind of odd order mismatches will not hurt the differential balance by its nature. Even for the capacitor mismatch, it does not even contribute to the voltage imbalance, unlike the case of the differential gain. In order to ease the programming and controllability operations, they proposed a pulse-coded memristor programming method where the memristance is programmed by patterning the pulse waveform. In case of a voltage-controlled memristor, the flux can be linearly controlled by determining the number of pulses (N_{PULSE}), duty ratio, pulse amplitude (V_{PT}), and pulse frequency (ω_{PT}). In this circuit, the memristance decreases or increases depending on the accumulated flux of the memristor as discussed in Sect. 2.5.

The authors used this idea of programmable resistor to build a programmable gain amplifier, shown in Fig. 2.15b, where the ac voltage gain is $A_v = g_m(r_o // R_L)$ where g_m is the differential transconductance of M_1 and M_2 , r_o is the amplifier's output impedance formed M_1 and M_2 and R_L is the load resistance. Therefore, the ac gain is a function of R_L so by controlling R_L , we can control the ac gain of the amplifier. Thus, the gain decreases or increases depending on the accumulated flux due to pulse source. This memristor-loaded amplifier circuit shows a fine gain resolution over the

wide tuning range under low-voltage programming pulses, other performances such as linearity and speed are exactly the same, as those of the cases with linear load resistors. This circuit becomes more advantageous when the application frequency is in the RF range, since the blocking capacitors can be integrated together with CMOS active devices for higher input frequencies.

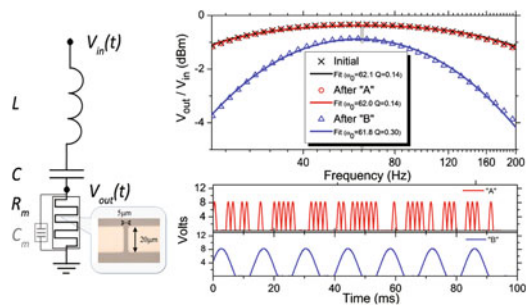
Another programmable memristor circuit is proposed by Pershin and Di Ventra in 2010 [53]. This memristor-based circuit works as a digital-controlled potentiometer which consists of a memristor and a couple of FETs. Two external control signals are used to program the memristance R_m between two limiting values R_1 and R_2 . Furthermore, several programmable analog circuits have been introduced such as a programmable threshold comparator, a programmable gain amplifier and a programmable relaxation oscillator.

Several other papers have been published for introducing different variable gain amplifier (VGA) topology utilizing titanium dioxide (TiO_2) memristors [54–56]. The TiO_2 solid-state memristor was employed in the feedback branch of an inverting voltage amplifier and was programmed externally so the typical circuit gain is M/R_1 followed by a low-pass filter to remove the DC voltage. In [54], the circuit was analyzed based on charge-controlled and voltage-controlled memristor models. Furthermore, in [56], the circuit was experimentally tested using a solid-state memristor. The experimental results show overall good performance of the memristor as a gain setting element in the op-amp feedback branch, where modifying the resistance of the memristor shunts the output impedance of the voltage amplifier, achieving distinct multiple gain levels.

2.8.1.3 Adaptive Filters

In Driscoll et al. [57], introduced the memristive adaptive filters where the memristive properties of vanadium dioxide are used. The authors experimentally demonstrated the adaptive filter functionality by constructing a simple R_mLC band-pass filter shown in Fig. 2.16 by adding a VO_2 memristive device R_m in series with an external capacitor C and inductor L . The inset shows an optical photograph of the two-terminal device used, a $5\ \mu\text{m} \times 20\ \mu\text{m}$ VO_2 region lithographically defined by gold contacts.

Fig. 2.16 Schematic for R_mLC adaptive filter, small-signal transfer function (V_{out}/V_{in}), and time series of the off-resonance “A” sequence of pulses and on-resonance “B” sequence of pulses [57, 58]



Moreover, the adaptive filter transfer function (V_{out}/V_{in}) plotted before and after off-resonance A and on-resonance B pulses and solid lines are RLC band-pass filters fit to data, which generates the ω_o and Q values in the legend showing in Fig. 2.16.

However, in [59], another memristor model is used to obtain first- and second-order low-pass filter. This memristor is based on fabricated zinc oxide (ZnO) nanowires grown on the copper layer of a printed circuit board which shows similar characteristics as memristive metal/oxide/metal structures. The ZnO device is used with a capacitor and an inductor to form a low-pass adaptive filter where the memristor reacts to different input voltage bias and changes its resistance accordingly. Also, the gain, damping, and Q-factor of the low-pass filters are observed to vary with small input voltages.

2.8.1.4 Loop Filter of Phase-Locked Loop

In communication systems, charge-pump phase-locked loop (CPPLL) is extensively used in frequency synthesis and clock recovery. Figure 2.17a shows a schematic diagram of CPPLL, which consists of a phase and frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a divider ($\div N$). In Zhao et al. [60], proposed a memristor-based controlled proportional-integral (PI) controller to design the loop filter in the charge-pump phase-locked loop (CPPLL). The low-pass PI controller is based on a monotonic increasing piecewise linear (PWL) memristor where a periodic rectangular pulse current source is applied as the input. The proportionality constant of the PI controller is controlled by the width of the pulse, i.e., the amount of charge passing through the memristor, which effectively controls the bandwidth of the controller. This circuit is very useful for fast locking when CPPLL is in the unlocked state, and to lower phase noise when CPPLL is in the locked state. In addition, the loop filter is passive and easy to design compared to other implementations such as adaptive bandwidth phase-locked loops (PLLs).

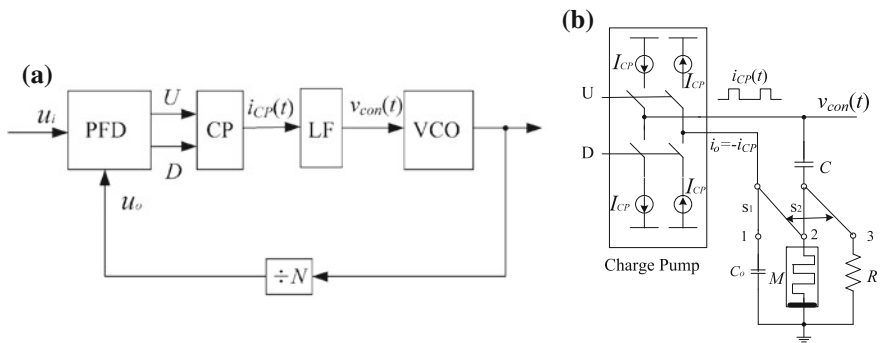


Fig. 2.17 a Schematic diagram of CPPLL and b memristor-based filter circuit [60]

2.8.2 Neuromorphic Circuits

A neuromorphic system is a mixed mode analog–digital system mimicking neural architecture to pattern neurons by real-time computation, simulation, and emulating the nervous system. But to simulate neural networks in electronic regime neurons and synapses (connections between neurons), this requires an implementation with very low power consumption. Electronic synapses are more difficult to engineer as they require being flexible as well as dynamic with memory capability. Scientists have simulated brains of small animals (cat, rat, and spider) [61–64] but associating computer memory more than terabytes (e.g., Blue Gene/P of IBM). Thus, the memristor plays a significant role to perform as a synapse with negligible power thrust [65, 66]. In Pershin et al. [66] have designed a memristor emulator which shows associative memory function with three electronic neurons connected by two memristor–emulator synapses. Also, S.H. Jo made a memristor with a Ag and Si active layer forming a highly conductive Ag-rich region and a less conductive Ag-poor region (Fig. 2.18). This hybrid system is capable of spike timing dependent plasticity (STDP) [67, 68] which is an important synaptic function. If the synapse update rate is 1 Hz, then this system can continue synaptic operation for around 5 years. The basic idea of STDP in memristive devices was proposed before [69] and a practical implementation of circuit learning was demonstrated by patterning the learning of an amoeba-like cell into a memristive system [64].

2.8.3 Chaotic System

Because of the random nature of chaotic systems, the memristor as a nonlinear element is well applicable for encryption and random number generation. The memristor makes it possible for better control and simpler versions of chaotic systems. Chua modeled the memristor to produce a chaotic attractor with negative conductance

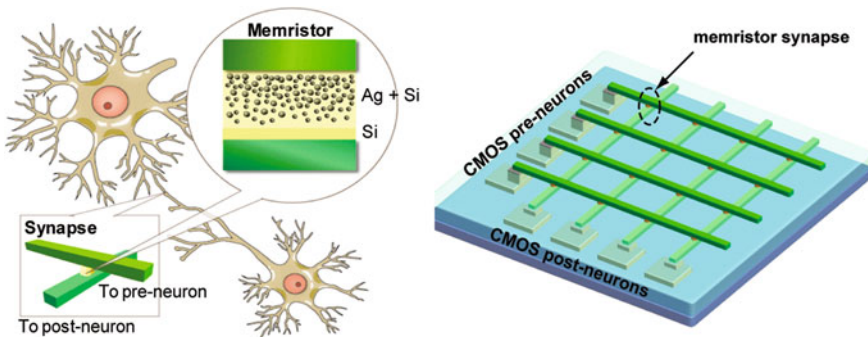
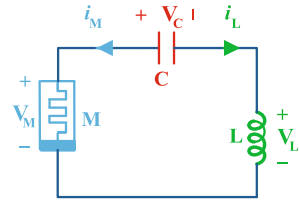


Fig. 2.18 Schematic illustration of using memristors as synapses between neurons [58, 64]

Fig. 2.19 Schematic of the proposed circuit [71]



and capacitor [70]. Though it was merely simulation based but the simplicity and functionality initiated memristor-based chaotic systems. Recently Muthuswamy and Chua demonstrated the simplest chaotic oscillator [71] where they used an inductor–capacitor–memristor series circuit as shown in Fig. 2.19. Though, the memristor was actively realized, and the pinched hysteresis loop was shown by both experimental and theoretical simulation where the memristance function is $R(x) = \beta(x^2 - 1)$ and $\dot{x} = i_M - \alpha x - i_M x$. The nonlinearity of the memristor adds up to the third state variables along with the inductor and the capacitor and the simplest system is also BIBO stable. Around the same time, Muthuswamy has shown another simpler practical implementation [72, 73] of the memristor in generating chaos. The difference between the two circuits is that in [72] the memristor is flux controlled, whereas in [71] it is charge controlled but both realizations look similar.

On the other hand, Cheng has demonstrated a memristor oscillator which gives periodic orbits of chaos from a 2-scroll transient chaos [74]. In another paper [75], a similar transition is observed but with more complicated dynamical behavior of the memristor where the initial condition plays the major role in generating periodic chaos. The effect of the initial condition on chaotic behavior is well studied in [76] where both the piecewise linear model and cubic model of the memristor are shown capable of periodic orbits somewhat similar to Hopf bifurcation. The theoretical study of generating chaos has also appeared in [77] with a cubic model of a flux-controlled memristor.

Recently, a chaotic circuit based on HP memristor was published in [78]. The circuit makes use of two HP memristors in an antiparallel connection as shown in Fig. 2.20a. The circuit is based on the topology of the canonical Chua's oscillator with the Chua's diode substituted by two HP memristors in antiparallel connection. The circuit consists of one negative resistor, two capacitors, an inductor, and two memristors. Numerical results of chaotic behavior are reported in Fig. 2.20, which shows the attractor obtained where three different bi-dimensional projections are also shown.

In order to increase chaos order, the memristive chaos circuits are extended to the fractional order as discussed in [79] where the fractional order is added to a memristor-based Chua's circuit for the first time. Moreover, a numerical solution of the fractional-order memristor-based Chua's equations was derived including dynamical behavior and stability analysis. In [80], the authors extended the simple chaotic circuit (shown in Fig. 2.19) to the fractional-order domain where the numerical solution was given using a predictorcorrector method and stability analysis of the system

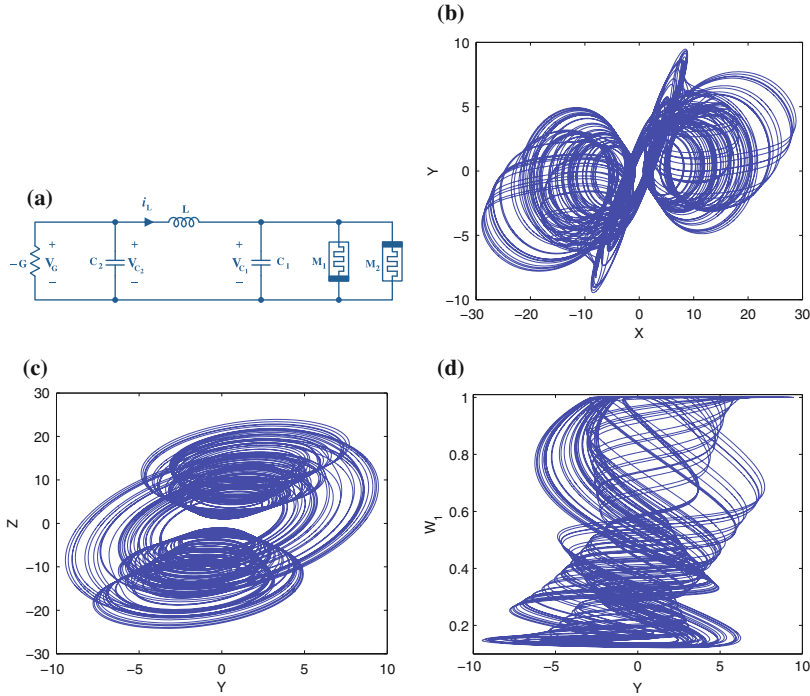


Fig. 2.20 Chaotic circuit and the attractors **a** circuit based on two HP memristors in antiparallel, **b** x-y phase plane, **c** y-z phase plane, and **d** y- w_1 phase plane [78]

equilibria are carried out, with the aim to show that chaos can be found when the order of the derivative is 0.965.

The most common application for chaotic systems is building secure communication systems but the main problem is how to sync between the receiver and transmitter [81]. A novel kind of compound synchronization among four chaotic systems was investigated in [82], where a sufficient condition is obtained to ensure compound synchronization among four memristor chaotic oscillator systems based on the adaptive technique. Moreover, a secure communication scheme via adaptive compound synchronization of four memristor chaotic oscillator systems was introduced. The authors derive the corresponding theoretical proofs and numerical simulations to demonstrate the validity and feasibility of the proposed control technique. Also, in [83], another chaotic oscillator was introduced which depends on the Van der Pol oscillator coupled to a linear circuit (VDPCL). This circuit has a very special stability property, exhibits interesting spectral characteristics, which makes it suitable for chaos-based secure communication applications.

Another category of chaotic oscillators is introduced in [84] which is inductance free. This circuit is composed of a twin-T oscillator, a passive RC network, and a flux-controlled memristor. The circuit exhibits complicated chaotic behavior of double periodicity.

2.8.4 Digital Applications

2.8.4.1 Memories

Resistive Random Access Memory (RRAM) is a two-terminal device where the switching medium is sandwiched between top and bottom electrodes and the resistance of the switching medium can be modulated by applying electrical signal (current or voltage) to the electrodes. Even though large electrical nonvolatile resistance changes are also observed in ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase change of material states RAM (PRAM).

One simple approach to integrate RRAM cells with conventional CMOS circuitry is 1T1R (1 transistor + 1 resistance switching element) structure [85, 86]. The select transistor controls the location of the switching element to be accessed. The 1T1R approach can be integrated with CMOS. However, since each switching element requires one transistor in this approach, the storage density will still be limited by transistor scaling and the advantages of the simple two-terminal RRAM devices have not been fully utilized.

Generally, the memristor essentially shows resistive switching behavior as it has metal–insulator–metal configuration. Before the physical evolution of the memristor, researchers have demonstrated high density memory applications of resistive switching [85–87] where the insulating layer works as a storage medium. Though the memristive characteristics were not realized, and the results held the memristor as a promising candidate as a nonvolatile memory. In [88] Chen assumed a Pt/MgZnO/Pt device as a memristor and showed its resistive switching characteristics which are reversible and steady, leading toward nonvolatile memory. Recently as a nonvolatile memory the density of the memristor is reported to be 100 Gbits/cm² in [89] which requires very low energy compared to the existing flash memory.

HP lab experimentally demonstrated the nonvolatility of the memristor which is CMOS compatible, fast in response, and requires very low power [13, 14, 90]. The nonvolatile memristor latch in [90] is shown to have high endurance of 10⁴ write cycles. In [13], 1 × 17 cross point arrays of the Pt/TiO₂/Pt memristor was fabricated to show the nonvolatility where the oxygen vacancies were engineered for controlling polarity and resistance of switching. The mathematical explanation of resistive switching of Pt/TiO₂/Pt memristor revealed that with higher applied current the switching time reduces sharply to decrease the input energy exponentially [14]. A comprehensive mathematical illustration of the memristor as nonvolatile

memory has been reported in [91] which will help to design a memristive system for memory applications. The nonvolatile memory capability of the memristor will turn on computers without rebooting them and hopefully in the future no physical RAM will be required separately.

In [92], The authors introduced a study of a memristor-based nonvolatile SRAM (or memristor latch) cell to achieve fast bit-to-bit parallel store/restore operations, low store/restore energy consumption, and a compact cell area which is suitable for low power mobile applications. This memristive nonvolatile 8T2R (Rnv8T) cell includes two fast-write memristor (RRAM) devices vertically stacked over the 8T, and a novel 2T memristor switch, which provides both memristor control and SRAM write-assist functions. The write-assist feature enables the Rnv8T cell to use read favored transistor sizing to prevent read/write failure at lower V_{DDs} . Moreover, the authors also fabricated the first macro-level memristor-based nonvolatile SRAM. This 16 Kb Rnv8T macro achieved the lowest store energy and R/W V_{DDmin} (0.45V) of any nonvolatile SRAM or two-macro solution.

Field programmable gate arrays (FPGAs) offer programmability at relatively low development cost and good performance. The common FPGA architecture consists of a regular, flexible and programmable two-dimensional array of configurable logic blocks (CLBs). Usually, a CLB consists of lookup tables (LUTs), multiplexers and flip-flops (FFs). LUTs are used to implement combinational logic circuits. All configurable resources (inclusive of the LUTs) are controlled by the configuration bits stored in a static random access memory cell (SRAM). However, an SRAM is unable to retain the configuration bits should either a malfunction occur at the power supply, or the power is turned off. A possible solution consists of storing the configuration bits in a nonvolatile flash memory; thus the flash memory is integrated into the FPGA. This leads to issues such as a larger silicon area, increase in cost and most importantly very slow data retrieving time. Moreover, as technology enters the very deep submicron and nanoscales, a substantial increase of leakage current is encountered when the FPGA is in standby mode, hence causing additional power dissipation. Thus an alternative nonvolatile memory block (as a LUT) based on the memristor as a storage device was proposed in [93] to overcome the above mentioned issues.

2.8.4.2 Logic Implementation

One exciting application of memristors is using them as the basic building block of a logic gate. In [94] a memristor-based logic gate—the IMPLY gate is implemented. The IMPLY gate can be used to implement all binary operations of two variables.

Borghetti et al. [94] used memristors to realize material implication, and then realized all the fundamental Boolean operations using material implication. The basic implication gate/latch circuit is shown in Fig. 2.21b. Two memristors, P and Q , are connected using a common horizontal nanowire to a load resistance, R_G , which is connected to the ground. The states of P and Q are represented by logic values p and q , respectively. The vertical nanowires cross over the horizontal nanowires and a layer of memristive switching material forming P and Q . Each memristive

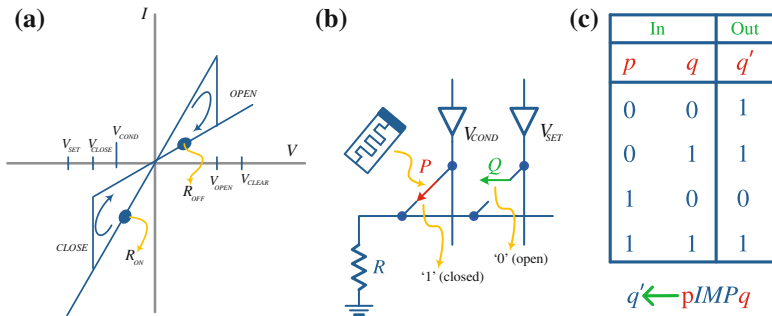


Fig. 2.21 **a** Idealized memristive electrical characteristics, **b** basic implication circuit, and **c** truth table for IMP operation [94, 95]

device can be assigned to logic 1 or logic 0 by using the tri-state drivers. When applying a negative voltage, V_{SET} a device is assigned logic 1 set (operation TRUE). Also when applying a positive voltage, V_{CLEAR} a device is assigned logic 0 clear (operation FALSE), and hence a high memristance is considered as logic 0 and a low memristance is considered as logic 1. V_{COND} is defined as a negative voltage with a magnitude smaller than V_{SET} which does not change the state of the driven device. The notation $p \leftarrow x$ indicates that the state of switch P (the logic value p) is changed to x the next time P is pulsed by V_{CLEAR} , V_{SET} or V_{COND} .

The memristive IMP operation $q \leftarrow p \text{IMP} q$ is implemented by applying V_{SET} to Q and V_{COND} to P simultaneously, in order for the two pulses and the load resistor R_G to change the states of p and q depending on their previous states. When P is in a high memristance state (logic 0), the applied voltage on Q is roughly V_{SET} and Q is turned on ($q = 1$) and p stays unchanged. On the other hand when P is in a low memristance state (logic 1) the voltage on the common terminal becomes V_{COND} and the voltage across memristor Q is roughly $V_{SET} - V_{COND}$ and both P and Q stay unchanged. Figure 2.21c shows the truth table for operation $q \leftarrow p \text{IMP} q$.

Using material implication the 16 binary operations of two variables were realized in the supplementary information of [94]. By using these functions any arithmetic circuit can be realized. The delay can be calculated by calculating how many IMPLY operations are performed in each gate as shown in Table 2.4 [96].

Using these logic gates, any combinational logic can be designed. In Shaltoot and Madian [97], introduced two different memristor-based architectures of carry lookahead adder. The first one is based on conventional carry lookahead adder based on implication. And the second one is simplified carry lookahead adder based on IMPLY gate. Moreover, their proposed circuits gave better results comparable to the conventional carry lookahead adder for increasing the number of bits. As a result, many circuits can be built using the full adder circuit such as multipliers [98].

Table 2.4 Boolean operations implemented via material implication

Operation	Implementation	Devices area
$p \text{ NAND } q$	$=p \text{ IMP } (q \text{ IMP } 0)$	3
$p \text{ AND } q$	$=(p \text{ IMP } (q \text{ IMP } 0)) \text{ IMP } 0$	4
$p \text{ NOR } q$	$=((p \text{ IMP } 0) \text{ IMP } q) \text{ IMP } 0$	4
$p \text{ OR } q$	$=(p \text{ IMP } 0) \text{ IMP } q$	3
$p \text{ XOR } q$	$=(p \text{ IMP } q) \text{ IMP } ((q \text{ IMP } p) \text{ IMP } 0)$	3
$\text{NOT } p$	$=p \text{ IMP } 0$	2

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Memcapacitor, and Meminductor

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2015, XX, 231 p. 188 illus., 29 illus. in color., Hardcover

ISBN: 978-3-319-17490-7