

# Chapter 2

## Enhancing ADC Performance by Exploiting Signal Properties

**Abstract** This chapter starts with a brief introduction of the analog-to-digital conversion process in Sect. 2.1 and a discussion of factors that define the performance of ADCs in Sect. 2.2. ADC performance limitations and trends are addressed in Sect. 2.3. In Sect. 2.4, a brief discussion of popular Nyquist-rate ADC topologies is given where the topologies most relevant to the focus of this book are discussed with the associated tradeoffs. A signal/system-aware design approach which exploits certain signal properties to enhance the ADC performance is discussed in Sect. 2.5 and examples are shown.

### 2.1 Introduction to Analog-to-Digital Converters

An analog-to-digital converter is an electronic circuit which converts a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude signal [1]. The analog-to-digital conversion involves three functions, namely sampling, quantizing and encoding [2], as shown in Fig. 2.1. After the conversion, the continuous quantities have been transformed into discrete quantities with a certain amount of error due to the finite resolution of the ADC and imperfections of electronic components. The purpose of the conversion is to enable digital processing on the digitized signal.

ADCs are essential building blocks in electronic systems where analog signals have to be processed, stored, or transported in digital form. The ADC can be a stand-alone general purpose IC, or a subsystem embedded in a complex system-on-chip (SoC) IC. A main driving force behind the development of ADCs over the years has been the field of digital communications due to continuous demand of higher data rates and lower cost [2]. In Fig. 2.2, a block diagram of a typical digital communication system is shown and the location of the ADC in the system is indicated [3]. The ADC is normally preceded by signal conditioning blocks (e.g. amplifiers, filters, mixers, modulators/demodulators, detectors, etc.) and followed by the baseband digital signal processing unit. With the advance in CMOS process

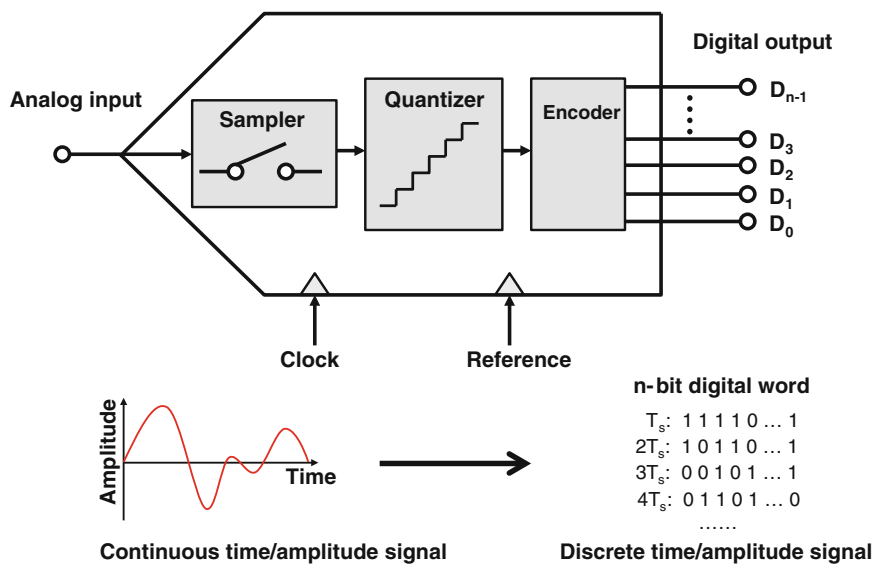


Fig. 2.1 Block diagram of an analog-to-digital converter

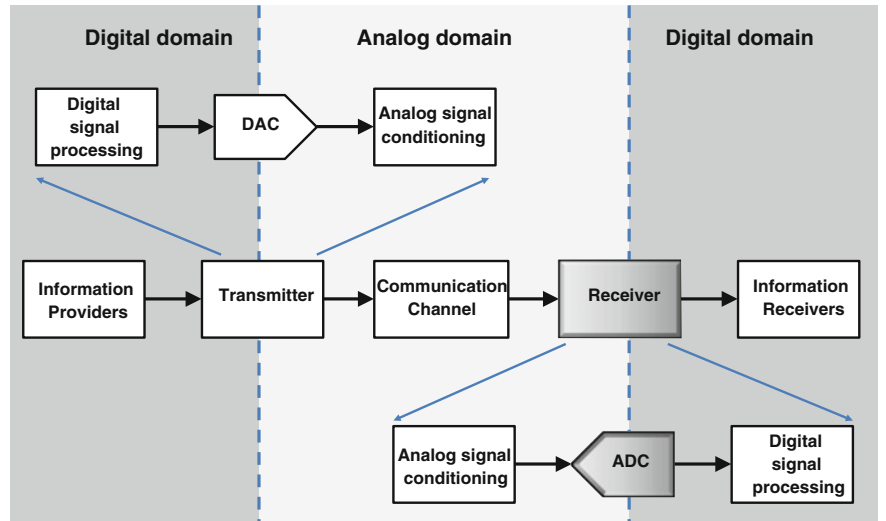


Fig. 2.2 Location of an ADC in a digital communication system

technology, the cost per digital function goes down exponentially. More and more signal conditioning functions are shifted from the analog processing domain into the digital processing domain e.g. to save cost or improve flexibility of the system [4, 5]. Data converters (ADCs and DACs) become crucial building blocks and even

bottlenecks in a digital communication system [6]. Improvements of the ADC performance such as sampling rate, accuracy, and power consumption enable new system architectures and define the competitiveness of the overall solution.

## 2.2 ADC Performance Parameters

Depending on the context and applications, requirements for the ADC vary dramatically. Many parameters are used to define the performance of an ADC [1, 2, 7]. The purpose of using these parameters is to characterize the physical behavior of an ADC in order to specify, design, and verify it for targeted applications. This section reviews three key ADC parameters for digital communication systems which are conversion accuracy, bandwidth, and power.

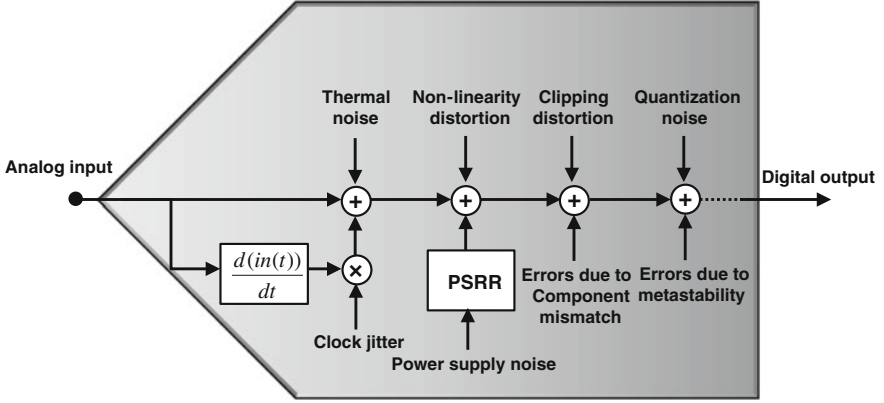
### 2.2.1 Conversion Accuracy

The conversion accuracy refers to the degree of closeness of the ADC's output value to its actual input value and can be expressed in absolute or relative terms [2]. Ideally, the conversion accuracy is only limited by the ADC's references, the number of quantization levels and their spacing which decides how small the conversion error can be. In reality, the conversion error is always larger due to physical imperfections of electronic components which introduce noise and distortion to the signal. An abstract model of an ADC with typically encountered error sources is drawn in Fig. 2.3 to show what affects the conversion accuracy.

The degradation of conversion accuracy due to these errors can be quantified by static and dynamic performance parameters [1, 2].

The static performance of an ADC is typically quantified by offset error, gain error, the differential non-linearity (DNL) error and integral non-linearity (INL) error [2]. The DNL is defined as the difference after gain and offset correction between the actual step width and the ideal value of one least significant bit (LSB). The INL is defined as the deviations of the values on the actual transfer function from a straight line. The DNL and INL errors are caused by component mismatch due to fabrication process variations, mechanical stress, temperature gradients across the circuit and operation conditions.

The dynamic performance of an ADC is normally quantified by signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), effective number of bits (ENOB), total harmonic distortion (THD), spurious free dynamic range (SFDR), inter-modulation distortion (IMD), and noise power ratio (NPR) [7]. Degradation of the dynamic performance of an ADC is contributed not only by static errors, but also by noise and signal dependent non-idealities, such as thermal noise, clock jitter, power supply noise, cross-talk, comparator metastability, dynamic settling



**Fig. 2.3** An abstract model of an ADC with typical error sources

and non-linear transfer functions of internal circuit blocks, and so on. Depending on the actual implementation, one of them can be the dominant error source.

Among the above mentioned specifications, SNDR is one of the widely used specifications for comparing the conversion accuracy among different ADCs as all noise and distortion components that affect the conversion accuracy are included [7]. The SNDR is defined as:

$$SNDR = \frac{P_{signal}}{P_{distortion} + P_{quantization\_noise} + P_{thermal\_noise} + P_{jitter\_noise} + P_{other\_noise}} \quad (2.1)$$

$\downarrow$   
Distortion

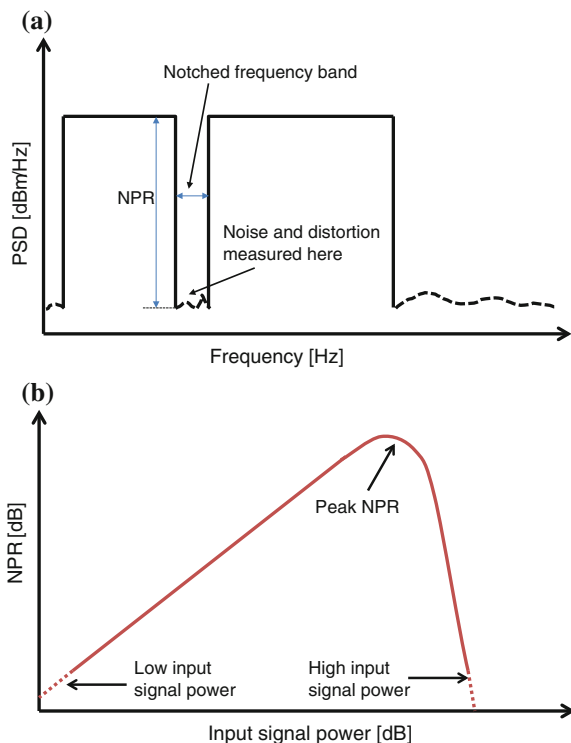
$\underbrace{\hspace{15em}}$   
Total noise power

where  $P_{signal}$  is the average input signal power,  $P_{distortion}$  is the total distortion power, and  $P_{quantization}$ ,  $P_{thermal}$ ,  $P_{jitter}$  and  $P_{other}$  are quantization, thermal, jitter and other noise power respectively. In most of the publications, the SNDR is measured using a single sinusoidal signal with full scale power as an excitation. The SNDR depends on both the amplitude and frequency of the signal since some of the error sources such as nonlinear distortion and clock jitter are input signal dependent, as shown in the Eq. 2.1.

In Eq. 2.1, noise and nonlinear distortion show equal contribution to the value of the SNDR. However, they can have very different impact on the performance of a specific system. Some systems are more sensitive to the nonlinear distortion, such as radar and GSM base station receivers; while some systems are more sensitive to noise, such as spread spectrum receivers. In these systems, specifying the conversion accuracy of the ADC separately with the SNR and SFDR is more appropriate than with the SNDR.

For communication systems adopting broadband multi-channel or multi-carrier transmission techniques, such as MC-CDMA, LTE, WiMAX, ADSL, and broadband cable modem, the actual signal that the ADC processes has very different properties compared to that of a single sinusoid. Using a simple sinusoid signal as an excitation to characterize the conversion accuracy of an ADC does not give an accurate representation of the real-world condition in these applications. For such systems, NPR testing provides an accurate measure of the noise and distortion performance of an ADC in a more realistic condition of a broadband system [2, 7, 8]. Instead of using a single sinusoid signal, a test signal, comprised of band-limited flat Gaussian noise to the frequency range of interest and with a narrow band (channel) of the noise deleted by a notch filters or other means, is used as an excitation for the NPR testing. The NPR is proven to be a more appropriate performance parameter and has gained popularity in characterizing broadband systems [7, 8]. Figure 2.4a shows an example of an NPR test signal in the frequency domain. The NPR is defined by the ratio of signal power measured in a certain frequency band to the combined noise and distortion power measured inside the notched frequency band (both frequency bands having equal bandwidth), as illustrated in Fig. 2.4a. The noise and distortion power measured inside the notched frequency band reveals the amount of noise and distortion caused by the ADC to the notched frequency band. In case the power spectral density of the signal is flat, it gives the same value as the ratio

**Fig. 2.4** **a** An example of a NPR test signal in the frequency domain; **b** NPR as a function of the test signal power



of the average power spectral density of the signal outside the notched frequency band to the average power spectral density inside the notched band as it is defined in [7]. The NPR is measured at the output of the ADC as the test signal is swept across a power range. Figure 2.4b shows a plot of NPR as a function of the test signal power.

The NPR is calculated, in decibels, from:

$$NPR = 10 \log_{10} \left( \frac{P_{No}}{P_{Ni}} \Big|_{in \text{ equal } BW} \right) dB = 10 \log_{10} \left( \frac{PSD_{No}}{PSD_{Ni}} \right) dB \quad (2.2)$$

where  $P_{No}$  and  $P_{Ni}$  are the power measured outside and inside the notched frequency band respectively, and  $PSD_{Ni}$  and  $PSD_{No}$  are the average power spectral density inside and outside the notched band respectively [7].

### 2.2.2 Bandwidth

Three commonly used definitions of the ADC bandwidth are the Nyquist bandwidth, the analog input bandwidth, and the effective resolution bandwidth (ERBW) [7]. The Nyquist bandwidth equals half of the sampling rate of the ADC. The sample rate ( $f_s$ ) is the frequency at which the ADC converts the analog input waveform to digital data. The Nyquist theorem explains the relationship between the sample rate and the frequency content of the measured signal [9, 10]. The input signal bandwidth must be smaller than the Nyquist bandwidth to avoid aliasing [9, 10]. The analog input bandwidth is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The ERBW is defined as the input frequency at which the SNDR drops 3 dB (or ENOB 1/2 bit) below its low frequency value [7]. An ADC used for sub-sampling applications is desired to have an analog input bandwidth and ERBW larger than its Nyquist bandwidth.

### 2.2.3 Power

Power consumption is also an important parameter of an ADC. It is a primary design constraint for applications that have limited available energy such as devices powered by batteries. Too much power consumption can also lead to a requirement for a heatsink or fan for the IC, which will increase the total system cost. The excessive heat caused by high power dissipation can have negative effect on the reliability of the IC and prevent the integration of more circuit blocks on the same die. Consequently, most designs nowadays are trying to either maximize the performance under a certain power budget or minimize the power consumption for a target performance.

### 2.2.4 ADC Figure-of-Merit

Various ADC parameters (including parameters mentioned above and others) can be combined to get one single number for the purpose of evaluating ADCs for a certain product or comparing scientific achievement. Numerous ADC figures-of-merits (FOMs) have been proposed and a classification of them can be found in [11]. Two most widely used ADC FOMs in scientific publications are the ‘Walden FOM’ (FOM<sub>1</sub>) and the ‘Schreier FOM’ (FOM<sub>2</sub>) [12, 13]:

$$FOM_1 = \frac{P}{\min\{f_s, 2 \times ERBW\} \times 2^{ENOB}} \quad (2.3)$$

$$FOM_2 = SNDR(dB) + 10 \log_{10} \left( \frac{BW}{P} \right) \quad (2.4)$$

If FOM<sub>2</sub> is rewritten in linear form and inverted, it is then proportional to

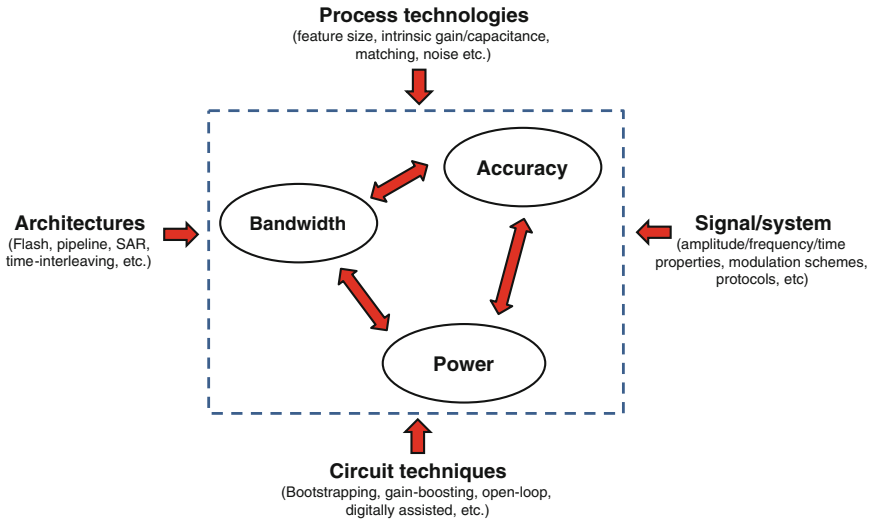
$$\frac{P}{BW \times 2^{2 \times ENOB}} \quad (2.5)$$

which becomes the so called “Thermal FOM” [14]. Comparing Eqs. 2.3 and 2.4, we can clearly see the difference lies in the relative weight given to the conversion accuracy performance. Equation 2.3 implies that the power consumption increases by 2 times when doubling the conversion accuracy (one extra ENOB) which is based on curve-fitting of empirical data [12]; while Eqs. 2.4 and 2.5 account for the fact that due to thermal noise limitations, achieving twice the conversion accuracy requires 4 times increase of the power consumption.

## 2.3 ADC Performance Limitations and Trends

As illustrated in Fig. 2.5, key factors that influence the ADC performance (in terms of bandwidth, accuracy, and power consumption) are the process technology, ADC architecture, circuit design techniques, and signal/system properties. Limitations of the available process technology, such as minimum feature size, reliability issues, intrinsic capacitance, as well as device imperfections (leakage, mismatch, noise, nonlinearity, etc.), require proper ADC architectures and innovative circuit design techniques to reduce their impacts on the ADC performance.

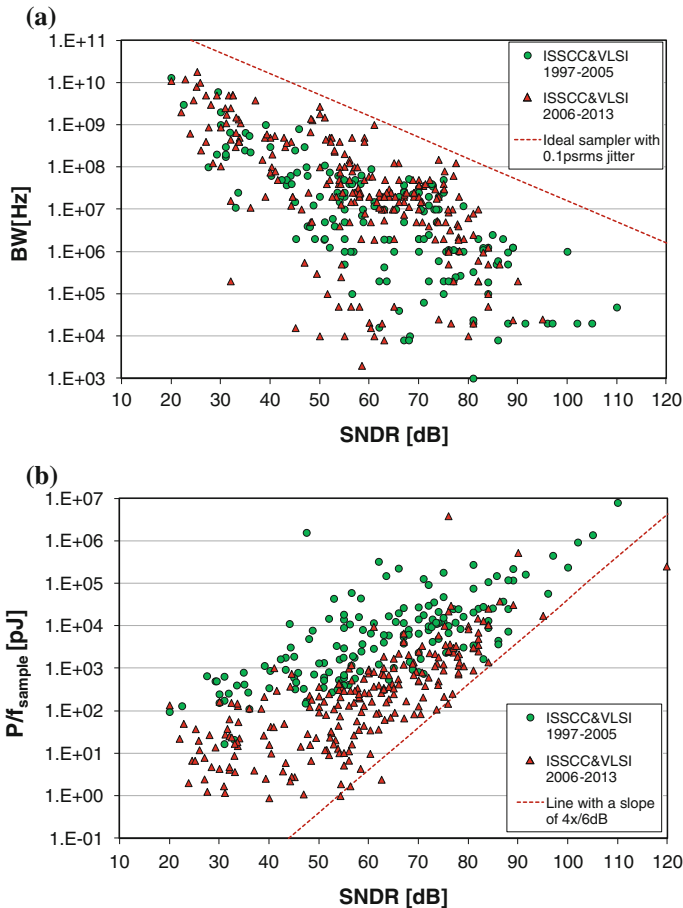
There is also a trade-off between conversion accuracy, bandwidth and power in designing ADCs using any process technology, improving one of the ADC parameters will mostly likely result in degradation of the other two parameters [15, 16]. The challenge lies in improving all these parameters simultaneously. As discussed in Sect. 2.2, the conversion accuracy of an ADC is limited by many error sources. For those static errors and some of the dynamic errors, numerous



**Fig. 2.5** Trade-off between conversion accuracy, speed and power in ADC design and key factors' impact on the overall ADC performance

calibration techniques have been developed to minimize them with little degradation of other ADC performance parameters. Many calibration techniques nowadays exploit the digital signal processing capabilities to “assist” analog circuits of the ADC for accuracy and bandwidth improvement with lower overall power consumption [17, 18]. These techniques measure and correct imperfections of devices and circuits, and they are able to improve the conversion accuracy or sampling speed of an ADC with smaller power overhead compared to the ones without using these techniques. ADC calibrations can be done at startup or in the background without affecting normal operation. However, when the conversion accuracy is limited by random noise, such as thermal noise and clock jitter, improving the conversion accuracy relies on using larger devices to minimize the noise power or increasing the converted signal power. The approach of using larger devices, which refers to the conventional approach mentioned in this book, increases the capacitive loading of the circuit nodes and leads to a higher power consumption for achieving a targeted bandwidth. The required power would actually quadruple per bit increase to maintain the same bandwidth by using this approach to lower the thermal noise power [19]. When the conversion accuracy is limited by quantization noise, the oversample and average technique can be used to improve the conversion accuracy effectively [20], but it requires the ADC to operate at a sampling rate significantly higher than the bandwidth of the signal. When the sampling speed of an ADC exceeds a certain limit of operation frequency, linear increase of the sampling rate further requires an exponential increase of its power consumption [21]. Therefore, the conversion accuracy and bandwidth limitations of an ADC are mainly set by thermal noise, clock jitter and intrinsic capacitance of devices.





**Fig. 2.6** **a** ADC BW versus SNDR, **b** ADC energy efficiency ( $P/f_{\text{sample}}$ ) versus SNDR. The experimental data includes ADCs published in ISSCC and VLSI symposium between 1997 and 2013 [22]

In the following section, recent published state-of-the-art ADCs are studied to find the current performance boundary set by available process technologies, circuit design techniques and architectures. The experimental data used for this purpose includes ADCs published in ISSCC and VLSI Symposium between 1997 and 2013 [22].

Figure 2.6a plots the bandwidth of the ADCs against the SNDR. From this figure, we can see that the achievable bandwidth of the ADCs decreases with higher SNDR. We can also observe that there exists a practical boundary for the achievable bandwidth of state-of-the-art ADCs at different SNDR. As shown in Fig. 2.6a, this boundary is close to the dashed line that represents the performance of an ideal sampler with 0.1 ps clock jitter. ADCs data points close to this line represent what is

at present feasible to design. It also implies that having a data point above this line is very challenging or simply not yet feasible with current technologies and techniques. This confirms one of the challenges mentioned above of achieving both higher conversion accuracy and higher bandwidth at the same time.

Figure 2.6b plots the energy efficiency against the SNDR. From this figure, we can observe that there also exists a practical boundary of the achievable conversion efficiency at different SNDR. For ADCs with SNDR greater than 55 dB, this boundary follows a dashed line with a slope of close to 4 times per 6 dB which is the so called ‘architecture frontier’ [23]. The slope of the dashed line corresponds to the fundamental thermal energy trade-off (power quadruples per 6 dB increase in SNR), and ADCs near this line shown in the figure tend to be thermal noise limited. Observed from this figure, the energy efficiency of the state-of-the-art ADCs with SNDR less than 55 dB on the boundary stay almost the same ( $\sim 1\text{pJ}$ ). With advance in technology, circuit design and architecture innovation, future ADCs with low SNDR will also become thermal noise limited design and get close to the dashed line.

Comparing ADCs published before and after 2006, we observe a slow improvement in the bandwidth-conversion-accuracy product in Fig. 2.6a and a substantial improvement in the energy efficiency of ADC in Fig. 2.6b. The energy efficiency has improved by about 100 times over the last 8 years for ADCs with low SNDR (less than 60 dB). This is mostly enabled by the continuous down scaling of the process technology (minimize device and wiring intrinsic capacitance) and innovations in circuit techniques. As current state-of-art ADCs with SNDR higher than 55 dB are mostly limited by thermal noise, the energy efficiency of these ADCs does not benefit from the process technology scaling due to the lower supply voltage [20, 23].

As observed from publications, state-of-the-art ADCs are well optimized nowadays. To meet the ever-increasing demand for better conversion accuracy, bandwidth and power efficiency, further improvements need to be achieved from process technology improvements, new circuit design techniques, innovative architectures, or signal/system-aware design approaches. Low-to-moderate resolution and high-speed ADCs will continuously benefit from the down-scaling and better optimized process technology (e.g. SOI, FinFET) until they are also limited by thermal noise. For thermal noise limited ADCs, innovative architectures and circuit design techniques to boost the input signal range are an effective way to improve both the bandwidth and energy efficiency which will be discussed in detail in Chap. 3.

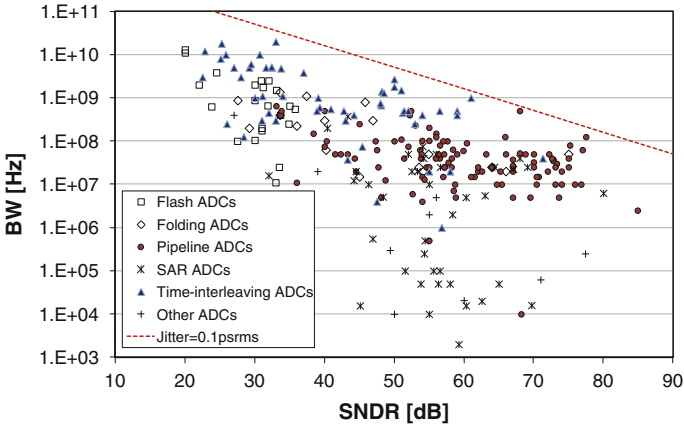
In the following sections, an overview of classical ADC architectures is given and an ADC design approach based on exploiting the signal and system properties is also discussed.

## 2.4 ADC Architectures

Many ADC architectures have been developed over the years. In general, ADCs are divided into two broad categories: Nyquist-rate ADCs and over-sampling ADCs (mainly referred to sigma-delta modulator ADCs). The Nyquist-rate ADCs are the

**Table 2.1** Classification of Nyquist-rate ADC architectures

Algorithms	ADC architectures
Parallel search	Flash ADC
Sequential search	Folding ADC
• Linear search	Integrating ADC (single/multi-slop)
• Binary search	Successive approximation ADC
• Sub-binary search	Cyclic ADC
	Sub-ranging ADC
	Pipeline ADC



**Fig. 2.7** Performance space of different Nyquist-rate ADC architectures (The experimental data includes ADCs published in ISSCC and VLSI symposium between 1997 and 2013 [22])

main focus of this book. Popular Nyquist-rate ADC architectures are listed in Table 2.1 and performance space of different Nyquist-rate ADC architectures is shown in Fig. 2.7. They can be categorized into two groups from the algorithmic point of view, namely parallel search ADCs and sequential search ADCs, or a combination of the two.

The main advantage of parallel search ADCs is in conversion speed, while for sequential search ADCs, their main advantage lies in hardware efficiency, which leads to smaller area for a similar conversion accuracy target [23]. Multiple parallel or sequential search ADCs can be placed in parallel and operate in a time-interleaving fashion to increase sampling speed which refer to the time-interleaving ADC architecture [24]. In the physical implementation, the vast variety of ADC architectures is realized by some basic circuit building blocks, such as track-and-hold, amplifiers, comparators, and reference circuit.

There are some important factors to be considered when comparing different ADC architectures for applications with certain performance requirements, which are conversion time (latency), design complexity, area and power [23].

Conversion time is defined as the time an ADC takes to complete a conversion; it is also specified as latency. The conversion time of a flash ADC does not change with the increase of the number of voltage levels it needs to distinguish. The latency of a SAR ADC or pipelined ADC (1-bit per stage) increases linearly with the increase of its number of bits of resolution. For an integrating ADC, the conversion time increases exponentially with the increase in its number of bits of resolution.

The design complexity of an ADC with certain architecture varies with its performance requirements. Figure 2.7 shows the performance space in terms of bandwidth and SNDR of different ADC architectures based on empirical data. In general, Flash ADCs are suitable architecture for high bandwidth and low resolution applications, SAR ADCs for low bandwidth and moderate-to-high resolution applications, Pipeline ADCs for moderate bandwidth and moderate-to-high resolution applications, and Time-interleaving ADCs for low-to-moderate resolution and very high bandwidth applications. From Fig. 2.7, we can also observe that the performance space of different ADC architectures have a good deal of overlap, this means that multiple architectures can be suitable to meet the target requirements. It is also possible to extend the performance space of certain architectures, but the complexity to design their circuit building blocks to meet the target performance would increase substantially and one architecture may become less competitive compared to other architectures. For example, the flash ADC architecture is suitable for applications requiring very high sampling speeds and low latency but with low resolution. However, selecting the flash ADC architecture to build an ADC with 12 bits resolution and moderate bandwidth is not appropriate. As the number of comparators, the requirements on the comparators and reference, and the associated input capacitance increases exponentially with every additional bit, the difficulty to maintain a large bandwidth and reduce the effect of stronger kick back will result in high design complexity. Instead, achieving such performance with the pipeline architecture is less challenging. Calibration techniques can be used effectively to extend the performance space of certain architectures, but the complexity of calibration circuits increases with the higher performance requirements which should be carefully considered.

Power consumption and die size are also important factors of choosing ADC architectures. For flash converters, every bit increase in resolution requires about 8 times increase in the die size of the ADC core circuitry (number of comparators doubles and each comparator quadruples in size to meet matching requirement). Consequently, the power of the ADC will also increase by 8 times. In contrast, the die size of a SAR, pipelined, or sigma-delta ADC increases linearly with an increase in resolution; while for an integrating ADC, its core die size will not change with an increase in resolution. It is well known that the increase in die size and power consumption increases cost. Trimming and calibration can be used to improve die size and energy efficiency as explained in the previous section. The minimum power required to achieve a certain conversion accuracy and sampling frequency will eventually be limited by thermal noise and clock jitter.

## 2.5 Exploiting Signal Properties

As discussed in Sect. 2.2, designing ADCs with high conversion accuracy, high sampling speed and low power consumption at the same time is challenging. Recent publications show slow improvement of the ADC performance as today's state-of-the-art ADCs are highly optimized, this is due to limitations of current available process technologies, circuit design approaches and architectures. In order to cope with the ever increasing demand for better ADC performance, it is worthwhile to exploit alternative design approaches. One promising approach is the so called 'signal-aware', 'system-aware' or 'application-aware' design approach [25–27]. Since most of the ADCs nowadays are designed for a specified application, there is much a priori knowledge of the signal and the system available. For example, in communication systems, how source data is encoded and modulated are normally known in advance. This knowledge can be exploited for the design of an optimized ADC for a target application. There are two advantages of this approach:

- The power consumption of the ADC can be reduced without compromising system performance by tailoring the ADC performance to the signal/system properties;
- A better system performance can be enabled without the need of a better ADC which may not be available currently.

Main purpose of the ADC is to digitize the information-bearing waveforms with minimum loss of the information it is intended to convey. The information that needs to be extracted is embedded in one or more properties of the analog waveform such as amplitude, frequency, and phase; the waveform may be corrupted by noise and interfering signals during transmission. Therefore, the a priori knowledge of some properties of the signal waveform (e.g. their probability density function, sparsity, time activities) can be exploited and mapped to the performance requirements of the ADC where opportunities can be found.

The idea of exploiting signal properties to optimize the design of ADCs has been applied to various previous works and shows promising results. In the following sections, various ADC architectures that utilized signal information to improve performance are introduced. Analysis and summary of these existing solutions are given.

### Amplitude properties

ADCs are normally designed with uniformly distributed quantization levels. This is only optimal (in terms of quantization noise) when the input signal amplitudes are uniformly distributed. For many applications, the signal amplitude distribution is far from uniform. When knowledge of the amplitude probability distribution function of the signal is available, the quantization levels in the ADC can be optimized according to the probability distribution function of the signal amplitudes to reduce quantization noise [28, 29]. The resulting ADC will have non-uniform distributed quantization levels, having finer quantization for signal amplitudes that have higher probability of occurrence to improve the overall signal-to-quantization-noise-ratio

(SQNR) and bit-error-rate (BER) with a given number of quantization levels. The Lloyd-Max's algorithm was presented in [28] to find the optimal set of quantization thresholds to minimize quantization noise. This approach can be very useful for low resolution ADCs where the quantization noise is the dominant noise source.

Another example of exploiting the signal amplitude property is the 'companding ADC' [30]. As shown in Fig. 2.8, it is realized with three functional building blocks: a signal compressor, a conventional ADC, and a signal expander that inverts the compressor function. With this architecture, a conventional ADC can be used instead of designing an ADC with non-uniform distributed quantization levels to achieve the same function. Ideally, the signal amplitude distribution can be converted into a uniform distribution by the 'compressor' to exploit the dynamic range of the ADC optimally, and after the conversion by the ADC, the signal is restored in the digital domain by the 'expander'. In this way, the restored signal can have a higher SQNR as well as dynamic range compared to a conventional ADC with the same amount of quantization levels for an input signal with non-uniformly distributed amplitudes. In practice, designing a 'compressor' which has a stable non-linear transfer function and achieving good matching between the analog 'compressor' and digital 'expander' is very challenging, therefore a piecewise linear approach is normally adopted [31].

### Spectral properties

In many applications, the signals of interest can have large sparsity in the frequency domain which means the actual spectrum occupied by signals is much smaller than the total bandwidth of the spectrum needed to capture at any given time instant. In these situations, sampling at two times the highest signal frequency is inefficient. Such signals can be reconstructed (via a compressed sensing algorithm) with significantly fewer samples than with Nyquist sampling [32]. Therefore, the average sampling rate of the ADC can be relaxed and the amount of output data is reduced. This approach has been demonstrated in various works [33, 34]. For example, [34] applied this approach to build a sampler for wideband spectrally-sparse environments and demonstrated the capability of digitizing an 800 MHz to 2 GHz band with an average sample rate of only 236 Msps which greatly reduced the sample rate requirement of the ADC and power consumption.

Another example of exploiting the spectral properties to enhance the ADC performance is an ADC architecture employing interference detection and cancellation. A mixed-signal architecture with a 'forward interference rejection' approach is presented in [35], which is suitable for processing a weak signal with strong interferences as shown in Fig. 2.9. This architecture contains two low dynamic

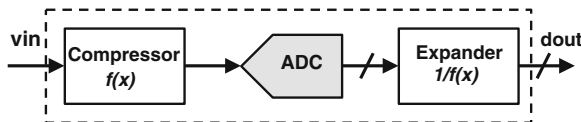
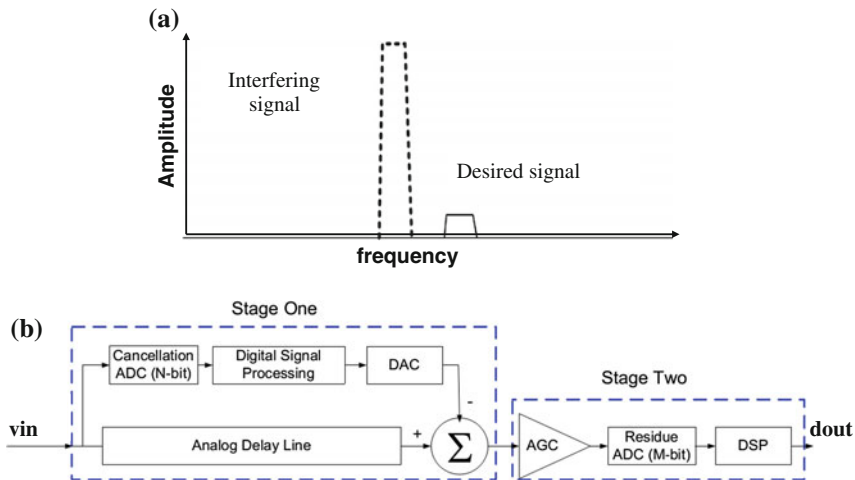
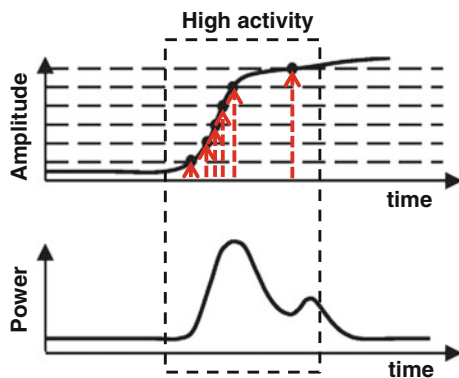


Fig. 2.8 Block diagram of a “companding ADC”



**Fig. 2.9** **a** Spectrum of a weak desired signal coexisting with a strong interfering signal, **b** ADC architecture employing interference detection and cancellation [35]

**Fig. 2.10** Event-based sampling and estimation of corresponding ADC power dissipation [39]



range ADCs and they can effectively act as a high dynamic range ADC in terms of the ability to resolve a small desired signal in the presence of a large interfering signal. By solving some practical implementation issues of this architecture (delay matching between two signal paths in stage one, signal subtraction and reconstruction, etc.), low dynamic range ADCs can be used to achieve the required system performance, which would otherwise require a high dynamic range ADC and consume significant more power. A programmable notch filter (with control circuitry) can also be used in stage one to achieve the same purpose [36].

### Time domain properties

ADCs are normally designed to sample at a constant rate which is based on the worst possible case of the considered applications. Rather than sampling the signals

at a constant high rate, the ADC can be designed to adapt its sampling rate according to the activity of the signal [37–41]. Therefore, the power consumption of the ADC can become proportional to the activity of the analog input, as illustrated in Fig. 2.10. For input signals that have burst-like properties in time domain, such as ECG signals, ultrasound signal and UWB impulse signals, significant power can be saved. This approach has been demonstrated in [39–41]. This type of ADCs is commonly referred to as a ‘level-crossing’ or ‘event-driven’ ADC [38, 41].

## 2.6 Conclusion

In this chapter, the analog-to-digital conversion process and ADC parameters were discussed. The ADC performance limitations, trade-offs between key ADC parameters (conversion accuracy, bandwidth and power consumption), and ADC performance trends were addressed.

As today’s state-of-the-art ADCs are highly optimized due to current available process technologies, circuit design approaches and architectures, it is a challenge to keep pace with the ever increasing demand for more advanced ADCs. However, as most of the ADCs nowadays are designed for a specific application, it is worthwhile to exploit signal and system properties which are a priori knowledge to further enhance the ADC performance. We conclude that this so-called ‘signal-aware’, ‘system-aware’ or ‘application-aware’ ADC design approach, as discussed in Sect. 2.5, is promising for this purpose.

In the following chapters of this book, this concept will be applied to the design of power efficient ADCs for broadband multicarrier systems. In Chap. 3, statistical amplitude properties of multi-carrier signals are exploited and a parallel-sampling ADC architecture for broadband multi-carrier signals is introduced and analyzed.

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