Contents

1 Introduction 1
1.1 An Introduction to Chaos 1
1.1.1 A Brief History of Chaos 1
1.1.2 An Application of Chaos 8
1.2 An Introduction to Field Programmable Gate Arrays 9
1.2.1 History of FPGAs 9
1.2.2 Why FPGAs? 10
1.3 Some Basic Mathematical Concepts 11
1.3.1 Linear Versus Nonlinear Equations 11
1.3.2 Linear Versus Nonlinear Dynamics 14
1.3.3 Fixed (Equilibrium) Points 18
1.3.4 System Behaviour Near Fixed Points 20
1.4 Conclusions 24
Problems 25
Lab 1: Introduction to MATLAB and Simulink 27
References 28

2 Designing Hardware for FPGAs 29
2.1 The FPGA Development Flow 29
2.2 The Architecture of an FPGA 30
2.3 An Overview of the Hardware and Software Development Platform 33
2.3.1 An Overview of the Terasic DE2-115 Development Board 33
2.3.2 VHDL Primer and Using the Quartus Toolset 37
2.3.3 Audio Codec Interfacing 45
2.4 Timing Closure 49
2.5 Conclusions 50
Problems 50
Lab 2: Introduction to Altera FPGA Tools 52
References 52

3 Chaotic ODEs: FPGA Examples 55
3.1 Euler's Method 55
3.2 Specifying Chaotic Systems for FPGAs Using DSP Builder 56
3.2.1 The Lorenz System 56
3.3 Introduction to Functional Simulation and In-System Debugging 61
3.4 Functional Simulation of Chaotic Systems. 62
3.5 Debugging Using SignalTap 65
3.5.1 General Concepts—An Illustration Using a Simple Example 65
3.5.2 Debugging the Chen System Using SignalTap. 67
3.6 Hardware Debugging Concepts 67
3.6.1 Observing a Problem 68
3.6.2 Identifying the Problem 69
3.6.3 Sources of Errors in VHDL Designs 70
3.6.4 Design Procedure. 71
3.7 Another Example—A Highly Complex Attractor System 72
3.8 Conclusions. 77
Problems 77
Lab 3: ModelSim Simulation, In-System Debugging and Physical Realization of the Muthuswamy-Chua System . . . 79
References 80

4 Bifurcations 81
4.1 The Concept of Bifurcations 81
4.2 Routes to Chaos 82
4.2.1 Period-Doubling Route to Chaos 82
4.2.2 Period-Adding Route to Chaos 83
4.2.3 Quasi-Periodic Route to Chaos 85
4.2.4 Intermittency Route to Chaos 85
4.2.5 Chaotic Transients and Crisis 87
4.3 Bifurcation Experiments with an FPGA 91
4.3.1 Period-Doubling Route to Chaos 92
4.3.2 Period-Adding Route to Chaos 93
4.3.3 Quasi-Periodic Route to Chaos 96
4.4 Conclusions. 100
Problems 100
Lab 4: Displaying Bifurcation Parameter(s) on the LCD 101
References 102

5 Chaotic DDEs: FPGA Examples and Synchronization Applications 103
5.1 An Introduction to Time Delay Systems 103

5.2 Simulating DDEs in Simulink 104
5.3 FPGA Realization of DDEs. 105
5.4 Applications of (Time Delayed) Chaotic Systems—Synchronization 113
5.4.1 Unidirectional Coupling 114
5.4.2 Bidirectional Coupling 115
5.5 Conclusions. 119
Problems 119
Lab 5: The Lang-Kobayashi Chaotic Delay Differential Equation. 120
References 121

Appendix A: Introduction to MATLAB and Simulink 123

Appendix B: Chapter 1 MATLAB Code 131

Appendix C: Chapter 2 VHDL, Simulink DSP Builder and SDC File 135

Appendix D: Chapter 3 VHDL, MATLAB Code and ModelSim Scripts 149

Appendix E: Chapter 4 MATLAB Code, VHDL and ModelSim Scripts 163

Appendix F: Chapter 5 VHDL 193

Glossary 217

Solutions 219

Springer

http://www.springer.com/978-3-319-18104-2

A Route to Chaos Using FPGAs
Volume I: Experimental Observations
Muthuswamy, B.; Banerjee, S.
2015, XXIII, 219 p. 131 illus., Hardcover
ISBN: 978-3-319-18104-2