

Chapter 2

Recent Research and Development Activities of Three-Dimensional Integration Technology

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2.1 Recent Announcement of Research and Development Activities

Since 2013, research and development activities in three-dimensional (3D) integration technology have been accelerating. The themes announced in 2013 and 2014 are described below and shown in chronological order in Figs. 2.1, 2.2, 2.3, 2.4.

(2013/Jan) Novati Technologies Licenses Ziptronix's Direct Oxide Bonding and Direct Bond Interconnect Patented Technologies [1].

"Ziptronix, Inc. has signed a licensing agreement with Novati Technologies, Inc. for the use of its patents covering direct bonding technology, ZiBond and DBI. We believe that Ziptronix's patented direct bonding technology enables the industry's best performance for applications such as 3D memory, BSI image sensors and a developing host of other applications."

(2013/Jan) TORKI K., Presentation Slide (2013), 3D-IC Integration, CMP annual users meeting, 17 January 2013, PARIS, "A very collaborative work has been achieved and still ongoing between the partening CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU" [2].

(2013/Jan) STATS ChipPAC and UMC Unveil World's First 3D IC Developed under an Open Ecosystem Model [3].

"STATS ChipPAC and UMC announced the world's first demonstration of TSV-enabled 3D IC chip stacking technology developed under an open ecosystem collaboration. The 3D chip stack, consisting of a Wide I/O memory test chip stacked upon a TSV-embedded 28 nm processor test chip, successfully reached a major milestone on package-level reliability assessment."

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2013



Fig. 2.1 Worldwide research and development activities in January–May 2013. *CMC* chemical–mechanical polishing, *MOSIS* metal oxide semiconductor implementation service, *CMC* commercial metal company, *HEP* high-energy physics, *NCSU* North Carolina State University, *UMC* United Microelectronics Corporation, *CIS CMOS* image sensor, *UTAC* United Test and Assembly Center Ltd, *JEDEC* Joint Electron Device Engineering Council, *TSV* through-silicon via, *IC* integrated circuit

2013

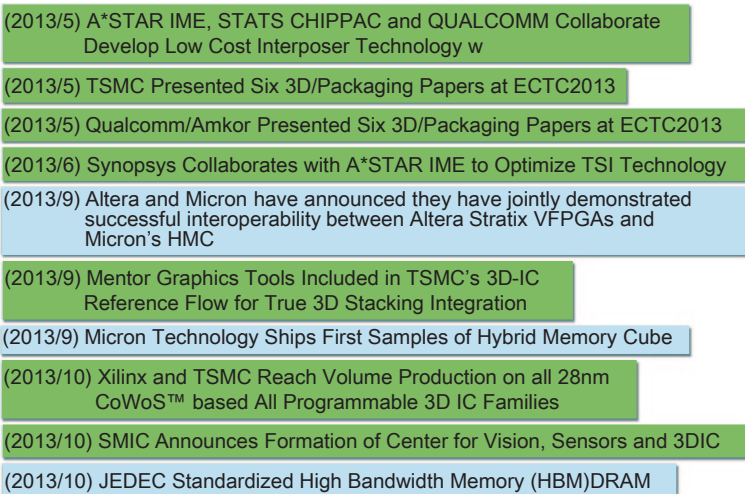


Fig. 2.2 Worldwide research and development activities in June–October 2013. *IME* Institute of Microelectronics, *TSI* top surface imaging, *VFPGA* virtual field-programmable gate array, *HMC* hybrid memory cube, *TSMC* Taiwan Semiconductor Manufacturing Company, *JEDEC* Joint Electron Device Engineering Council, *HBM* high bandwidth memory, *DRAM* dynamic random-access memory

2013

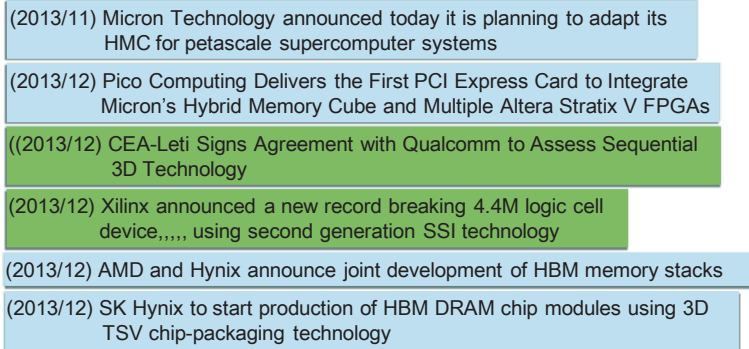


Fig. 2.3 Worldwide research and development activities in November–December 2013. *IC* integrated circuit, *PCI* peripheral component interconnect, *VFPGA* virtual field-programmable gate array, *AMD* advanced micro device, *HBM* high bandwidth memory, *DRAM* dynamic random-access memory, *TSV* through-silicon via, *SMIC* Semiconductor Manufacturing International Corporation, *SSI* stacked silicon integration

2014

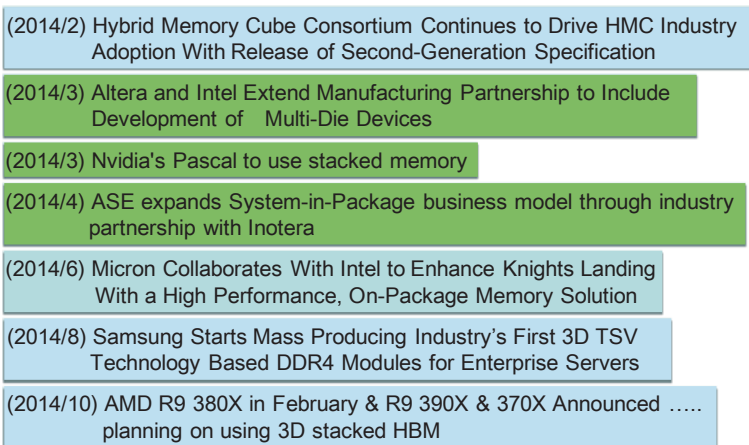


Fig. 2.4 Worldwide research and development activities in 2014. *HMC* hybrid memory cube, *ASE* Advanced Semiconductor Engineering, *TSV* through-silicon via, *AMD* advanced micro device, *HBM* high bandwidth memory, *DDR* double data rate

(2013/Feb) Sony and Olympus presented new CIS technology at ISSCC 2013 [4].

“The Sony ISX014 8MP sensor features 1.12 μm pixels and integrated high speed ISP. The pixel layer and logic layer part are manufactured as separate chips and stacked by using TSVs. Previously the pixel and logic circuit of Sony’s back side illuminated (BSI) CMOS image sensor were formed during the same fabrication process.”

(2013/Mar) Singapore's UTAC to Co-Develop 2.5D Through-Silicon-Interposer With A*STAR'S Institute of Microelectronics for Volume Manufacturing [5].

"A*STAR (IME) and UTAC announced a collaboration to develop a 2.5D Through-Silicon-Interposer (TSI) platform which will enable UTAC to join the scarce list of suppliers in offering fine-pitch 2.5D TSI packaging solutions."

(2013/Apr) GlobalFoundries Demonstrates 3D TSV Capabilities on 20 nm Technology [6].

"GLOBALFOUNDRIES announced the accomplishment of a key milestone in its strategy to enable 3D stacking of chips for next-generation mobile and consumer applications. At its Fab 8 campus in Saratoga County, N.Y., the company has demonstrated its first functional 20 nm silicon wafers with integrated Through-Silicon Vias (TSVs)."

(2013/May) Mentor and Tezzaron Optimize Calibre 3DSTACK for 2.5/3DICs [7].

"Mentor Graphics and Tezzaron Semiconductor announced they are collaborating to integrate the Mentor® Calibre® 3DSTACK product into Tezzaron's 3D-IC offerings. The new integration will focus on fast, automated verification of die-to-die interactions in 2.5D and 3D stacked die configurations by verifying individual dies in the usual manner, while verifying die-to-die interfaces in a separate procedure with specialized automation features."

(2013/May) UMC Establishes its Specialty Technology Center of Excellence in Singapore [8].

"UMC announced that the company has established Fab 12i in Singapore as its 'Center of Excellence' to spearhead the company's R&D and manufacturing for advanced specialty process technologies. The Center of Excellence was set up with an initial investment of US \$ 110 million, and will undertake R&D collaborations with local research institutes such as Singapore's Institute of Microelectronics. Technologies being developed include CMOS image sensor backside illumination, embedded memory, high voltage applications and TSV (through silicon via) connections."

(2013/May) A*STAR IME, STATS CHIPPAC and QUALCOMM Collaborate Develop Low Cost Interposer Technology [9].

"A*STAR Institute of Microelectronics (IME), Qualcomm Technologies Inc., and STATS ChipPAC announced a collaboration to develop technology building blocks for Low Cost Interposers (LCI) for 2.5D ICs in May 2013."

(2013/May) TSMC Presented 3D technology at ECTC2013 "Reliability Characterization of Chip-on-Wafer-on-Substrate (CoWoS) 3D IC Integration Technology" [10].

"TSMC reported 'CoWoS' 3D IC integration technology has been developed with comprehensive reliability characterization. The copper interconnect reliability of silicon interposer are not impacted by the TSV insertion, in terms of EM, SM, IMD TDDb, and Vbd/TDDb of MiM de-cap. μ Bump EM and TSV EM are characterized to provide a design guideline for maximum current carrying capability."

(2013/May) Qualcomm/Amkor Presented Six 3D/Packaging Papers at ECTC2013 [11, 12].

"The trial production evaluation towards utilization of TSV base three-dimensional structure package of Wide I/O memory and logic chip is progressing steadily at Qualcomm. 3D-TSV structure which stacked 28 nm generation logic device and maximum of four chips Wide I/O memory were bonded using TSV was

reported for the first time in the world. Qualcomm made the device in cooperation with U.S. Amkor Technology as an experiment.”

(2013/Jun) Synopsys Collaborates with A*STAR IME to Optimize TSI Technology [13].

“Synopsys announced that it joined Singapore’s A*STAR Institute of Microelectronics (IME)-led 2.5D TSI Consortium to provide the framework for heterogeneous 3D-IC systems using through-silicon interposer (TSI) technology.”

(2013/Sep) TSMC and Cadence Deliver 3D-IC Reference Flow for True 3D Stacking [14].

“Cadence Design Systems announced that TSMC has collaborated with Cadence to develop a 3D-IC reference flow which features innovative true 3D stacking. The flow, validated on a memory-on-logic design with a 3D stack based on a Wide I/O interface, enables multiple die integration. It incorporates TSMC 3D stacking technology and Cadence® solutions for 3D-IC, including integrated planning tools, a flexible implementation platform, and signoff and electrical/thermal analysis.”

(2013/Sep) Mentor Graphics Tools Included in TSMC’s 3D-IC Reference Flow for True 3D Stacking Integration [15].

“Mentor Graphics Corp. announced that its solutions have been validated by TSMC with a true 3D stacking test vehicle for TSMC’s 3D-IC Reference Flow. The flow expands support from silicon interposer offerings to include TSV-based, stacked die designs. Specific Mentor® offerings include capabilities for metal routing and bump implementation, multi-chip physical verification and connectivity checking, chip interface and TSV parasitics extraction, thermal simulation, and comprehensive pre- and post-package testing.”

(2013/Oct) Xilinx and TSMC Reach Volume Production on all 28 nm CoWoS™ based All Programmable 3D IC Families [16].

“Xilinx and TSMC announced production release of the Virtex®-7 HT family, the industry’s first heterogeneous 3D ICs in production. With this milestone, all Xilinx 28 nm 3D IC families are now in volume production. These 28 nm devices were developed on TSMC’s Chip-on-Wafer-on-Substrate (CoWoS™) 3D IC process that produces significant silicon scaling, power and performance benefits by integrating multiple components on a single device.”

(2013/Oct) SMIC Announces Formation of Center for Vision, Sensors and 3DIC [17].

“Semiconductor Manufacturing International Corporation (SMIC) announced today the formation of SMIC’s Center for Vision, Sensors and 3DIC (CVS3D). CVS3D consolidates and strengthens SMIC’s R&D and manufacturing capabilities for silicon-based sensors, thru-silicon-via (TSV) technology and other middle-end wafer process (MEWP) technologies.”

(2013/Dec) CEA-Leti Signs Agreement with Qualcomm to Assess Sequential 3D Technology [18].

“CEA-Leti announced an agreement with Qualcomm Technologies, Inc. to assess the feasibility and the value of Leti’s sequential 3D technology. In recent years, Leti has been actively working on a new 3D integration technology process called sequential 3D integration that enables the stacking of active layers of transistors in the third dimension. In comparison with 3D-TSV technologies, advantageously

used to stack separate die, sequential 3D technology is anticipated to process all the functions in a single semiconductor manufacturing flow.”

(2013/Dec) Xilinx will be the industry’s largest capacity doubled to 4.4 million devices logical unit [19].

“Xilinx announced owns 4.4 million logic cells Record product, its density is the industry’s highest density product Virtex ® -7 2000T more than twice, the device to make it successful in the market for two generations of high-end devices maintain a leading edge, and provide customers with a value advantage beyond process nodes VU440 using advanced 3D IC technology, the capacity on the 20 nm process node has exceeded all previous competitive 14/16 nm technology plan publicly.”

(2014/Mar) Altera and Intel Extend Manufacturing Partnership to Include Development of Multi-Die Devices [20].

“Altera Corporation and Intel Corporation today announced their collaboration on the development of multi-die devices that leverage Intel’s world-class package and assembly capabilities and Altera’s leading-edge programmable logic technology. The collaboration is an extension of the foundry relationship between Altera and Intel, in which Intel is manufacturing Altera’s Stratix® 10 FPGAs and SoC s using the 14 nm Tri-Gate process.”

(2014/Apr) ASE expands System-in-Package business model through industry partnership with Inotera [21].

“Advanced Semiconductor Engineering, Inc. announced a joint development with Inotera Memories, in a move to further strengthen ASE’s System-in-Package (SiP) capabilities. Complementing ASE’s established portfolio, Inotera will provide manufacturing services for silicon interposer, an interconnect device on silicon wafer for 2.5D IC solutions. This collaborative business model, combining Inotera’s strong front-end wafer processing capability with ASE’s advanced IC packaging and testing technology, will serve to deliver solutions featuring high quality, stable yield and an efficient cost structure, to a broader customer base and market.”

We now describe research and development activities that are expected to lead to high-volume manufacturing.

2.2 Dynamic Random-Access Memory

2.2.1 *Through-Silicon Via Technology for Dynamic Random-Access Memory*

Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association has heavily promoted the adoption of through-silicon via (TSV) for dynamic random-access memory (DRAM) applications based on the improvements in speed-per-power consumption (lower pj/bit). Notable technologies include wide I/O DRAM for mobile, high bandwidth memory (HBM) for high-performance computing (HPC), and double data rate (DDR).

3D stacking (3DS) technology can increase memory capacity by stacking multiple DRAM chips into a single package using TSV. The suffixes in DDR4_2H,

DDR4_4H, and DDR4_8H DRAM denote two (2-high), four, and eight stacking layers, respectively. For example, a 16 GB DRAM can be constructed from stacking eight layers of 16-Gb chips. This allows a master-/slave-type architecture with many improvements over traditional DDR3 stacks, such as increased memory capacity, lower power consumption, and higher data transmission rates.

However, JEDEC is divided on the matter of whether DRAM is ready for TSV volume manufacturing. Samsung, the largest DRAM manufacturer, has been aggressively developing TSV technology. Although there was a delay since their original announcement at the *Institute of Electrical and Electronics Engineers'* (IEEE) Symposium on Computers and Communications—ISCC 2011, Samsung began mass production of DDR4 in August 2014.

The following is the announcement of Samsung [22].

“Samsung Electronics, Ltd. announced today that it has started mass producing the industry’s first 64 gigabyte (GB), DDR4, registered dual Inline memory modules (RDIMMs) that use three dimensional (3D) ‘through silicon via’ (TSV) package technology.”

It took 45 years from the beginning of TSV research and development for industry to begin high-volume manufacturing devices with this technology. Although some challenges related to reliability and cost remain, it would seem that TSV production will continue to gain momentum.

2.2.2 Wide I/O and Wide I/O2 Mobile Dynamic Random-Access Memory

JEDEC released standard JESD229 in December 2011 for the new Wide I/O mobile DRAM. However, Wide I/O mobile DRAM did not take off in smartphone industries, which had experts perplexed. In hindsight, we see that the supply chain was complex and bandwidth requirements have increased beyond expectations; there was also a thermal issue. Consumer demand instead led to the development of LPDDR3 (DDR3 for mobile computers) that provided an economical solution to achieving higher bandwidths.

DRAM bandwidth requirements continue to increase rapidly, but for the near future, the LPDDR4 technology will satisfy smartphone requirements. After abandoning Wide I/O, JEDEC introduced the Wide I/O2 task group (TG) standard in September 2011, planned to freeze the specification at the end of 2013, and estimated device production at the beginning of 2015. Wide I/O2 is expected to have more appealing performance, including a bandwidth greater than 50 MB/s and lower power consumption [23].

Following is the JEDEC conference news on March 16, 2013. “JEDEC to Discuss Wide I/O 2, LPDDR4 Standards at Conference, mobile technology will be the focus of a conference hosted by JEDEC standard-setting organization in early. Industry leaders will discuss various aspects of mobile chip standards in general as well as will cover the next-generation memory standards for smartphones and tablets, including LPDDR4 and Wide IO 2” [24]. Table 2.1 shows properties of mobile DRAM [25, 26, 27, 28].

Table 2.1 Properties of mobile DRAM

	LPDDR2	LPDDR3	LPDDR4	Widel/O	Widel/O2
<i>Standardization JEDEC</i>	<i>JESD209-2F</i>	<i>JESD209-3B</i>		<i>JESD229</i>	
Published	Rev. June 2013 (April 2011)	August 2013	Under developing	December 2011	Under developing
Data rate per pin (Mbit/sec)	1066	1600	3200	266	800
I/O count per channel	32	32	32	512	512
Channel	1 or 2	1 or 2	1 or 2	–	–
Bandwidth (GB/s)	4.3/8.5	6.4/12.8	12.8/25.6	17	51.2
VDD	1.2	1.2	1.1	1.2	1.1
Power consumption (W)		2.3	1.5	0.8–1.0	
Power efficiency (pJ/bit)	9.8	8.4	5.5	5.3	2.9
High Volume Manufacturing (HVM)	2010	2013	2015	Dropped	2015

No 3D products are included

2.3 Hybrid Memory Cube and High Bandwidth Memory Dynamic Random-Access Memory

Demand for bandwidth and power efficiency in digital applications has no foreseeable limit. HMC and HBM development will be driven by networking/server applications, for which the evolution of DDR technology will reach its limit. HMC precedes HBM; the announcements made in 2013–2014 were as follows.

2.3.1 Hybrid Memory Cube

(2013/Apr) Hybrid Memory Cube Consortium Gains Rapid Consensus for Final Specification and Decision to Renew Consortium [29].

“More than 100 developer and adopter members of the Hybrid Memory Cube Consortium (HMCC) announced they’ve reached consensus for the global standard that will deliver a much-anticipated, disruptive memory computing solution.”

(2013/Sep) Altera and Micron have announced that they have jointly demonstrated successful interoperability between Altera Stratix V FPGAs and Micron’s HMC [30].

“Altera Corporation and Micron Technology announced they have jointly demonstrated successful interoperability between Altera Stratix® V FPGAs and Micron’s Hybrid Memory Cube (HMC). This technology achievement enables system designers to evaluate today the benefits of HMC with FPGAs and SoCs for next-generation communications and high-performance computing designs.”

(2013/Sep) Micron Technology Ships First Samples of Hybrid Memory Cube Volume Production Planned for 2014 [31].

“Micron Technology Inc. announced today that it is shipping 2 GB Hybrid Memory Cube (HMC) engineering samples. HMC represents a dramatic step forward in memory technology, and these engineering samples are the world’s first HMC devices to be shared broadly with lead customers.”

(2013/Nov) Micron Technology announced today it is planning to adapt its HMC for petascale supercomputer systems, representing a dramatic step forward in memory technology [32].

“Micron Technology announced it is planning to adapt its Hybrid Memory Cube (HMC) for petascale supercomputer systems, representing a dramatic step forward in memory technology. HMC is designed for applications requiring low-energy, high-bandwidth access to memory, which is the most important requirement for supercomputers.”

(2013/Dec) Pico Computing Delivers the First PCI Express Card to Integrate Micron’s Hybrid Memory Cube and Multiple Altera Stratix V FPGAs [33].

“Pico Computing announced they have created the world’s most powerful blade server. The EX800 delivers compute density never before realized in a single PCI Express card and features Micron’s groundbreaking Hybrid Memory Cube (HMC) technology which provides unprecedented levels of highbandwidth, lowpower, random access memory performance.”

(2014/Feb) Hybrid Memory Cube Consortium Continues to Drive HMC Industry Adoption With Release of Second-Generation Specification [34].

“The Hybrid Memory Cube Consortium (HMCC), dedicated to the development and establishment of an industry-standard interface specification for the Hybrid Memory Cube (HMC) technology, today announced its continued work to build the HMC ecosystem and support for the industry adoption of this groundbreaking technology through the development of a new interface specification.”

(2014/May) Fujitsu exhibited the main board of the next supercomputer first time in Japan and the performance per size is 22 times of “KEI”: (in Japanese) [35].

“Eight DRAM modules per MPU are carried in a main board. This DRAM module is ‘Hybrid Memory Cube (HMC)’ of U.S. Micron Technology.”

(2014/June) Micron Collaborates With Intel to Enhance Knights Landing With a High Performance, On-Package Memory Solution [36].

“Micron Technology announced an ongoing collaboration with Intel to deliver an on-package memory solution for Intel’s next-generation Xeon Phi™ processor, codenamed Knights Landing.”

Also Micron reported at 2012 Symposium on VLSI Technology Digest of Technical Papers as follows. The HMC is a 3D DRAM architecture that reduces the access latency between logic and DRAM, improves the bandwidth and reduces power consumption. The main application targets are servers, graphics, and networking systems. The HMC is a heterogeneous stack that is internally connected using TSVs. For example, a standard 1-Gb 50-nm DRAM building block (DRAM layer) can be combined with various versions of application-specific logic (logic layers) using TSVs. In the HMC prototype, 1866 TSVs on 60- μm pitch were used, which had an energy consumption of 10.48 pj/bit—much smaller than the 65 pj/bit of DDR3 modules. In terms of architecture, the DRAM layer is a slave to the logic layer timing control. The logic layer also contains adaptive timing, calibration, refresh, and thermal management capabilities that are hidden from the host. Thus, HMC can use a simple abstracted protocol and high-speed links, such as a serializer/deserializer (SerDes), to connect a host or another cube. By increasing the number of TSVs (i.e., the number of links), the total bandwidth can reach 320 GB/s and beyond [37].

HMC Consortium developers are Altera, ARM, IBM, Micron, Open-Silicon, Samsung, SK hynix, and Xilinx. And adopter members are more than 100 [38].

2.3.2 High Bandwidth Memory Dynamic Random-Access Memory

(2013/Dec) SK Hynix to start production of HBM DRAM chip modules using 3D TSV chip-packaging technology [39].

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