

Contents

1 Research and Development History of Three-Dimensional Integration Technology	1
Morihiro Kada	
1.1 Introduction	1
1.1.1 The International Technology Roadmap for Semiconductors	1
1.1.2 3D Integration Technology	3
1.2 Motivation for 3D Integration Technology	4
1.3 Research and Development History of 3D Integration Technology	5
1.3.1 3D Packaging Technology	5
1.3.2 Origin of the TSV Concept	6
1.3.3 Research and Development History of 3D Technology in Organizations	8
1.3.3.1 Japan	9
1.3.3.2 Japanese 3D Integration Technology Research and Development Project (Dream Chip)	10
1.3.3.3 The USA	11
1.3.3.4 Europe	13
1.3.3.5 Asia	14
1.3.3.6 International	15
1.4 Research and Development History of 3D Integration Technology for Applications	15
1.4.1 CMOS Image Sensor and MEMS	15
1.4.2 DRAM	16
1.4.3 2.5D with Interposer	17
1.4.4 Others	17
References	19
 2 Recent Research and Development Activities of Three-Dimensional Integration Technology	 25
Morihiro Kada	
2.1 Recent Announcement of Research and Development Activities	25
2.2 Dynamic Random-Access Memory	30

2.2.1	Through-Silicon Via Technology for Dynamic Random-Access Memory.....	30
2.2.2	Wide I/O and Wide I/O2 Mobile Dynamic Random-Access Memory.....	31
2.3	Hybrid Memory Cube and High Bandwidth Memory Dynamic Random-Access Memory	33
2.3.1	Hybrid Memory Cube	33
2.3.2	High Bandwidth Memory Dynamic Random-Access Memory	34
2.4	FPGA and 2.5D	36
2.5	Others	36
2.6	New Energy and Industrial Technology Development Organization Japan.....	37
2.6.1	Next-Generation “Smart Device” Project.....	37
2.6.2	Background, Purpose, and Target of “Smart Device” Project.....	37
	References	38
3	TSV Processes.....	43
	Masahiko Tanaka, Makoto Sekine, Itsuko Sakai, Yutaka Kusuda, Tomoyuki Nonaka, Osamu Tsuji, Kazuo Kondo	
3.1	Deep Silicon Etching by Bosch Process	43
3.1.1	Introduction	43
3.1.2	Basic Characteristics of the Bosch Process.....	44
3.1.3	Bosch Etching Equipment for TSV.....	49
3.1.4	Conclusions	51
3.2	High-Rate Silicon Via Etching and Basics of Sidewall Etch Reaction by Steady-State Etch Process.....	52
3.2.1	Introduction	52
3.2.2	MERIE Process for TSV Application	53
3.2.2.1	Effect of RF.....	54
3.2.2.2	Effect of Pressure	56
3.2.2.3	Effect of Oxygen Addition.....	56
3.2.3	Investigation of Sidewall Etch Reaction Induced by $\text{SF}_6\text{-O}_2$ Plasma	58
3.2.3.1	Effect of Oxygen Addition.....	60
3.2.3.2	Effect of Substrate Temperature.....	62
3.2.3.3	Effect of SiF_4 Addition.....	63
3.2.4	Conclusion.....	65
3.3	Low-Temperature CVD Technology.....	65
3.3.1	Introduction	65
3.3.2	Cathode-Coupled Plasma-Enhanced CVD (LS-CVD)	66
3.3.3	Low-Temperature SiO_2 Deposition.....	69
3.3.3.1	Wafer Temperature During Low-Temperature Deposition	69

3.3.3.2	Step Coverage in Si-Via Holes.....	70
3.3.3.3	Electrical Characteristics of SiO ₂ Film Deposited at Low Temperature	72
3.3.3.4	Stress Control of SiO ₂ Film Deposited Using LS-CVD.....	73
3.3.4	Conclusion.....	74
3.4	Electrodeposition for Via Filling.....	74
3.4.1	Cu ⁺ Ion as an Accelerant Additive of Copper Electrodeposition.....	74
3.4.2	Relation Between Via Filling and Cu ⁺ Ion by Periodical Reverse Current Waveform.....	79
3.4.3	Simulation of Cu ⁺ Ion Distribution Inside the Via.....	82
3.4.4	High-Speed Via Filling Electrodeposition by Other Organizations	87
3.4.5	Reduction of Thermal Expansion Coefficient of Electrodeposited Copper for TSV by Additive	90
	References	94
4	Wafer Handling and Thinning Processes.....	97
	Takashi Haimoto, Eiichi Yamamoto, Takahiko Mitsui, Toshihiro Ito, Tsuyoshi Yoshida, Tsubasa Bandoh, Kazuta Saito and Masahiro Yamamoto	
4.1	Wafer Thinning Solution for TSV Devices	97
4.1.1	Introduction	97
4.1.2	General Thinning	98
4.1.3	Wafer Thinning for TSV Devices.....	99
4.1.4	TTV Control.....	99
4.1.5	Summary	102
4.2	A Novel Via-Middle TSV Thinning Technology by Si/Cu Grinding and CMP	103
4.2.1	Introduction.....	103
4.2.2	Experimental Method.....	105
4.2.3	Results and Discussion.....	106
4.2.3.1	Si/Cu Simultaneous Grinding Using Low-Density TSV Wafers	106
4.2.3.2	Si/Cu Simultaneous Grinding Using High-Density TSV Wafers	107
4.2.3.3	Si/Cu Same Removal Rate CMP (First CMP): Non-Selective CMP Between Cu and Si....	112
4.2.3.4	TSV Protrusion CMP (Second CMP): Selective CMP Between Cu and Si.....	114
4.2.3.5	Post Second CMP Cleaning	115
4.2.4	Conclusion.....	117
4.3	Temporary Bonding.....	118
4.3.1	Background	118

4.3.2	The 3M™ Temporary Bonding Materials.....	119
4.3.3	The 3M™ Temporary Adhesive.....	120
4.3.4	Laser-Absorbing Layer	124
4.3.5	The Next Steps	128
4.4	Temporary Bonding and Debonding for TSV Processing.....	128
4.4.1	Introduction	128
4.4.2	Temporary Bonding and Debonding Process.....	129
4.4.3	Debonding Method.....	131
4.4.4	Functions and Performance Requirements for Temporary Bonding Device	132
4.4.5	Ability and Performance Requirements for Debonding Devices	135
4.4.6	Tokyo Electron's Temporary Bonder and Debonder Device Concept and Lineup	137
4.4.7	Future Outlook	137
	References	138
5	Wafer and Die Bonding Processes	139
	Hiroaki Fusano, Yoshihito Inaba and Toshihisa Nonaka	
5.1	Permanent Wafer Bonding	139
5.1.1	Introduction	139
5.1.2	Low-Temperature or Room Temperature Wafer Direct Bonding Method and Application	140
5.1.2.1	Fusion Bonding.....	140
5.1.2.2	Surface Activated Bonding	140
5.1.2.3	Anodic Bonding	141
5.1.2.4	Cu ₂ Cu/Oxide Hybrid Bonding.....	142
5.1.2.5	Conclusion of Low-Temperature or Room Temperature Wafer Direct Bonding Methods and Their Applications	142
5.1.2.6	Future Outlook for Bonding Application Using Low-Temperature or Room Temperature Wafer Direct Bonding Methods	142
5.1.3	Requests Made to Equipment Makers and Initiatives Regarding Low-Temperature or Room Temperature Wafer Direct Bonding Methods	143
5.1.3.1	Post BAA.....	144
5.1.3.2	Scaling	144
5.1.3.3	Distortion	145
5.1.3.4	Bonding Strength	146
5.1.3.5	Void	146
5.1.4	Tokyo Electron Initiatives	147
5.1.5	Conclusion.....	148
5.2	Underfill Materials.....	148
5.2.1	Technical Trend for Three-Dimensional Integration Packages and Underfill Materials	148

5.2.2	Requirements for Underfill Materials	150
5.2.2.1	Requirements for CUF and Material Technology Trend.....	150
5.2.2.2	Requirements for NCP and Material Technology Trend.....	152
5.2.3	Application to CUF Between the Stacked Chips	154
5.3	Nonconductive Films	155
5.3.1	Introduction	155
5.3.2	Required Material Feature from Bonding Process.....	156
5.3.3	Void Issue in NCF	160
5.3.4	High Throughput NCF–TCB	163
	References	165
6	Metrology and Inspection.....	167
	Gilles Fresquet, Jean-Philippe Piel, Sylvain Perrot, Hideo Takizawa, Osamu Sato, Allen Gu, Michael Feser, Bruce Johnson, Raleigh Estrada and Yoshitaka Tatsumoto	
6.1	Principles of Spectroscopic Reflectometry	167
6.1.1	Introduction	167
6.1.2	Measurement.....	168
6.1.3	Setup.....	169
6.1.4	Analysis	169
6.1.5	Conclusion.....	171
6.2	Low-Coherence Interferometry for Three-Dimensional Integrated Circuit Through-Silicon Via.....	171
6.2.1	Optical Measurement of Topographies and Thicknesses	171
6.2.1.1	3D IC TSV Needs Tomography	171
6.2.1.2	Tomography with Low-Coherence Interferometry	172
6.2.2	Theory of Optical Coherence Tomography.....	172
6.2.2.1	Basic Principle	172
6.2.2.2	Time-Domain OCT	174
6.2.2.3	Fourier-Domain OCT.....	177
6.2.2.4	Practical Considerations.....	179
6.2.3	Conclusion.....	182
6.3	Silicon and Glue Thickness Measurement for Grinding.....	182
6.3.1	Introduction.....	182
6.3.2	TSV Wafer Manufacturing Method and Challenges of Grinding	183
6.3.3	Features of BGM300.....	184
6.3.4	Verifying BGM300 Measurement Results	185
6.3.5	Measurement After Grinding	186
6.3.6	Optimized Wafer Grinding Based on Via Height Information from BGM300	187
6.3.7	Conclusion.....	189

6.4	3D X-ray Microscopy Technology for Nondestructive Analysis of TSV	189
6.4.1	Introduction	189
6.4.2	Fundamentals of X-ray Microscopy.....	190
6.4.2.1	Physics of X-ray Imaging	190
6.4.2.2	3D X-ray Microscopy	191
6.4.3	Applications for TSV Process Development.....	192
6.4.4	Applications for TSV Failure Analysis	194
6.4.5	Summary	195
6.5	Wafer Warpage and Local Distortion Measurement	196
6.5.1	Introduction	196
6.5.2	Basic Functions of WDM300.....	196
6.5.3	Measurement and Analysis of Local Deformations	197
6.5.4	Application	198
6.5.5	Summary	200
	References	200
7	TSV Characteristics and Reliability: Impact of 3D Integration Processes on Device Reliability	201
	Kangwook Lee and Mitsuma Koyanagi	
7.1	Introduction.....	201
7.2	Impact of Cu Contamination on Device Reliabilities in Thinned 3D-IC Chip	202
7.2.1	Impact of Cu Diffusion at Backside Surface in Thinned 3D-IC Chip	204
7.2.1.1	Effect of Intrinsic Gettering Layer	204
7.2.1.2	Effect of EG Layer	206
7.2.2	Impact of Cu Diffusion from Cu Via	210
7.2.2.1	Effect of the Barrier Thickness and the Scallop Roughness	211
7.2.2.2	Effect of the Annealing Temperature	214
7.2.2.3	Keep-Out-Zone Characterization by Cu Diffusion from Cu Via.....	215
7.3	Impact of Mechanical Stress/Strain on Device Reliability in Stacked IC	216
7.3.1	Micro-Bump-Induced Local Stress in Stacked IC	217
7.3.2	Si Mechanical Strength Reduction by Thinning	220
7.4	Impact of 3D Integration Process on DRAM Retention Characteristics	222
7.4.1	Impact of Mechanical Strength on Retention Characteristics in Thin DRAM Chip.....	223
7.4.2	Impact of Cu Contamination on Memory Retention Characteristics in DRAM Chip	228
	References	232

8 Trends in 3D Integrated Circuit (3D-IC) Testing Technology	235
Hiroshi Takahashi, Senling Wang, Shuichi Kameyama, Yoshinobu Higami, Hiroyuki Yotsuyanagi, Masaki Hashizume, Shyue-Kung Lu and Zvi Roth	
8.1 Crucial Issues and Key Technologies for 3D-IC Testing	236
8.2 Research Trends in Pre-Bond Test for 3D-IC	237
8.3 Research Trends in Post-Bond Test for 3D-IC	238
8.4 Research Trends in Automatic Test Pattern Generator and Test Scheduling for TSVs in 3D-IC	240
8.5 An Accurate Resistance Measuring Method for TSVs in 3D-IC	243
8.5.1 Background of Our Study	243
8.5.2 Problems of Conventional Analog Boundary Scan for TSV Resistance Measurement	245
8.5.2.1 Analog Boundary Scan	245
8.5.2.2 Standard Resistance Measuring Method by 1149.4	246
8.5.2.3 Problems of Conventional Analog Bound- ary Scan for TSV Resistance Measuring	247
8.5.3 Proposed Measuring Method	249
8.5.4 Summary	251
8.6 Delay Measurement Circuits for Detecting TSV Delay Faults	251
8.6.1 Application of Time-to-Digital Converter Embedded in Boundary Scan for 3D-IC Testing	251
8.6.2 Delay Measurement Circuit Using the Vernier Delay Line	254
8.6.3 Estimation of Defect Size Detectable by the Test Method	256
8.6.4 Summary	258
8.7 Electrical Interconnect Tests of Open Defects in a 3D-IC with a Built-In Supply Current Test Circuit	258
8.7.1 Electrical Tests with a Built-In Supply Current Test Circuit	258
8.7.2 Experimental Evaluation of Our Electrical Test Method	262
8.7.3 Summary	265
References	265
 9 Dream Chip Project at ASET	 269
Morihiro Kada, Harufumi Kobayashi, Fumiaki Yamada, Haruo Shimamoto, Shiro Uchiyama, Kenichi Takeda, Kenichi Osada, Tadashi Kamada and Fumihiko Nakazawa	
9.1 Overview of Japanese 3D Integration Technology Research and Development Project (Dream Chip)	270
9.1.1 3D Integration Process Basic Technologies	270
9.1.1.1 Thermal Management and Chip-Stacking Technology	270
9.1.1.2 Thin-Wafer Technology	271

9.1.1.3	3D Integration Technology	271
9.1.2	Application Technologies.....	272
9.1.2.1	Ultrawide Bus 3D-SiP Integration Technology.....	272
9.1.2.2	Mixed-Signal (Digital and Analog) 3D Integration Technology for Automotive Application.....	272
9.1.2.3	Heterogeneous 3D Integration Technology for Radio Frequency Microelectromechan- ical Systems.....	272
9.2	Thermal Management and Chip-Stacking Technology.....	273
9.2.1	Background	273
9.2.2	Chip-Stacking/Joining Technology	273
9.2.2.1	Metal Bump Materials and Structure	273
9.2.2.2	Reliability Study of Micro-bump	274
9.2.2.3	Electromigration Test to Understand the Current Density of Micro-bump Joint.....	276
9.2.2.4	Flip Chip Bonding Density Towards 10- μ m Connection Bump Pitch.....	277
9.2.2.5	Stack and Gang Bonding.....	285
9.2.2.6	Nondestructive Inspection Technologies of Micro-joint	287
9.2.3	Thermal Management Study	292
9.2.3.1	Evaluation Technology of 3D Integrated Chip Stack	292
9.2.3.2	TV200 Measurement Result and Correla- tion with Simulation.....	294
9.2.3.3	Thermal Conductivity Anisotropy Induced by Cu TSV.....	295
9.2.4	Development of Automobile Drive Assistance Camera.....	295
9.2.4.1	Development of Integration Process	295
9.2.4.2	Development of Cooling System for Automobile Drive Assistance Camera	297
9.2.5	Summary	300
9.3	Thin Wafer Technology	302
9.3.1	Background of Wafer Thinning Technology	302
9.3.2	Issues of Wafer Thinning	303
9.3.3	Ultrathin Wafer Thinning Process.....	303
9.3.3.1	Wafer Support System.....	303
9.3.3.2	Heat Resistance of the Resin Used for WSS Temporary Bonding	307
9.3.3.3	Dicing Technology of Thin Chips.....	310
9.3.3.4	Die Pickup Technology of Thin Chips.....	311
9.3.3.5	Thin Wafer Processing Technique in the Wafer-Stacking Process.....	317

9.3.4	Issues in the Prevention of Device Characteristic Changes and Metal Contamination During Wafer Thinning.	321
9.3.4.1	Evaluation of Crystal Defects and Metal Pollution in the Thin Wafer	322
9.3.4.2	Backside Grinding Methods and Their EG Effect	322
9.3.4.3	Variation of Electrical Characteristics with Mechanical Stress	325
9.3.5	Standardization	329
9.3.6	Summary	330
9.4	3D Integration Technology	331
9.4.1	Background and Scope	331
9.4.2	C2C Process	332
9.4.2.1	C2C Integration Overview	332
9.4.2.2	C2C Integration Results	334
9.4.3	W2W Process	338
9.4.3.1	W2W Integration Overview	338
9.4.3.2	Wafer Bonding Technology	342
9.4.3.3	W2W Integration Results	345
9.4.4	Standardization	350
9.4.4.1	Reference Model of TSV Electrical Characteristics and Guideline of Test Conditions	350
9.4.5	Summary	355
9.5	Ultrawide Bus 3D System in Package Technology	356
9.5.1	Background	356
9.5.2	The Test Vehicle Fabrication	357
9.5.3	Evaluation	360
9.5.4	Summary	369
9.6	Mixed Signal (Digital and Analog) 3D Integration Technology for Automotive Applications	369
9.6.1	Introduction	369
9.6.2	Challenges	370
9.6.3	Results of Development of Mixed-Signal 3D Integration Technology	371
9.6.3.1	Basic Technology Development of a 3D Integrated Imaging Sensor Module for In-Vehicle Support Systems	371
9.6.3.2	The Mixed-Signal (CIS/CDS/ADC/IF) Integrated Structure with TSV Connection	373
9.6.3.3	Development of an Si Interposer with TSV-Type Decoupling Capacitor	379
9.6.3.4	A Trial Production and Evaluation of the Driving-Assistance Image-Processing System for Automobiles	383
9.6.4	Conclusion	384

9.7	Heterogeneous 3D Integration Technology for Radio	
	Frequency Microelectromechanical Systems.....	385
9.7.1	Background and Issues.....	385
9.7.2	Development Result.....	386
9.7.2.1	Structure of 3D Integration RF Module.....	386
9.7.2.2	MEMS Tunable Filter	387
9.7.2.3	MEMS Switch.....	390
9.7.2.4	CMOS Driving IC.....	394
9.7.2.5	3D Integration of Tunable Filter Module.....	395
9.7.2.6	RF and Tuning Performances of the Fabricated 3D Tunable Filter Module.....	396
9.7.3	Summary	397
	References	398
	Index	401

Three-Dimensional Integration of Semiconductors

Processing, Materials, and Applications

Kondo, K.; Kada, M.; Takahashi, K. (Eds.)

2015, XIX, 408 p. 460 illus., 269 illus. in color.,

Hardcover

ISBN: 978-3-319-18674-0