

Chapter 2

Three-Dimensional Integration: A More Than Moore Technology

Abstract Three-dimensional integrated circuits (3D-ICs), which contain multiple layers of active devices, have the potential to dramatically enhance chip performance, functionality, and device packing density. They also provide for microchip architecture and may facilitate the integration of heterogeneous materials, devices, and signals and offer a promising solution for reducing both silicon footprint and interconnect length without shrinking the transistors. However, before these advantages can be realized, key technology and CAD challenges of 3D-ICs must be addressed. More specifically, the process required to build circuits with multiple layers of active devices and CAD tools used for design and validation of such circuits. Several such methodologies and CAD tools associated with the design fabrication of 3-D ICs are discussed in this chapter. Few successful 3D-IC design methods and CAD tools and benefits of applying 3D design to the future reconfigurable systems are also discussed in this chapter.

2.1 Introduction

The ongoing demand for greater functionality resulting in multiple IC products, longer off-chip interconnects ravage the performance of microelectronic systems. The advent of System-on-Chip (SoC) in the mid 1990s primarily addressed the increasing delay of the off-chip interconnects. Integrating all of the components on a monolithic substrate enhances the overall speed of the system, while decreasing the power consumption. To assimilate disparate technologies, however several difficulties must be surmounted to achieve high yield for the entire system. Additional system requirements for the radio frequency (RF) circuitry, passive elements, and discrete components, such as decoupling capacitors, which are not easily integrated due to performance degradation or size limitations. While Moore's law [1] and the pursuit of ever increasing transistor counts is well known in IC design and manufacturing circles, what is seldom brought to light for others, are the escalating cost and technology challenges associated with this pursuit. Smaller transistors and larger dies have been reasonable answer to this quest in the past. Stacked dies using wire bond connections and flip-chips have even been employed to create system-in-package (SiP) solutions

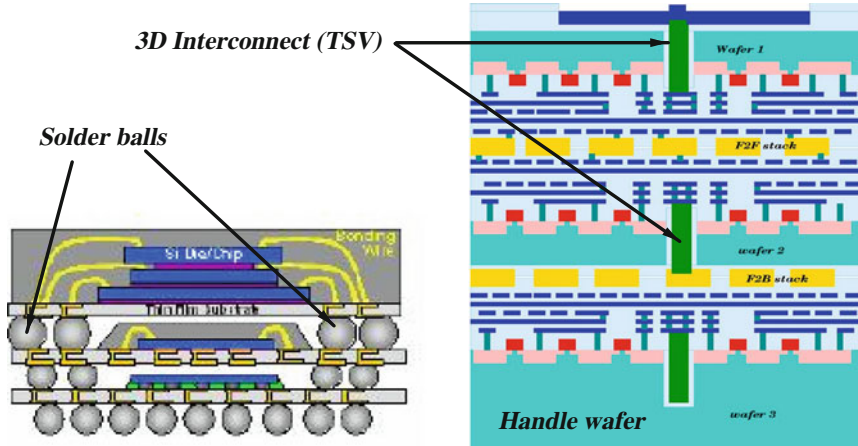


Fig. 2.1 Interconnects bond wires in typical System-in-package (SiP) and 3D-IC

that meet the needs of some. Looking for alternative solutions for next generation designs, that meet the performance, integration, form-factor, manufacturability, and cost requirements, may have begun to look at going up rather than out. With this trend, the Three-dimensional (3D) integration using through-silicon via (TSV) technology has gained much attention. Once the domain of specialist applications, more mainstream users, such as memories, microprocessors and specialized logic designs are now being considered as TSV candidates. The advantages of 3D-IC integration are better electrical performance, low power consumption, lower area and weight and high performance (Fig. 2.1).

2.1.1 Opportunities for Three-Dimensional Integration

Performance requirements such as increased bandwidth, reduced latency, and lower power consumption are driving the adoptions of 3D-IC designs. A complete 3D-IC implementation is usually envisioned as a stack of active chips using TSVs to connect through each chip down to a package substrate. TSV designs represent a convergence of SoC and SiP disciplines, providing designers the means to significantly increases the bandwidth between the logic chip and the memory especially with wide memory interfaces that cannot be achieved with bond wires, as well as the ability to mix and match dies that not only use different process node, but also different manufacturing technologies such as SiGe, SOI, CMOS low voltage, CMOS high voltage, Bipolar, GaAs, etc. The ability to combine different dies in a single stack enable to acquire needed functionality to provide high-quality, proven die. What is new in 3D-ICs is the ability to place vertical interconnections (TSVs) in a dense array, without the strict perimeter constraints imposed by an equivalent wire-bonded design. Utilizing

stacked chips, particularly in memory-intensive designs, allows designers to stay at today's reasonable process nodes for each die and derive the benefit or proven volume manufacturing processes.

Three-dimensional (3D) die stacks and high-bandwidth silicon packaging technology using emerging through silicon vias (TSVs), thinned silicon, and fine-pitch silicon-silicon interconnections (SSIs) make use of a wide variety of technology structures, materials, and processes. Universities, consortia, and industry have driven research and early demonstrations for a decade. TSV and SSI interconnection density can scale in excess of six orders of magnitude, making the technology widely applicable from simple to very complex applications. At academic research institutes and semiconductor industries, new 3D test-vehicle (i.e., demonstrator) designs followed by manufacturing, assembly, and characterization studies continue to provide technologists with an understanding of structure and process-integration capabilities and limitations. Results from these technology studies provide guidance on 3D design rules, structures, processes, tests, and reliability, which can support the manufacturing of 3D products and provide data that we may use to determine technology directions. Practical technology fabrication and integration approaches need to consider targeted TSV and SSI interconnection density, silicon thickness, and power densities. In addition, decisions with respect to options such as TSV conductor material, SSI integration material, and use of die-on-die, die-on-wafer, or wafer-to-wafer process approaches need to be made with regard to interconnection redundancy, die size, yield, cost, and test methodology.

The inherent advantage of 3D integration is the drastic decrease in interconnect length, particularly the long global interconnects, which directly results in increased speed [2–6]. We can understand this by simple geometry analysis for 3D-ICs. A given square area A has maximum Manhattan wirelength $2\sqrt{A}$. The same area is split into two tiers reduces the wirelength to $\sqrt{2}\sqrt{A} + l_v$, where l_v is the length of via between tiers. In general, n layers gives a maximum Manhattan wirelength of $2\sqrt{\frac{A}{n}} + (n-1)l_v$. Figure 2.2 illustrate the graphical representation of wire-length reduction which the original 2D chip implemented using 3D technology with n tiers. The interconnect power is also reduced as the capacitance of the wires decreases

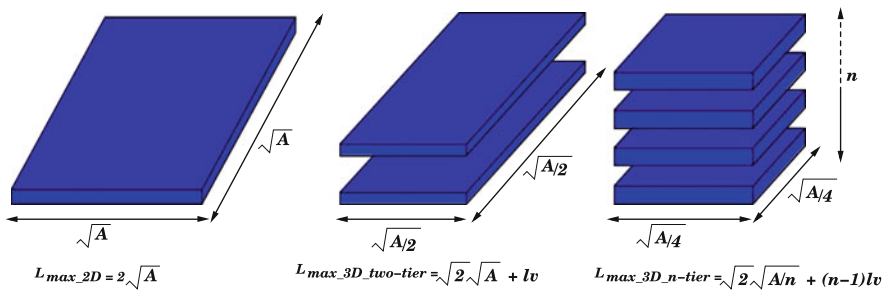


Fig. 2.2 Illustration of wire-length reduction where the original 2D chip implemented using 3D technology

[7, 8]. Additionally, the total power dissipated by an interconnect system is further decreased as the number of repeaters inserted along the interconnect is reduced [9]. Finally, coupling among intraplane adjacent interconnects is lower due to decreased length, improving signal integrity. The 3D-IC based systems provides the capability to include disparate technologies [10], greatly extending the capabilities of modern systems-on-chip (SoC). This defining feature of 3D-ICs offers unique opportunities for highly heterogeneous and sophisticated systems [11, 12]. A vast pool of applications such as medical, wireless communications, military, and low-cost consumer products, exists for vertical integration, as the proximity of the system components caused by the third dimension is suitable for either the high performance or low power ends of the SoC application space [13]. This heterogeneity, however, greatly complicates the interconnect design process within a multi-tier system, as potential design methodologies need to manage the diverse interconnect impedance characteristics and process variations caused by the different fabrication processes and technologies employed in the different physical tiers.

Three-dimensional circuits can be conceptualized as the bonding of multiple wafers or bare dice. The distinctive difference between an SiP and a 3D IC is the granularity of the vertical interconnects. Different bonding styles between the planes within a 3D system are also possible Face-to-Face (F2F), Face-to-Back (F2B), and Back-to-Back (B2B) [14, 15]. Examples of SiP structures and various bonding styles for 3D circuits are illustrated in Fig. 2.1. Each of these bonding styles is likely to include through silicon vias (or interplane vias) with different physical dimensions. Consequently, the density of the vertical interconnects can vary not only among different 3D circuits but also among the physical planes within a 3D circuit.

2.2 Historical Evolution of 3D System Integration

The proposal of doubling the number of transistors on an IC chip every 24 months by Gordon Moore in 1965 (Moore's law) [1] has been the most powerful driver for the development of the microelectronics industry in the past 45 years. This law emphasizes lithography scaling and 2D integration of all functions on a single chip, perhaps through system-on-chip (SoC) as schematically shown in the left-hand side of Fig. 2.3. On the other hand, the integration all these functions can be achieved through 3D-IC integration [13, 16–18] as illustrated in Fig. 2.4.

Through Silicon Via (TSV) is the heart 3D-IC integration [19]. Though the 1956 Nobel Laureate in Physics, William Shockley invented TSVs more than 50 years ago in U.S. Patent #3,044,909, filed in 1958 and issued in 1962, but it was not intended for 3D-IC integration and it took half a century for the production technology to reach the level of expertise that would actually permit making TSVs. From a die with hundreds of transistors in the 1960s to dies approaching billions of circuits in 2014, on-chip integration has continued to require lithographic advancements for circuit and increase in wire density has led to increasing the number of wiring levels on the chip. Over decades of semiconductor scaling, on-chip integration has far

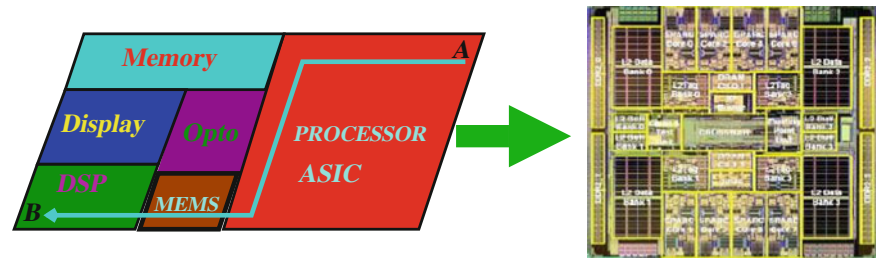


Fig. 2.3 Typical 2D System-on-Chip (SoC) integration

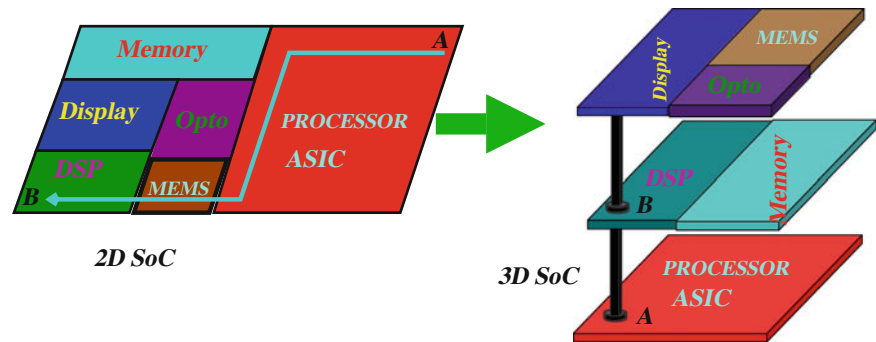


Fig. 2.4 The difference in wire length between 2D SoC and 3D SoC, the wire length between blocks A and C in 2D SoC and 3D SoC

out-stripped off-chip 3D integration and growth in I/O interconnections. For off-chip interconnections over the last five decades, I/O interconnections grew from tens of I/O interconnections to about several thousands of I/O interconnections for the most complex die manufactured today [20–22]. Figure 2.5 shows the evolution of 3D-IC technology along with the resulting relative I/O interconnection density for 3D design and implementation. The emerging 3D integration approaches can be implemented different packaging form factors to combine TSVs, thinned silicon and interposer technology as required to achieve higher interconnection density. High bandwidths may be achieved using 3D chip integration, 3D die stacking, or 3D silicon packaging in which each form factor offers high interconnection density ($10^4/\text{cm}^2$ to $10^8/\text{cm}^2$). Therefore, trade-offs between best system form factors will be dependent on factors such as system architecture, manufacturing costs, and test and assembly integration yields.

Looking toward the future, industry and academic researchers are developing wafer-to-wafer and die-to-wafer stacking techniques for the fabrication of devices that leverage the z-direction but eliminate the need for multiple packages [23]. Additionally, these techniques reduce interconnect delays, form factors, and power consumption while allowing integration of numerous heterogeneous devices. In the wafer-to-wafer approach, circuitry is divided into sections that are built onto separate

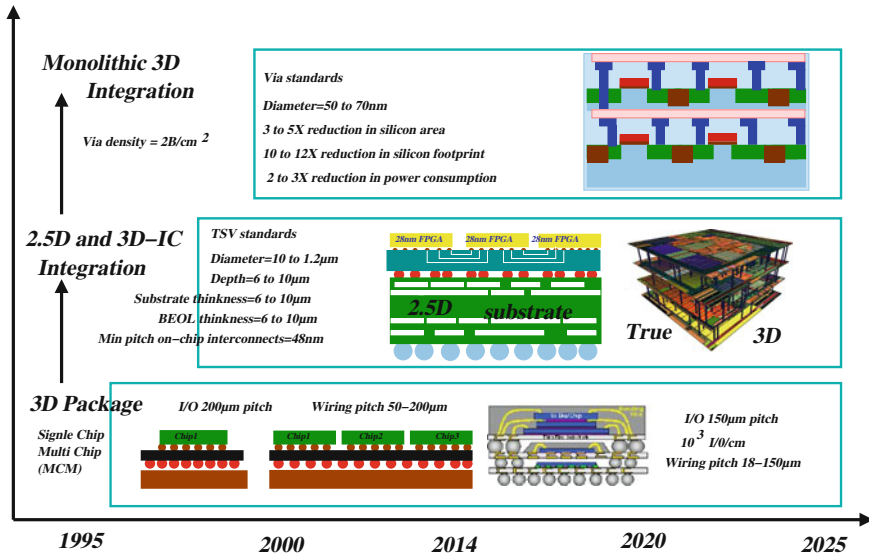


Fig. 2.5 Evolution of 3D integration and vertical interconnect technology

wafers using standard processing methods. The wafers are then post-processed for through-silicon interconnections (TSVs), creating the vertical connectors. The wafers are aligned, bonded, thinned, and diced into individual devices. In October 2006, several equipment manufacturers, led by Alcatel, EV Group, Semitool, and XSiI, formed a consortium, dubbed EMC-3D, to address the technical and cost issues associated with the creation of TSV interconnect technology for die stacking and wafer-to-wafer attach. In the die-to-wafer variation, a known good die (KGD) is bonded to a wafer. This approach is preferred in configurations that require three or more dies in a stack. Privately held Ziptronix Inc, a spin-out business of the Research Triangle Institute, advanced the state of the art in the die-to-wafer methodology when it introduced, late in 2005, a direct bond interconnect technology (a covalent room-temperature bond) that replaces through-die vias (TSVs), increases electrical connection density, and reduces interconnect delays.

Research investigations have explored a wide variety of structures, processes, and bonding approaches. Researchers recognize the importance of

- developing fine-pitch vertical interconnections using TSVs,
- developing thinning technology for silicon and interconnection technology that joins thinned silicon dies into die stacks and that joins dies to silicon packages,
- developing wafer-to-wafer bonding technologies.

In addition to power delivery and signal interconnections, investigators have also included approaches for thermal cooling and modeling of heat removal from thinned silicon structures and fine-pitch interconnections. Vertical interconnect (TSV) technology is a key focus area and an enabler for the evolution of 3D-IC design and

packaging. As already indicated, TSV technology is one of the key interconnect solutions enabling a vertical method of electrical connectivity for various 3D-IC configurations such as stacked die and wafer-level packaging. In TSV investigations, technical reports have included studies in which researchers sought submicron TSV diameters for compatibility with wafer front-end-of-line (FEOL) and back-end-of-line (BEOL) wafer fabrication or alternatively for silicon-based package solutions. TSV diameters and pitches have ranged from large sizes, such as about 10–100 μm via diameter and silicon thickness of about 50–300 μm , down to via diameters of less than 1–10 μm with corresponding silicon thicknesses ranging from about 50 μm down to about 6 μm silicon thicknesses. Reported TSV conductors have included tungsten, copper, composite, paste, doped polysilicon, as well as other electrical conductors. For example, [24] gave a TSV technical presentation on 10 μm copper conductors utilizing TSVs for electrical interconnection at a 20 μm pitch.

Fine-pitch interconnection, also at a 20 μm pitch for silicon-on-silicon connections with TSVs, has also been reported by [25] and also variety of bonding and electrical interconnection approaches between silicon die in thinned silicon die, die stacks, or packages using silicon reported in [26, 27]. In these interconnection examples, anisotropic conductive polymers were used to bond 25 μm thinned dies with 50 μm pitch AuSn bumps. Technical publications have also reported fine-pitch solder connections to copper as a means either to stack thinned silicon chips to other silicon dies or to join dies to silicon packages [25–28]. An application that leverages TSVs and fine-pitch interconnections with demonstration of functioning memory die stacks has also been presented [29]. The main future challenge for TSV technology relates to its ability to maintain performance parameters, such as signal integrity or heat management, as data rates climb. However, a number of companies have been able to demonstrate efficient TSV electrical interconnect solutions that meet data rates on the order of 10 Gb/s. Many technology suppliers as ZyCube, Intel, Samsung and IBM are currently optimizing the manufacturability and reliability of their 3D-IC fabrication process. Tezzaron's *Super-Via* technology, initially a post backend-off-line process with Cu–Cu bonding [16] was abandoned due to failures of the used copper TSVs (5 μm diameter). In consequence they changed their process now to tungsten filled *Super-Contacts* with 1.2 μm diameter [30, 31].

2.3 Vertical Interconnect Technology Development (TSV)

Through Silicon Via or TSVs are a critical enabler for both wafer-to-wafer and die-to-die stacking for which low-inductance, high bandwidth vertical interconnects are needed in silicon. Applications may require only a few, thousands, or millions of vertical interconnections, a number that is very product dependent and is affected by architecture, desired product specifications, silicon thickness, materials, structures, and processes. The range in size includes diameters from less than 1.2–90 μm . The silicon thickness ranges from less than 6 μm to a full wafer thickness of 730 μm , with

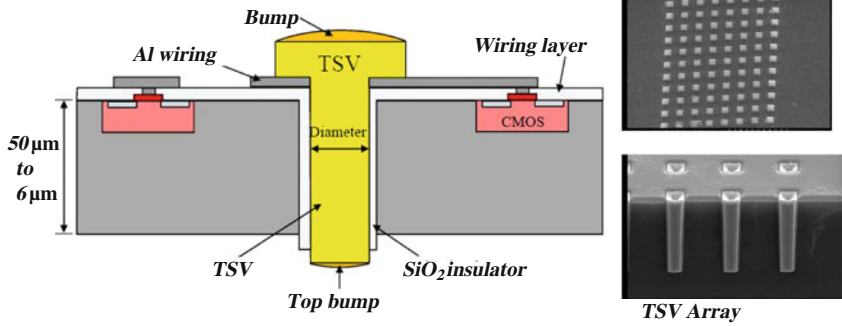


Fig. 2.6 Representation of Through Silicon Via (TSV)

most studies having been performed with 150 μm thicknesses or less. Material evaluations have included copper, tungsten, and composite materials. Figure 2.6 shows examples of TSV cross-sections.

As illustrated in Fig. 2.6, a through-silicon via (TSV) is a vertical via that completely passes through a silicon die. Its main purpose is to establish electrical connectivity between devices in two different dies in a 3D-IC stack. There is presently no consensus on the most efficient bonding technique which largely depends on the application requirements [30, 32, 33]. There are various bonding techniques [34] which range from direct oxide bonding, metal to metal (Cu–Cu) bonding, with different variants and adhesives. Still, the most prevalent technique to stack TSV based dies is a micro-ball based bonding. Micro-balls or micro-bumps are the most appropriate for present 3D applications since the density of TSVs is not very high (1K–10K/chip), their locations are predetermined and micro-bump based stacking is presently more reliable than alternative techniques. Depending on when the TSVs are fabricated, two major types of TSV exist: via-first and via-last, as illustrated in Fig. 2.7.

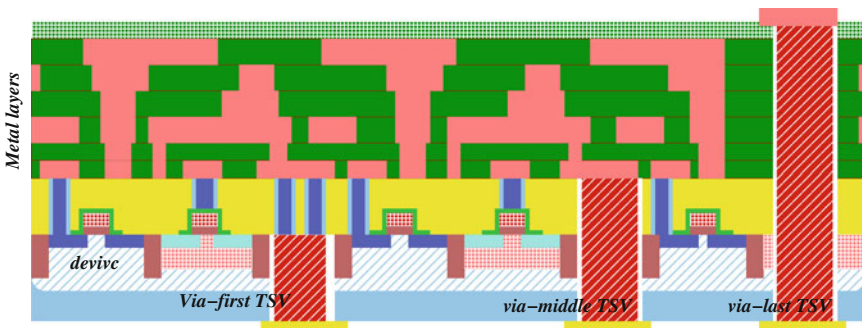


Fig. 2.7 An illustration of Via-first, via-mid and via-last TSV technology process

- Via-first: TSV's are fabricated before CMOS or Si frontend (FEOL, Front-End-Of-Line) device fabrication processing.
- Via-middle: TSV's are fabricated after the Si frontend (FEOL) device fabrication processing but before the backend (BEOL-back-end-of-line), interconnect process.
- Via-last: TSVs, are fabricated after or in the middle of the Si Backend (BEOL) or bonding, essentially when the wafer is finished.

The dimensions of via-first TSVs are typically smaller (1–10 μm diameter), with aspect ratios (=height:diameter) of 3:1–10:1. A key benefit to the via first approach is that companies using it don't need to worry about spoiling expensive wafers at the R&D stage because they can use bare Si or SOI wafers. For Si interposer wafer development related to heterogeneous stacking, via-first is still being developed and used. In this case of via-last TSVs, the processing can be done at the foundry or packaging house and there is the possibility to start TSV processing from the top surface of the wafer (Front-side processing) where the active transistor layouts are placed. The via-last TSV diameter is wider (10–50 μm), with aspect ratios of 3:1–15:1. There are two main technologies for *drilling* TSVs: dry etching or Bosch etching, and laser drilling. Polysilicon, copper, and tungsten are the most popular materials for TSV fill. Silicon dioxide is a popular material for the liner that sits between the TSV and silicon substrate for insulation purpose. From the perspective of physical design, via-first TSVs are less intrusive because they interfere only with the device, M1, and top layers, whereas via-last TSVs interfere with all layers in the die as illustrated in Fig. 2.7. Via-first TSVs have their landing pads on M1 and the top metal layers, whereas via-last TSVs have their landing pads only on the top metal layers. These landing pads include keep-out-zone uniformly located around them to reduce coupling effects. The connection between via-first TSVs are made using local interconnect and vias in between adjacent dies, whereas via-last TSVs are stacked on top of each other as illustrated in Fig. 2.7. Therefore, via-first TSVs are usually used for signal and clock delivery, whereas power delivery network utilize via-last TSVs in general.

2.4 3D Integration: Manufacturing Methods

Various 3D integration technologies currently pursued by semiconductor industry and research institutions. There are many different integration and manufacturing schemes for 3D interconnects. One way to categorize the different integration schemes is by the orientation of the individual dies to each other. Figure 2.8 shows face-to-back (F2B) and face-to-face (F2F) integration. F2F integration does not require TSVs in general, however TSV can be used for I/O connections, whereas TSVs are required for F2B integration. For two-layer chip stacks, both integration schemes have some advantages and disadvantages. F2B configuration uses standard process for test, assembly and packaging, however F2F do not have a standard process. For multi-layer stacks, F2B has the advantage that after each bonding step

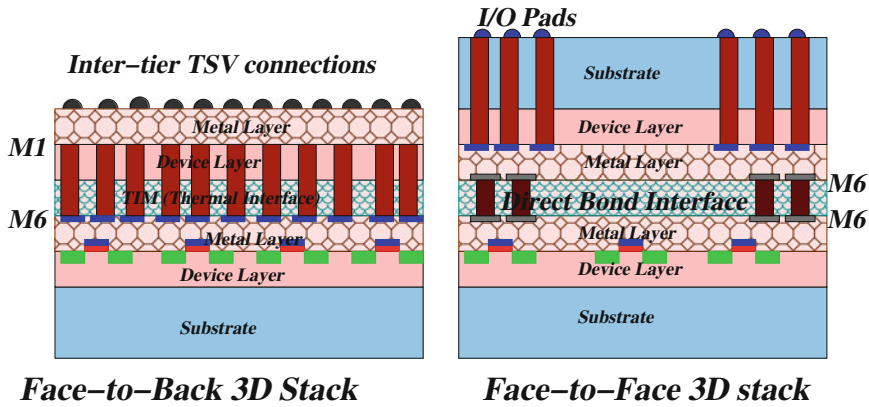


Fig. 2.8 3D stacking methods: F2F and F2B stacking configuration

the top device layer is face up so that the stacking unit process can be repeated multiple times. However, for F2B integration, the die/wafer has to have the final thickness already during stacking, as subsequent thinning is not possible. In F2F stacking configuration wafer thinning is not a requirement.

Another more popular way to categorize 3D integration schemes is based on the point at which the TSV is created during the manufacturing process. In the past, the only distinction was whether the via was manufactured before or after wafer thinning: via-first or via-last. Today, it is common to further distinguish whether the via was created prior to front-end processing, i.e., via first, or after front-end processing (but before wafer thinning), i.e., via-middle. Figure 2.9 shows a typical process flow for via-middle manufacturing. Another important distinction within the various integration schemes is based on wafer or die level processing: chip-to-chip (C2C), chip-to-wafer (C2W) and wafer-to-wafer (W2W). C2C has mainly been used for high performance, high margin devices. For lower margin devices like consumer electronics, C2C is not very suitable due to single die processing. Of course, W2W integration allows wafer-level processing after stacking. W2W integration gives the highest throughput and the highest alignment accuracy. But W2W integration requires that the dies have the exact same size, and it has the inherent risk that a defective die is bonded to a good die, thereby destroying the whole stack. C2W is a hybrid process and combines the single die placement with the feasibility of wafer-level processing after die placement. With C2W integration, it is possible to stack dies of different sizes. With a modular design and chip architecture, it must be assumed that dies typically will have different sizes. For heterogeneous integration in particular, C2W is the method of choice as currently only silicon devices are manufactured on 300 mm wafers, while all other semiconductor materials are being manufactured on smaller wafer sizes. In addition C2W enables testing of every die prior to stacking, which allows true *known good die* manufacturing. Figure 2.10 shows the difference between C2W and W2W integration. A fourth stacking method

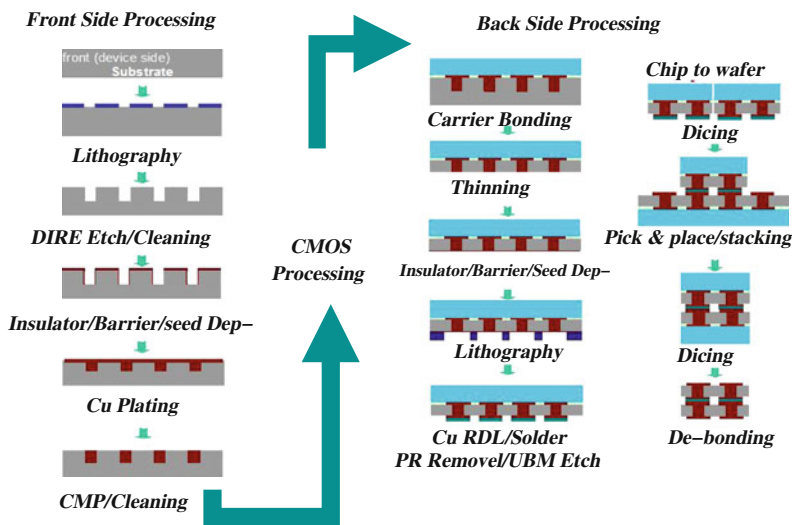


Fig. 2.9 A typical 3D Via-mid stacking process integration: *Front-side* and *Back-side* processing methods

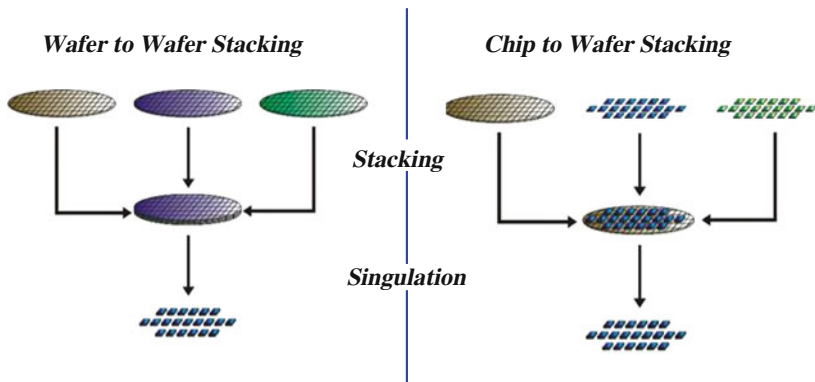


Fig. 2.10 3D Integration methods: Wafer-to-Chip and Wafer-to-Wafer stacking

and well advanced in today’s FPGA industry is silicon interposer-based integration (called horizontal or 2.5D integration), vertical die to die stacking (also called 3D stacking), and a range of mixed configurations. An interposer-based stacking gained popularity last year because of several attractive applications [35] as well as its technological feasibility. It might not be sufficiently effective for other applications, however, such as the memory on logic [36] or the logic splitting application, where the logic is split between two or more dies that are then put on top of each other for shorter interconnections. Also memory can be split in such a way that read-write

logic is on one chip while the cells are on the other. A true 3D stacking is needed for maximum performance in those applications.

2.5 Challenges in 3D Physical Design

The introduction of the third dimension has significantly increased the complexity of the integrated circuit design process. The 3D design and integration faces enormous challenges in both manufacturing technology and physical design. The major challenge is to define the characteristics of the verticals interconnects and the constraints that this type of interconnects poses on physical design process and other typical problems are reuse of existing 2D-IP blocks, testability, CAD tools and thermal issues. While thermal integrity is a critical issue in all high performance chip design, since the system reliability is strongly dependent on the temperature and this problem is even more significant for 3D designs due to the high power density in the stacked arrangement. Increasing the number of tiers that can be integrated into a single 3D system is a primary objective of 3D integration. A 3D system with high-density vertical interconnects is therefore indispensable. Vertical interconnects implemented as TSVs produce the highest interconnect bandwidth within a 3D system, as compared to wire bonding, peripheral vertical interconnects, and solder-ball arrays. Alternatively, the density of this type of interconnect dictates the granularity of the interconnected layers of the system, directly affecting the inter-tier communication bandwidth. Other important criteria should also be satisfied by the TSV fabrication process. A fabrication process for vertical interconnects should produce reliable and inexpensive TSVs. A high TSV aspect ratio, the ratio of the diameter of the top edge to the length of the via, may also be required for certain types of 3D circuits. The effect of forming the TSVs on the performance and reliability of neighboring active devices should also be negligible.

The electrical characteristics of the TSVs are of primary importance in 3D-ICs and are considerably different from the horizontal interconnect segments [37], as described by recent electrical models [38]. This situation is due to the structure of these interconnects and the diverse technologies, such as CMOS and SOI, that can exist in a 3D system. Producing low resistance and capacitance TSVs is a fundamental objective of manufacturing technologies. Finally, not properly characterizing the contribution of the TSVs to the delay of the critical inter-tier interconnect can result in significant inaccuracy in the performance of a 3D system [39]. Consequently, these structures must be carefully considered during the 3D physical design process. The thermal traits of the TSVs are also significant, as these vias can affect the thermal behavior of a 3D-IC. TSVs can be used to provide high thermal conductivity paths to facilitate the flow of heat from the upper tiers to the tiers attached to the heat sink, maintaining the temperature of a 3D circuit within acceptable levels. Materials with low thermal resistance, such as copper, are therefore preferred.

2.5.1 Complexity of 3D Physical Design Tools and Their Limitations

The solution space for classical physical design methodologies increases significantly in 3D systems, as the physical distance of two circuit cells is reduced not only by placing these cells near each other on the same tier but also by placing the cells in vertically adjacent locations. This situation results in a formidable increase in the number of solutions that can be explored, resulting in an exponential growth in the computational time. The increase in the number of metal layers yields similar computational issues for the routing task [40]. Computationally efficient heuristic algorithms are the primary tool to manage the dramatic increase in the solution space for 3D circuits. Methods such as simulated annealing (SA) and genetic algorithms complete the mosaic of the 3D physical design process [35, 41]. The main challenge in 3D physical design is dealing with tools that are not specifically designed to meet their needs. There are several works presented in the literature that describe various 3D system design options and physical design algorithms for 3D-ICs, but very few in the area of 3D design demonstration and methodology.

One quick solution to the lack of physical design tools for 3D-ICs is to build so-called *pseudo* 3D tools, which are based on straightforward extension of existing tools for 2D-ICs [30]. These pseudo 3D tools are able to handle simple 3D designs, wherein existing 2D designs are simply stacked and connected without any major design change. A good example of this is 3D stacking of processor and memory dice, where the only change required is to add TSVs in the layouts to deliver signal, power, and clock in vertical directions. This can be done by adding TSVs in the layout whitespace or by slightly modifying the layout to leave space for TSVs and wires. These TSVs are then treated as pseudo IO pads in the layout. In addition, traditional objectives, such as wire length and area, are insufficient for 3D circuits, particularly heterogeneous multi-tier integrated systems. Since these systems can combine disparate technologies, such as radio frequency (RF), analog, and digital circuits, other objectives, such as noise and signal integrity, need to be simultaneously considered in addition to conventional objectives. These objectives require the synergistic development of design methodologies, which previously were individually developed for each type of circuit. However, future trends in 3D-IC design calls for finer-grained 3D optimizations, such as 3D module floorplanning or 3D gate placement across the tiers for performance and power consumption improvement. In addition the number of tiers in the stack is expected to increase in order to meet the demand for higher-level system integration. These trend requires more powerful native 3D physical design tools that are built from ground up and are capable of handling many tiers and many TSVs simultaneously while addressing the current and emerging issues like cost, reliability, and manufacturability. In addition TSV and thermal-aware 3D design, verification, and analysis tools including 3D DRC/LVS, timing, power, signal integrity, power integrity and clock integrity analysis tools need to be seamlessly integrated and efficiently managed.

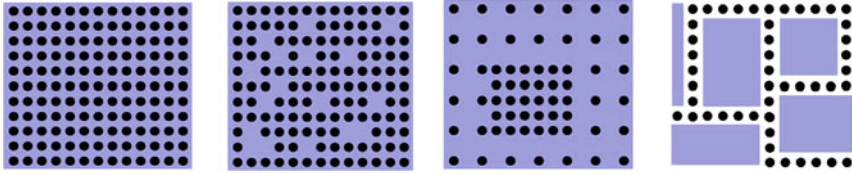


Fig. 2.11 TSV placement styles for 3D Stacked chips: Regular and non-regular placement for improving design quality and thermal profile of the chip

2.5.2 TSV and Thermal Management

TSV management is at the heart of physical design for 3D-ICs. Especially, the count and location of TSVs have significant impact on the quality and reliability of 3D-IC layouts. A recent study [42] shows that the overall wire length-up to a certain point reduces as more TSVs are used in the 3D layout. The number of TSVs used in 3D-IC layout entirely depends on how the design is partitioned into multiple dies. Research is needed to determine the optimal partitioning styles for given applications. Possible solutions include tradeoff studies among core-level, block-level, and gate-level partitioning across the dies in the 3D stack. Research is also required to investigate the impact of TSV location on 3D-IC design quality and reliability [43]. Possible solutions include trade-off studies between regular and non-regular TSV placement [43] with respect to these metrics, as illustrated in Fig. 2.11. TSV cost is another important factor that needs to be addressed during physical design. The cost of TSV depends on geometry-related data such as the pitch, diameter, and aspect ratio as well as the materials used for the TSV fill and liner. Moreover, the total number of TSVs used in the layout significantly affects the overall cost of the 3D-ICs. It is important to model and balance the trade-offs between the cost and other metrics such as performance, power, reliability, and manufacturability during physical design with TSVs.

A 3D system consists of disparate materials with considerably different thermal properties including semiconductor, metal, dielectric, and possibly polymer layers used for plane bonding. Although the power consumption of these circuits is expected to decrease due to the considerably shorter interconnects, the power density increases since there is a greater number of devices per unit volume as compared to a 2D circuit. As the power density increases, the temperature of the planes nonadjacent to the heat sink of the package can rise, resulting in degraded performance or thermal gradients that can accelerate wear out mechanisms [44, 45]. Design methodologies at various stages of the IC design flow, such as synthesis, floorplanning, and placement and routing, which maintain the temperature of a circuit within specified limits or alleviate thermal gradients among the tiers of the 3D circuit, are therefore necessary. Two key elements are required to establish a successful thermal management strategy: a thermal model, to characterize the thermal behavior of a circuit, and design techniques that alleviate thermal gradients among the physical layers of a 3D stack while maintaining the operating temperature within acceptable levels. The primary

requirements of a thermal model are high accuracy and low complexity [46–48], while thermal design techniques should produce high-quality circuits without incurring long computational design time [49]. To reduce the complexity of the modeling process, standard methods to analyze heat transfer, such as finite difference, finite element, and boundary element methods, have been adopted to evaluate the temperature of a 3D circuit. Simpler analytic expressions have also been developed to characterize the temperature within a 3D system.

Thermal design techniques can be classified into two categories: thermal strategies that improve the thermal profile of a 3D circuit without requiring any redundant interconnect resources for thermal management and those methodologies that are an integral part of a more aggressive thermal policy that utilize thermal TSVs, sacrificing other design objective(s). The thermal aware design techniques uses the location and spatial distribution of TSV to accurately estimate the temperature profile of the 3D chip. As discussed earlier, TSVs are made of copper or tungsten and they are good thermal conductors. By carefully arranging the TSVs, it is possible to transfer the heat efficiently from the tiers far from heatsink towards the tiers placed near to heatsink. To do this, we need to include 3D thermal analysis tool to the physical design flows to create thermal aware design tools. As described in Fig. 2.11, depending of the type of design, a uniform or a non-uniform TSV distribution can be used to effectively transfer heat from one layer to another. There are also more aggressive thermal management methods using redundant interconnect resources. These TSVs are typically called thermal or dummy vias [10] to emphasize the objective of conveying heat rather than providing signal communication for circuits located on different physical layers. Thermal wires can also be employed to transfer heat [50]. Thermal wires correspond to those horizontal wires that connect regions with different thermal via densities through thermal inter-tier vias.

2.5.3 Power and Clock Delivery in 3D-ICs

On-chip power delivery is a major challenge in 3D-IC design. In 3D ICs, the on-chip power-ground (P/G) networks in several tiers are vertically connected with P/G TSVs, leading to much higher current demand per TSV. The number of TSVs used in the 3D P/G network is also limited so as to prevent placement and routing congestion. In addition, signal routing must be done carefully to prevent coupling noise between P/G TSVs and signal wires. This complex optimization problem usually results in larger area, more power consumption, and more noise, which leads to less performance and diminishing benefit of TSV-based 3D-IC technology. Research needed on P/G network synthesis, optimization, and analysis to addresses these issues while minimizing on-chip resource usage such as P/G wires, P/G TSVs. The sequential elements in 3D ICs (i.e., flip-flops and latches) are potentially located in all of the dies in the 3D stack. This poses a major challenge in delivering clock signal to all of them while reducing power consumption, skew, slew, and jitters. A recent study [51] shows that more clock TSV usage up to a certain point translates to more wire length

reduction and thus power saving. However, clock TSVs, as in the case with signal and P/G (Power and Ground) TSVs, occupy layout space and causes coupling. Thus, clock TSV management becomes an important issue in 3D clock tree synthesis. In addition, the high thermal variations in 3D ICs induce a substantial amount of skew variation in the clock tree, which has adverse implications for the performance and reliability of 3D-ICs. The 3D clock tree itself is the longest wire in the circuit and contains many buffers to control skew and slew. Since the delay characteristics of clock wires, buffers, and TSVs are significantly affected by the temperature, care must be taken to ensure that the skew is kept minimum based on a given non-uniform thermal profile.

2.5.4 TSV-Induced Design for Manufacturability Issues

Primarily due to their large size compared with other layout objects, TSVs in 3D-IC layouts cause significantly non-uniform layout density distributions on the active, poly, and M1 layers. This density variation issue is expected to cause trouble during chemical-mechanical polishing (CMP) steps in the BEOL processing of the individual die, and requires new TSV-aware solutions. In addition, the printability of the devices and wires nearby TSVs will be affected in a non-negligible way. The CTE (coefficient of thermal expansion) mismatch between TSV copper and silicon causes significant stress to the devices nearby during manufacturing and operation of the 3D ICs. This in turn affects the timing characteristics of the devices and thus the overall circuit performance. The reliability of substrate and devices nearby TSVs is also affected because the thermal hotspots created in the regions cause repeated thermal expansion and contraction during 3D IC operation. This transient thermal behavior, together with the residual stress from TSV fabrication, may cause cracking and other physical damage in the substrate and devices. Research efforts required to address these issues during physical design. Possible solutions include TSV-aware CMP fill synthesis for the top and bottom metal layers, TSV stress-aware timing analysis and physical design [52], and TSV-aware substrate and device reliability modeling and optimization. TSVs are significantly larger than devices and local interconnects and thus complicates physical design and optimization for 3D layouts. Accurate electrical, mechanical, and thermal modeling of TSVs is essential in successful physical design of TSV-based 3D-ICs. In addition, full-chip layout construction and analysis for 3D-ICs should consider the impact of TSVs on performance, power, reliability, manufacturability, and cost.

2.5.5 Floorplanning for 3D Circuits

The predominant design objective for floorplanning a circuit has traditionally been to achieve the minimum area or, alternatively, the maximum packing density while

interconnecting these blocks with minimum length wires. Most floorplanning algorithms can be classified as either slicing [53] or nonslicing [54, 55]. Floorplanning techniques belonging to both of these categories have been proposed for 3-D circuits [56–59]. An efficient floorplanning technique for 3-D circuits should adequately handle two important issues: representation of the third dimension and the related increase in the solution space. Conventional floorplanning assumes a single 2D layer on which several modules must be arranged. A wide variety of different algorithmic approaches have been used in order to solve the floorplanning problem. 3D floorplanning includes new 3D-specific characteristics that must be represented in the underlying data structures. For example, high output power modules need comprehensive consideration, such as thermal-driven floorplanning [60] and vertical dependencies arise in addition to horizontal ones.

There are two ways to represent the vertical dependencies. The first possibility is the multiple usage of classical data structures, so-called 2.5D methods. Here, additional mechanisms have to be implemented to consider vertical relations between module placed in different tiers, such as vertical alignments as well as overlapping and non-overlapping constraints. The representations include a discrete z -direction, such as the combined bucket and 2D array approach (CBA) in [61]. Vertical dependencies must be incorporated directly into the data structure to prevent invalid solutions without time-consuming evaluations as well as to minimize the solution space. More recent data structures for floorplanning represent multilayer modules in the three dimensions. An example of such a data structure is 3D Slicing Tree described in [53, 62]. As illustrated in Fig. 2.12, different operations, such as module rotation and swapping, can be carried out efficiently to modify the given tree. A concatenation of these operations allows obtaining any possible slicing tree from any given slicing tree. However solutions from a 3D-Slicing Tree are limited to slicing floorplans.

2.5.6 Placement for 3D Circuits

Placement algorithms have traditionally targeted minimizing the area of a circuit and the interconnect length among the cells, while reserving space for routing the interconnect. In vertical 3D-IC integration, a placement dilemma arises in deciding whether two circuit cells sharing a large number of interconnects can be more closely placed within the same tier or placed on adjacent physical tiers, decreasing the interconnection length. Placing the circuit blocks on adjacent tiers can often produce a line with the shortest wire-length to connect these blocks. An exception is the case of small blocks within an SiP where the length of the inter-tier vias is greater than $100\mu\text{m}$ [63, 64]. Placement methodologies have also been discussed where other objectives, such as thermal gradients among the physical tiers and the temperature of the tiers [65], are considered. Several approaches have been adopted for placing circuit cells within a volume [66–70]. Different types of circuit cells for various 3D technologies have been investigated in [36]. Layout algorithms for these cells have also been devised, demonstrating the benefits of 3D integration. Since TSVs consume

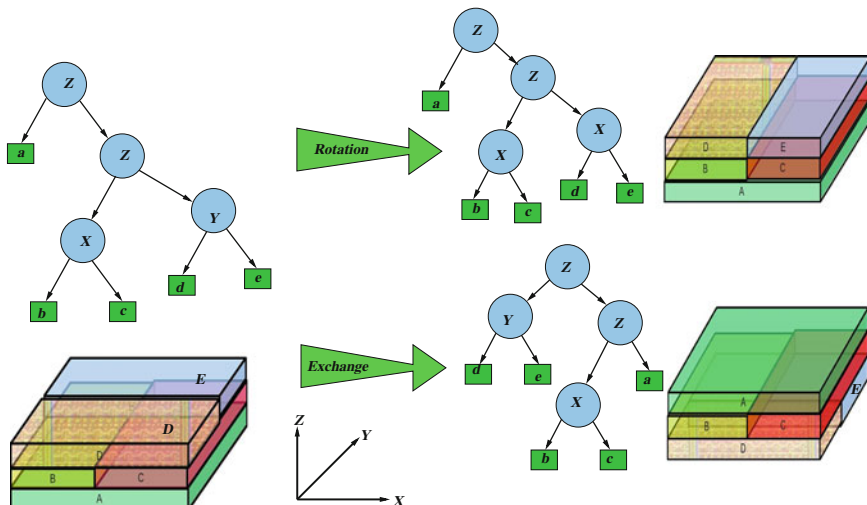


Fig. 2.12 Illustration of 3D Slicing Tree operation to permute a given 3F floorplan: A rotation alters an inner node (representing a cut through the normal plane) resulting in a physical rotation of modules contained in the sub-trees of that node. An exchange swaps two sub-trees resulting in a physical exchange of modules contained in these sub-trees

silicon area, possibly increasing the length of some interconnects, an upper bound on this type of interconnect resource is necessary. Alternatively, sparse utilization of the vertical interconnects can result in insignificant savings in wire length. To consider the effect of the vertical interconnects, a weighting factor has been used to increase the distance in the vertical direction, controlling the decision as to where to insert the inter-tier vias [69]. This weight essentially behaves as a controlling parameter that favors the placement of highly interconnected cells within the same or adjacent physical tiers. Alternatively, TSVs are treated as circuit cells since these interconnects occupy silicon area [71] and are included in the individual cell placement process within each tier. Since this approach can result in two different locations for placing a TSV, as illustrated in Fig. 2.13, a weighted average distance between these two locations can be utilized to place a TSV [71]. Although these approaches consider the location of the TSV, the fundamental objective is to decrease the interconnect length. The maximum achievable reduction in the interconnect length for the longest on-chip interconnect is proportional to \sqrt{n} , where n is the number of tiers constituting a 3D circuit [8]. Any further improvement in the performance of the inter-tier interconnects can be obtained by considering the electrical characteristics of the TSV.

Multi-objective placement techniques for 3D circuits are necessary to generate efficient 3D floorplans. Additional objectives that affect both the cell placement and wire length are simultaneously considered. The force directed method is a well-known technique used for cell placement [72], where repulsive or attractive forces are placed on the cells as if these cells are connected through a system of springs. The force directed method has been extended to incorporate the thermal objective

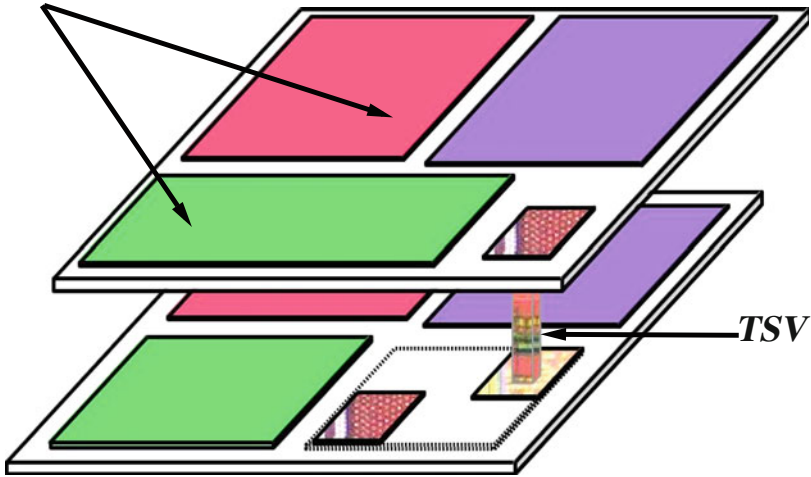
Circuit blocks

Fig. 2.13 Treating the TSVs as circuit cells on different planes can result in two different locations for placing a TSV. These locations define a region in which the TSV can be placed to satisfy different design objectives

during the placement process [73]. In this approach, repulsive forces are applied to those blocks that exhibit high temperatures (i.e., *hot blocks*) to ensure that the high-temperature blocks are placed at a greater distance from each other. The efficiency of this force directed placement technique has been evaluated on the MCNC [74] and IBM-PLACE benchmarks [75], demonstrating a 1.3 % decrease in the average temperature, a 12 % reduction in the maximum temperature, and a 17 % reduction in the average thermal gradient. The total wire length, however, increases by 5.5 %. As demonstrated by these results, this technique primarily achieves a uniform temperature distribution across each plane, resulting in a significant decrease in thermal gradients as well as the maximum temperature. The average temperature throughout a 3D-IC, however, is only slightly decreased. As a more practical example that demonstrates the need to include the thermal objective in 3D physical design techniques, consider an Intel Pentium 4 processor, which has been redesigned in two planes [76]. The increased power density due to stacking can increase the peak temperature within the 3D processor by approximately 26 °C, as compared to the original 2D system if thermal issues are ignored [76]. This increase can significantly degrade the performance and reliability of the processor. If the thermal objective is incorporated during the placement process, a negligible 2 °C increase is observed [76]. Alternatively, additional TSVs that do not function as a signal path can be utilized to further enhance the heat transfer process. The design objective is to identify those regions where thermal vias are most needed (hot-spots) and place thermal vias within those regions at the appropriate density. Such an assignment, however, is mainly restricted by two factors; the routing blockage caused by these vias and the size of the

unoccupied regions or white space that exist within each tier. Although thermal via insertion can be applied as a post-placement step, integrated techniques produce a more efficient distribution of the thermal TSVs for the same temperature constraint [77, 78]. One advantage of this approach is the large granularity with which the thermal analysis method could work. The thermal conductivity of each region can be treated as a design variable that is only subsequently translated into a precise number of thermal vias placed inside this region. The integrated technique requires 16 % fewer thermal vias for the same temperature constraint, with a 21 % increase in computational time and an almost 3 % reduction in total area.

2.5.7 Routing for 3D Circuits

Routing is the most complex and least developed of the physical design techniques used in 3D circuits. During the routing stage, all terminals of the nets in the circuits netlist must be properly connected while respecting the constraints, such as design rules, routing resources capacities and optimizing routing objectives like minimize total wire-length, maximum timing slack etc. The multiple metal layers available for routing on each physical layers exacerbate the difficulty in routing a net connecting several circuit cells located on different layers. As these interconnects also compete with the transistors for silicon area, routing is a formidable task for 3D circuits. An early paper on routing 3D circuits demonstrated several issues related to this physical design task [79]. Consequently, several heuristics have been developed that address routing in the third dimension [80, 81]. The main difference between the 2D and 3D routing is caused by the multi-tier position of the net terminals that lead to net topologies which span more than one tier as illustrated in Fig. 2.14. This requires expensive inter-tier vias to be used in addition to regular signal vias which connect metal layers within the same tier. An effective approach for routing 3D circuits is to convert the routing inter-tier interconnect problem into a 2D channel routing task, as the 2D channel routing problem has been efficiently solved [82, 83]. A number of methods can be applied to transform the problem of routing the inter-tier vias into a 2D routing task, which requires utilizing a portion of the available routing resources for inter-tier routing (usually the top metal layers). Inter-tier interconnect routing can be implemented in five major stages including inter-tier channel definition, pseudoterminal allocation, inter-tier channel creation (channel alignment), detailed routing, and final channel alignment [80]. Additional stages route the 2D channels, both the inter-tier and intra-tier vias, and perform channel ordering to determine the wire routing order for the 2D channels.

Alternatively, multilevel algorithmic techniques [84] have been applied to route 3D circuits. The advantages of multilevel routing are the lower computational time and higher completion rates as compared to flat and hierarchical routers. Multilevel routing can be treated as a three stage process: a coarsening phase, an initial solution generation at the coarsest level (level p) of the grid, and a subsequent refinement process until the finest level of the grid is reached. Before the coarsening phase

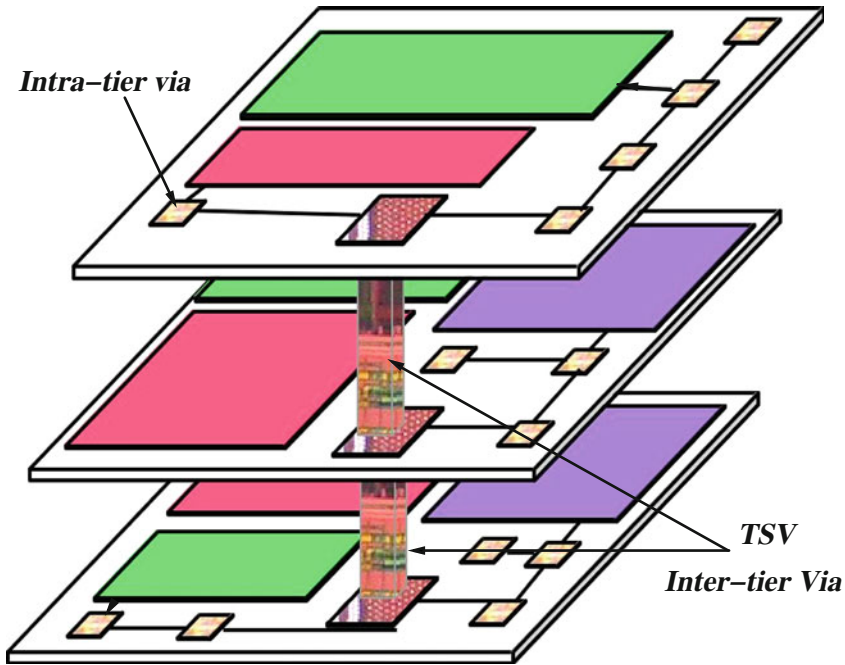


Fig. 2.14 Example route for a net in a three-tier 3D design

is initiated, the routing resources in each unit block of the grid are determined by a weighted area sum model. The routing resources are allocated during each coarsening step. The resources for the local nets within a block are transferred at each coarsening step. At the coarsest level, an initial routing tree is generated. This initial routing task commences with a minimum spanning tree for each multi-terminal net. A Steiner tree heuristic and a maze searching algorithm generate a 3D Steiner tree for each of these interconnects. Additionally, the TSVs are estimated for each block. During the last phase, the initial routing tree is refined until the finest level is reached. In this refinement phase, the signal (and thermal) TSVs are successively assigned and distributed within each block. The routing of the wires follows the refinement of the TSVs. At the finest level, a detailed router completes the routing of the circuit [84].

Multilevel routing for 3D-ICs has been extended to include the thermal objective [85, 86]. A thermal-driven 3D router using a multilevel routing approach composed of a recursive coarsening, an initial routing, and recursive refinement process presented in [85]. The major milestone of this model is the thermal-driven via planning algorithm. Based on this global view and capabilities of a multilevel planning scheme, the via planning step effectively optimize the temperature distribution and wire-length using direct planning of the inter-tier vias instead of indirect planning through a routing path search. This approach allows to control the chip temperature effectively. It also should be noted that any inter-tier via is also considered as a

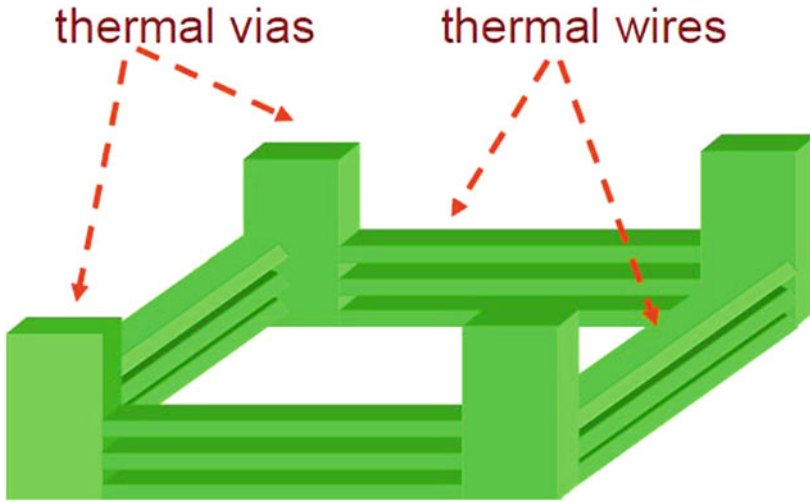


Fig. 2.15 An illustration of 3D thermal net designed to transfer heat vertically and horizontally from one location to the other

thermal via. The approach provides flexibility to add dummy inter-tier vias when the signal inter-tier vias number is not sufficient to bring down the chip temperature to an acceptable level. An initial routing solution is built using a 3D minimum spanning tree (MST) for each multi-pin net. Obstacles, such as thermal via regions, are avoided by using a simple maze routing algorithm. Then, the number of dummy inter-tier vias to be inserted is estimated using binary search. The upper bound of dummy inter-tier via numbers that can be inserted into each device layer is estimated by the amount of whitespace between the blocks. During each refinement stage, the inter-tier vias are refined first to minimize wire-length and temperature. This via-refinement process includes two steps, inter-tier via number distribution and signal inter-tier via assignment. These steps try to optimize temperature and wire-length, respectively. After inter-tier via refinement, wires are also adjusted according to the updated via positions. Another approach is presented in [50]. It tackles the temperature-aware 3D routing problem not only by using thermal vias but also by introducing the concept of thermal wires. Thermal wires are objects with the function of spreading thermal energy in the lateral direction. Thermal vias perform the bulk of the conduction to the heat sink, while thermal wires help distributing the heat paths among multiple thermal vias. This strategy not only limits the temperature impact on the delay of signal nets, but also reduces congestion in hot regions. This is beneficial since more thermal vias may be inserted later into these regions to reduce the chip temperature. Figure 2.15 illustrate a model thermal net that is used in modern 3D chip design to transfer heat vertically and horizontally. The thermal nets are constructed using TTSVs and horizontal metal wires specially designed for heat transfer. The width and length of horizontal thermal wires can be bigger than horizontal signal wires.

2.6 3D-IC Design Verification

Many of the capabilities required for successful TSV design verification exist today in some EDA tools that are commercially available. There are, however a number of significant omissions and obstacles to avoid in *standard* physical verification methodologies. Some re-factoring of the tired and true design methodologies that are in place today is needed to accommodate TSV design structures as part of the verification landscape. The progress that take place EDA industry are evolutionary, rather than a revolutionary, approach in developing the 3D IC design tools. This appears to be a good decision because the technology, the rules and the standards are still evolving. The main EDA challenges are expected in the design space exploration [87], automatic across-die design partitioning, placement and routing, thermal and stress management, and 3D stack testing.

In the design space today, the location of each TSV is carefully orchestrated and tracked. A precise connection is made to each specific micro-bump on another die designed for the match, or other commodity chip with pre-defined locations. A commodity chip might be a memory, for example that is available from multiple sources, with same TSV pin-out and compatible characteristics. In such scenarios, TSV locations are deliberate and precise, acting more like an embedded connector than a traditional via. Regardless of the design complexities and the perceived need for new design methodologies for TSV design, there is still a fundamental need for a separate physical verification flow. An increase in complexity is the design domain does not necessarily have to follow into verification complexity increase of the same magnitude. Regardless of design style and methodology, physical verification is a necessary step to accurately verify design rule compliance, 3D stack LVS checking across the die parasitic extraction and simulation. Existing verification flows include the use of DRC, LVS and extraction to verify the connectivity of multiple stacked dies [88]. 3D-IC designs that utilize TSVs are essentially a double sided die. The TSV connects the regular front metal stack and back metal stack as illustrated in Fig. 2.16. The back metal stack provides for routing flexibility and consists of one or two layers. TSVs typically connect the first metals in the front (M1) and back metal (M6 or higher) stacks are manufactured using *via-first* process sequence and the TSVs go through the entire metal stacks are manufactured using *via-last* process sequence and result in smaller TSV densities since they require significant area to pass through the metal stacks. Various TSV models have been proposed ranging from piratically ignoring the TSVs altogether in verification (i.e. modeling them as single small resistance), to the complex models based of fitting S-parameter measurements with the parameter of TSV model [32]. Electrical characteristics of the TSV depend on its physical dimensions, size and thickness of its liner as well as on the material characteristics of silicon substrate. At the present stage of technology development and 3D-IC applications, it is assumed that there are no interactions between the TSVs, and a model for a single TSV is provided by the foundries. For verification purposes, TSVs are treated as an LVS device (GDS based flow) or as a Via (LEF/DEF based flow), and the provided spice TSV model of arbitrary complexity to be used for

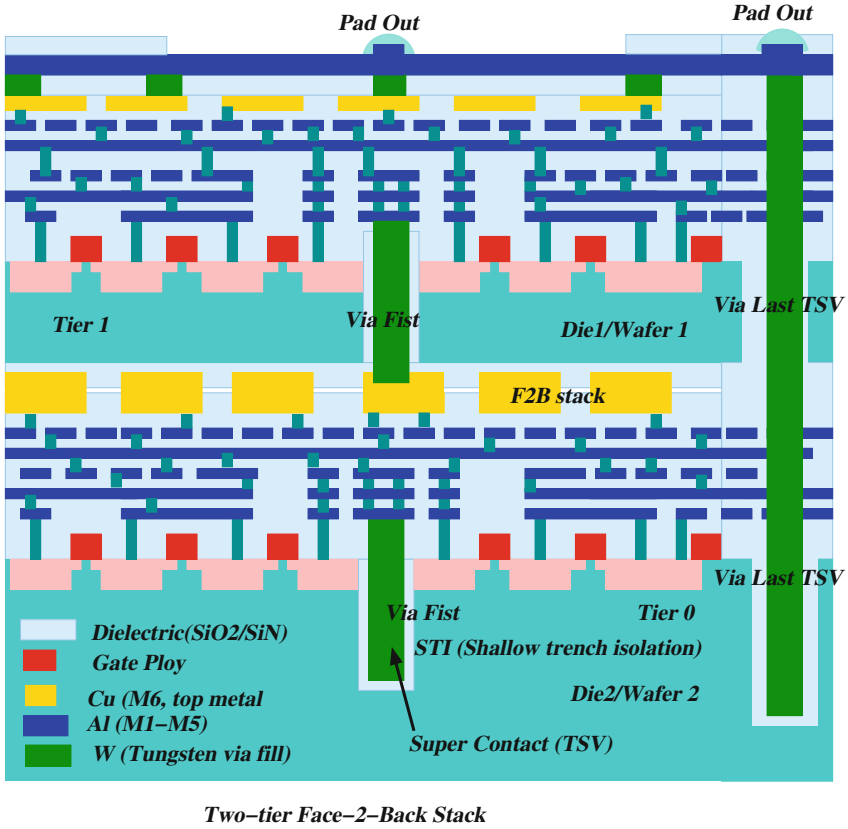


Fig. 2.16 Via first and via last with front and back metal stack

downstream simulation. This assumption, however, may not hold true as the technology advances and the TSV densities and frequencies become high, requiring accurate modeling and extraction of the interactions. Significant research effort has been put into this area recently [89–92] and it is expected to intensify in the coming years. This new methodology would require more accurate process description, accurate frequency dependent modeling and appropriate flow development to take advantage of the modeling accuracy.

2.7 Summary

Developing a design flow for 3D-ICs is a complicated task with many ramifications. Design methodologies at the frontend and mature manufacturing processes at the backend are required to effectively provide large scale 3D systems. Physical design

techniques at different stages of a developmental design flow for 3D circuits have been discussed in this chapter, emphasizing the effect of the 3D nature on each design stage. A variety of floorplanning, placement, and routing techniques and algorithms for 3D circuits have been described that consider the unique characteristics of 3D circuits. In these techniques, the discrete nature of the third dimension is exploited to decrease the number of candidate solutions and, consequently, the computational time required to design a 3D circuit. Due to increased power densities and greater distances between the circuits on the upper planes and the heat sink, physical design techniques that embody a thermal objective can be a useful mechanism to manage thermal issues in 3D-ICs. Design techniques can reduce thermal gradients and temperatures in 3D circuits by redistributing the blocks among and within the planes of a 3D circuit. Alternatively, thermal vias can be utilized in 3D circuits to transfer heat to the heat sink. Thermal wires in the horizontal direction are similar in function to thermal vias and can also be utilized to lower thermal gradients within 3D circuits.

Another requirement for maximizing the speed of 3D circuits is to reliably distribute the clock signal within these circuits. A 3D clock distribution network, however, cannot be directly extended from a 2D circuit due to the asymmetry of a multi-tier 3D circuit and the effect of the inter-tier via impedance. Several clock distribution networks have been developed to investigate synchronization issues in 3D systems. In addition to higher performance, 3D integration offers significant opportunities for designing highly diverse and complex systems. Research on the design of 3D-ICs has only recently begun to emerge. Many challenges remain unsolved and significant effort is required to provide effective solutions to the problems encountered in the design of 3D-ICs. Furthermore, distributing power to the tiers of the stack located far from the power/ground pads is another fundamental issue in 3D-ICs. As the power/ground pads are typically located along the edges of the plane, providing sufficient current while satisfying target voltage levels for every transistor within a 3D-IC requires innovative power distribution networks. Addressing these important design issues will considerably accelerate the development of commercial 3D integrated systems.

References

1. G. Moore, Cramming more components onto integrated circuits. *Proc. IEEE* **86**(2), 82–85 (1998)
2. A. Rahman, A. Fan, J. Chung, R. Reif, Wire-length distribution of three-dimensional integrated circuits, in *Proceedings of the IEEE International Interconnect Technology Conference*, pp. 233–235, May 1999
3. A. Rahman, R. Reif, System level performance evaluation of three-dimensional integrated circuits. *IEEE Trans. Very Large Scale (VLSI) Syst.* **8**, 671–678 (2000)
4. D. Stroobandt, J. Van Campenhout, Accurate interconnection lengths in three-dimensional computer systems. *IEICE Trans. Inform. Syst. Spec. Issue Phys. Des. Deep Sub-micron* **10**(1), 99–105 (2000)
5. J.W. Joyner, Impact of three-dimensional architectures on interconnects in gigascale integration. *IEEE Trans. Very Large Scale (VLSI) Syst.* **9**, 922–928 (2001)

6. J.W. Joyner, P. Zarkesh-Ha, J.D. Meindl, A Stochastic global net-length distribution for a three-dimensional system-on-a-chip (3D-SoC), in *Proceedings IEEE International ASIC/SOC Conference*, pp. 147–151, Sep 2001
7. R. Zhang, K. Roy, C.-K. Koh, D.B. Janes, Stochastic interconnect modeling, power trends, and performance characterization of 3-D circuits. *IEEE Trans. Elect. Devices* **48**, 638–652 (2001)
8. J.W. Joyner, J.D. Meindl, Opportunities for reduced power distribution using three-dimensional integration, in *Proceedings of the IEEE International Interconnect Technology Conference*, pp. 148–150, June 2002
9. B.S. Cherkauer, E.G. Friedman, A unified design methodology for CMOS tapered buffers. *IEEE Trans. Very Large Scale (VLSI) Syst.* **3**, 99–111 (1995)
10. K. Banerjee, S.K. Souri, P. Kapour, K.C. Saraswat, 3D-ICs: A novel chip design paradigm for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proc. IEEE* **89**, 602–633 (2001)
11. M. Koyanagi et al., Future system-on-silicon LSI chips. *IEEE Micro* **18**, 17–22 (1998)
12. V.K. Jain, S. Bhanja, G.H. Chapman, L. Doddannagari, A highly reconfigurable computing array: DSP plane of a 3D heterogeneous SoC, in *Proceedings of the IEEE International System on Chip Conference*, pp. 243–246, Sep 2005
13. V.F. Pavlidis, E.G. Friedman, *Three-Dimensional Integrated Circuit Design* Morgan Kaufmann (2009). ISBN: 978-0-12-374343-5
14. R.J. Gutmann et al., Three-dimensional (3D) ICs: a technology platform for integrated systems and opportunities for new polymeric adhesives, in *Proceedings of IEEE International Conference on Polymers Adhesives Microelectron. Photon.*, pp. 173–180, Oct 2001
15. M. Healy et al., Multiobjective microarchitectural floorplanning for 2-D and 3-D ICs. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **26**, 38–52 (2007)
16. P. Garrou, C. Bower, P. Ramm, *Handbook of 3D Integration* (Wiley-VCH, New York, 2008). ISBN: 978-3-527-32034-9
17. R. Tummula, M. Swaminathan, *System-On-Package: Miniaturization of the Entire System* (McGraw-Hill, New York, 2008)
18. J.H. Lau, Critical issues of 3D IC integration, *IMAPS transactions. J. Microelectron. Electron. Packag.* (First Quarter Issue), 35–43 (2010)
19. J.H. Lau, Heart and Soul of 3D IC Integration, posted at 3D InCites on June 29 (2010), <http://www.semineedle.com/posting/34277>. Accessed 29 June 2010
20. K.W. Guarini, A.T. Topol, M. Jeong, R. Yu, L. Shi, M.R. Newport, D.J. Frank, Electrical integrity of state-of-the-art 0.13 μm SOI CMOS devices and circuits transferred for Three-dimensional (3D) Integrated Circuit (IC) fabrication, in *IEDM Technical Digest*, pp. 943–945, 2002
21. R. Berridge, R.M. Averill III, A.E. Barish, M.A. Bowen, P.J. Camporese, J. DiLullo, P.E. Dudley, IBM POWER6 microprocessor physical design and design methodology. *IBM J. Res. Dev.* **51**(6), 685–714 (2007)
22. Y. Orii, T. Nishio, Ultra-thin POP technologies using 50 μm pitch flip chip C4 interconnections, in *Presented at the Electronic Components and Technology Conference (ECTC)* (Reno, NV, 2007)
23. J.J.Q. Lu, R. Gutmann, T. Matthias, P. Lindner, Aligned wafer bonding for 3-D interconnect, <http://www.reed-electronics.com/semiconductor/article/CA630263>. Accessed Aug 2005
24. K. Takahashi, Y. Taguchi, M. Tomisaka, H. Yonemara, M. Hoshino, M. Ueno, Y. Egawa, Process integration of 3D chip stack with vertical interconnection, in *Proceedings of the 54th Electronic Components and Technology Conference*, pp. 601–609, 1–4 June 2004
25. M. Umamoto, K. Tanida, Y. Nemoto, M. Hoshino, K. Kojima, Y. Shirai, K. Takahashi, High performance vertical interconnection for high-density 3D chip stacking package. in *Proceedings of the 54th Electronic Components and Technology Conference*, pp. 616–623, 1–4 June 2004
26. M. Feil, C. Adler, D. Hemmetzberger, M. Konig, K. Bock, The challenge of ultra thin chip assembly, in *Proceedings of the 54th Electronic Components and Technology Conference*, pp. 35–40, 1–4 June 2004

27. M. Hutter, F. Hohnke, H. Oppermann, M. Klein, and G. Engelmann, Assembly and reliability of flip chip solder joints using miniaturized Au/Sn bumps, in *Proceedings of the 54th Electronic Components and Technology Conference*, pp. 49–57 (2004)
28. V. Kripeshm, S. Yoon, S.W. Yoon, V.P. Ganesh, N. Khan, M.D. Rotaru, W. Fang, M.K. Iyer, Three-dimensional system-in-package using stacked silicon platform technology. *IEEE Trans. Adv. Packag.* **28**(3), 377–386 (2005)
29. H. Ikeda, M. Kawano, T. Mitsuhashi, Stacked memory chip technology development, in *SEMI Technology Symposium (STS) 2005 Proceedings, Session 9*, pp. 37–42 (2005)
30. S. Gupta, M. Hilbert, S. Hong, R. Patti, *Techniques for Producing 3D ICs with High-Density Interconnect* (Tezzaron Semiconductor Naperville, IL, 2005)
31. R. Patti, Advances in 3D memory and logic devices, in *IMAPS International Conference on Device Packaging, TAI3* (Scottsdale, AZ, 2010)
32. D. Min Jang, C. Ryu, K. Yong Lee, B. Hoon Cho, J. Kim, T. Sung Oh, W. Jong Lee, J. Yu, Development and evaluation of 3-D SiP with vertically interconnected Through Silicon Vias (TSV), in *Proceedings 57th Electronic Components and Technology Conference, ECTC-07*, Reno, NV, pp. 847–852 (2007)
33. M. Sadaka, I. Radu, L. di Cioccio, 3D Integration: advantages, enabling technologies and applications, in *IEEE International Conference on IC Design and Technology (ICICDT)*, Grenoble, France, pp. 106–109 (2010)
34. S.J. Koester et al., Wafer level 3D integration technology. *IBM J. Res. Technol. IBM Res. Dev.* **52**(6), 585–597 (2008)
35. D.E. Goldberg et al., *Genetic Algorithms in Search, Optimization, and Machine Learning* (Addison-Wesley, Reading, 1989)
36. A. Harter et al., *Three-Dimensional Integrated Circuit Layout* (Cambridge University Press, Cambridge, 1991)
37. C. Ryu et al., High frequency electrical circuit model of chip-to-chip vertical via interconnection for 3-D chip stacking package, in *Proceedings of IEEE Topical Meeting Electrical Performance of Electronic Packaging*, pp. 151–154, Oct 2005
38. D.M. Jang et al., Development and evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV), in *Proceedings of the IEEE International Electronic Components Technology Conference*, pp. 847–850, June 2007
39. V.F. Pavlidis, E.G. Friedman, Interconnect delay minimization through interlayer via placement in 3-D ICs, in *Proceedings of the ACM Great Lakes Symposium on VLSI*, pp. 20–25, Apr 2005
40. S. Tayu, S. Ueno, On the complexity of three-dimensional channel routing, in *Proceedings of the IEEE International Symposium on Circuits Systems*, pp. 3399–3402, May 2007
41. C. Addo-Quaye, Thermal-aware mapping and placement for 3-D NoC designs, in *Proceedings of the IEEE International SOC Conference*, pp. 25–28, Sep 2005
42. D. Hyun Kim, S. Mukhopadhyay, S. Kyu Lim, Through-silicon-via aware interconnect prediction and optimization for 3D stacked ICs, in *ACM/IEEE International Workshop on System Level Interconnect Prediction* (2009)
43. J.U. Knickerbocker et al., Three-dimensional silicon integration. *IBM J. Res. Dev.* **52**(6) (2008)
44. T.-Y. Chiang, S.J. Souri, C.O. Chui, K.C. Saraswat, Thermal analysis of heterogeneous 3D-ICs with various integration scenarios, in *Proceedings of IEEE International Electron Devices Meeting*, pp. 681–684, Dec 2001
45. C.C. Liu, J. Zhang, A.K. Datta, S. Tiwari, Heating effects of clock drivers in bulk, SOI, and 3D CMOS. *IEEE Trans. Elect. Device Lett.* **23**(12), 716–728 (2002)
46. G. Digele, S. Lindenkreuz, E. Kasper, Fully coupled dynamic electro-thermal simulation, *IEEE Trans. Very Large Scale (VLSI) Syst.* **5**, 250–257 (1997)
47. Z. Tan, M. Furmanczyk, M. Turowski, A. Przekwas, CFD-micromesh: a fast geometrical modeling and mesh generation tool for 3D microsystem simulations, in *Proceedings of the International Conference on Modeling Simulation Microsystems*, pp. 712–715, March 2000
48. P. Wilkerson, M. Furmanczyk, M. Turowski, Compact thermal model analysis for 3-D integrated circuits, in *Proceedings of the International Conference on Mixed Design Integration of Circuits Systems*, pp. 277–282, June 2004

49. M.B. Kleiner, S.A. Kahn, P. Ramn, W. Weber, Thermal analysis of vertically integrated circuits, in *Proceedings of IEEE International Electron Devices Meeting*, pp. 487–490, Dec 1995
50. T. Zhang, Y. Zhang, S. Sapatnekar, Temperature-aware routing in 3D-ICs, in *Proceedings of the IEEE Asia South Pacific Design Automation Conference*, pp. 309–314, Jan 2006
51. X. Zhao, D. Lewis, H.H.S. Lee, S. Kyu Lim, Pre-bond testable low-power clock tree design for 3D stacked ICs, in *IEEE International Conference on Computer-Aided Design* (2009)
52. J. Yang, K. Athikulwongse, Y.J. Lee, S. Kyu Lim, D. Pan, TSV stress aware timing analysis with applications to 3D-IC layout optimization, in *ACM Design Automation Conference* (2010)
53. R.H.J.M. Otten et al., Automatic floorplan design, in *Proceedings of IEEE/ACM Design Automation Conference*, pp. 261–267, June 1982
54. X. Hong et al., Corner block list: an effective and efficient topological representation of non-slicing floorplan, in *Proceedings IEEE/ACM International Conference on Computer-Aided Design*, pp. 8–11, Nov 2000
55. E.F.Y. Yong, C.C.N. Chu, C.S. Zion, Twin binary sequences: a non-redundant representation for general non-slicing floorplan. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **22**, 457–469 (2003)
56. H. Yamazaki, K. Sakanushi, S. Nakatake, Y. Kajitani, The 3D-packing by meta data structure and packing heuristics. *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.* **E83-A**(4), 639–645 (2000)
57. Y. Deng, W.P. Maly, Interconnect characteristics of 2.5-D system integration scheme, in *Proceedings of the IEEE International Symposium Physical Design*, pp. 341–345, Apr 2001
58. L. Cheng, L. Deng, D.F. Wong, Floorplanning for 3-D VLSI design, in *Proceedings of the IEEE International Asia South Pacific Design Automation Conference*, pp. 405–411, Jan 2005
59. Z. Li et al., Hierarchical 3D floorplanning algorithm for wire length optimization. *IEEE Trans. Circuits Syst. I Regul. Pap.* **53**(12), 2637–2646 (2006)
60. P. Zhou, Y. Ma, Z. Li, R. Dick, L. Shang, H. Zhou, X. Hong, Q. Zhou, 3D-STAF: scalable temperature and leakage aware floorplanning for three-dimensional integrated circuits, in *Proceedings of the ICCAD*, pp. 590–597 (2007)
61. J. Cong, J. Wie, Y. Zhang, A thermal-driven floorplanning algorithm for 3D-ICs, in *Proceedings of ICCAD*, pp. 306–313 (2004)
62. L. Cheng, L. Deng, M.D.F. Wong, Floorplanning for 3D-VLSI design, in *IEEE International Asia South Pacific Design Automation Conference (ASPAC)*, pp. 405–411 (2005)
63. M.W. Newman et al., Fabrication and electrical characterization of 3D vertical interconnects, in *Proceedings of the IEEE International Electronic Components Technology Conference*, pp. 394–398, June 2006
64. W.-C. Lo et al., An innovative chip-to-wafer and wafer-to-wafer stacking, in *Proceedings of the IEEE International Electronic Components Technology Conference*, pp. 409–414, June 2006
65. B. Goplen, S. Sapatnekar, Placement of thermal vias in 3D-ICs using various thermal objectives. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **25**, 692–709 (2006)
66. M. Ohmura et al., An initial placement algorithm for 3D VLSI, in *Proceedings of IEEE International Symposium on Circuits Systems*, vol. IV, pp. 195–198, May 1998
67. T. Tanprasert et al., An analytical 3D placement that preserves routing space, in *Proceedings of the IEEE International Symposium on Circuits Systems*, vol. III, pp. 69–72, May 2000
68. Y. Deng, W.P. Maly, Interconnect characteristics of 2.5D system integration scheme, in *Proceedings of the ACM International Symposium on Physical Design*, pp. 171–175, Apr 2001
69. I. Kaya, M. Olbrich, E. Barke, 3D Placement considering vertical interconnects, in *Proceedings of the IEEE International SOC Conference*, pp. 257–258, Sep 2003
70. S.T. Obenaus, T.H. Szymanski, Gravity: fast placement for 3-D VLSI. *ACM Trans. Des. Autom. Electron. Syst.* **8**(3), 298–315 (2003)
71. W.R. Davis et al., Demystifying 3D-ICs: the pros and cons of going vertical. *IEEE Des. Test Comput.* **22** (2005)
72. H. Eisenmann, F.M. Johannes, Generic global placement and floorplanning, in *Proceedings of IEEE/ACM Design Automation Conference*, pp. 269–274, June 1998

73. B. Goplen, S. Sapatnekar, Efficient thermal placement of standard cells in 3D-ICs using a force directed approach, in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 86–89, Nov 2003
74. MCNC Benchmarks, <http://er.cs.ucla.edu/benchmarks/ibm-place>
75. IBM-PLACE Benchmarks, http://www.cbl.ncsu.edu/pub/Benchmark_dirs/LayoutSynth92
76. B. Black et al., Die stacking (3D) microarchitecture, *Proceedings of IEEE/ACM International Symposium on Micro-architecture*, pp. 469–479, Dec 2006
77. B. Goplen, S. Sapatnekar, Thermal via placement in 3D-ICs, in *ISPD*, pp. 167–174 (2005)
78. Z. Li et al., Efficient thermal via planning approach and its application in 3D floorplanning. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **26**, 645–658 (2007)
79. R.J. Enbody, G. Lynn, K.H. Tan, Routing the 3D chip, in *Proceedings of IEEE/ACM Design Automation Conference*, pp. 132–137, June 1991
80. C.C. Tong, C. Wu, Routing in a three-dimensional chip. *IEEE Trans. Comput.* **44**(1), 106–117 (1995)
81. J. Minz, S.K. Lim, Block-level 3D global routing with an application to 3D packaging. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **25**, 2248–2257 (2006)
82. A. Hashimoto, J. Stevens, Wire routing by optimizing channel assignment within large apertures, in *Proceedings of IEEE/ACM Design Automation Conference*, pp. 155–169, June 1971
83. T. Ohtsuki, E. Horbst, *Advances in CAD for VLSI: Logic Design and Simulation* (The University of Michigan, North-Holland, 1986). ISBN: 444878920, 9780444878922
84. J. Cong, M. Xie, Y. Zhang, An enhanced multilevel routing system, in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 51–58, Nov 2002
85. J. Cong, Y. Zhang, Thermal driven multilevel routing for 3D-ICs, in *Proceedings of the IEEE Asia and South Pacific Design Automation Conference*, pp. 121–126, June 2005
86. J. Cong, Y. Zhang, Thermal via planning for 3D-ICs, in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 744–751, Nov 2005
87. D. Milojevic, R. Radojcic, R. Carpenter, P. Marchal, Pathfinding: a design methodology for fast exploration and optimisation of 3D-stacked integrated circuits, in *International Symposium on System-on-Chip, 2009. SOC 2009*, pp. 118–123 (2009)
88. M. Hogan, D. Petranovic, Robust verification of 3D-ICs: Pros, Cons and Recommendations, in *IEEE International Conference on 3D System Integration, 2009. 3DIC*, pp. 1–6, 28–30 Sept 2009
89. J.H. Wu, Through-substrate Interconnects for 3-D Integration and RF systems. Ph.D. dissertation, MIT, Cambridge, MA, Oct 2006
90. I. Savidis, E.G. Friedman, Electrical modeling and characterization of 3-D vias, in *Proceedings of the IEEE International Symposium on Circuits Systems*, pp. 784–787, May 2008
91. I. Savidis, E.G. Friedman, Closed-form expressions of 3-D via resistance, inductance, and capacitance. *IEEE Trans. Electron Devices* **56**(9), 1873–1881 (2009)
92. D. Hyun Kim, K. Athikulwongse, S. Kyu Lim, A study of through-silicon-via impact on the 3D stacked IC layout, in *IEEE International Conference on Computer-Aided Design* (2009)

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