

Preface

Three-dimensional integrated circuits (3D-ICs) design has become a major driving force in the modern VLSI design and manufacturing technology. It provides the best platform for design and manufacturing of high density and high performance chips and the field is continuing to grow at an amazing pace. The idea to write this book on 3D FPGAs using 3D technology originated from the research and experimental work done during my doctoral studies at University of Pierre and Marie Curie under the guidance of Professor Habib Mehrez. This book was written as a text that covers the foundations of 3D integrated circuits and high performance 3D reconfigurable FPGA architecture design. It was written for use in a core and elective course at the graduate level in field of Electrical Engineering, Computer Engineering, and doctoral research programs. Today, many universities upgrade their curriculum to include modern VLSI design methodologies and re-configurable system design. No previous background on 3D integration is required, nevertheless, fundamental understanding of 2D CMOS VLSI design is required. It is assumed that the reader has taken the core curriculum in Electrical Engineering or Computer Engineering, with courses like CMOS VLSI design, Digital System Design and Microelectronics Circuits being the most important. It is accessible for self-study by both senior students and professionals alike.

Scope and Coverage

A brief introduction and the concept of 3D integration is presented in Chap. 1. It begins with brief review of advanced VLSI design and technology scaling; Chap. 1 continues to establish the basic and fundamental needs of introducing three-dimensional integrated circuits design into the modern VLSI technology. It also stress the needs for new and augmented 3D CAD tools to support designs such as, the *design for 3D*, to manufacture high performance 3D integrated systems and reconfigurable architecture. Three-dimensional (3D) integration is an emerging technology that is expected to lead to an industry paradigm shift due to its

tremendous advantages over 2D integration in terms of density and performance. Academic and industrial research institutes around the world currently focus on technology innovations, simulation and design and product prototypes. Anticipated applications start with memory, portable device and high-performance computers, reconfigurable system design and extend to high-density multifunctional heterogeneous integration of infotech-nanotech-biotech systems. Chapter 2 focusses on the fundamentals and in-depth analysis of different 3D integration methodologies and design. This chapter also talks about potential benefits of 3D integration that can vary depending on approach; they include multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs.

Today, FPGAs (Field Programmable Gate Arrays) have become important actors in the computational devices domain that was originally dominated by microprocessors and ASICs. The main challenge in 2D FPGA design is to find a good trade-off between flexibility and performances. Three factors combine to determine the characteristics of an FPGA: quality of its architecture, quality of the CAD tools used to map circuits into the FPGA and its electrical technology design. A first look at the FPGA hardware is provided in Chap. 3. The chapter provides in-depth analysis of programmable logic components and interconnection blocks in FPGA design and how they are interconnected to function as a generic reconfigurable system. This chapter establishes the basic understanding that FPGAs are semiconductor devices and contain programmable logic components connected by a regular, hierarchical programmable interconnect system. The distinguishing characteristic of FPGAs is their on-field programmability, which allows the logic functionality of an FPGA to be re-programmed even after the manufacturing process. FPGAs are used for rapid prototyping of digital circuits. The design and test of digital systems are very time-efficient and cost-effective with FPGAs. It also discusses about the logic components in the FPGA, mostly consists of memory elements such as registers or even complete blocks of memory that can be configured to hold any desired state. As we know, FPGAs were used mostly for prototyping and emulation systems in the design process of digital system design and ASICs. However, recently, FPGAs have become popular for a variety of mainstream products in networking, telecommunication, digital signal processing and in consumer electronics. FPGAs can be classified based on the technology using to program it.

FPGA architectures have been intensely investigated over the past two decades. A major aspect of FPGA architecture research is the development of Computer Aided Design (CAD) tools for design and implementation of fast and high density FPGAs and mapping applications to it. It is well established that the quality of an FPGA-based implementation is largely determined by the effectiveness of accompanying suite of CAD tools. Benefits of an otherwise well-designed, feature-rich FPGA architecture might be impaired if the CAD tools cannot take advantage of the features that the modern FPGA design provides. Thus, CAD algorithm research is essential to the necessary architectural advancement to narrow the performance gaps between FPGAs and other computational devices like ASICs.

Two-dimensional CAD flow of mesh-based and tree-based FPGA architectures are described and analyzed in Chap. 4. This chapter provides a perfect starting point for FPGA designs to evaluate and understand the algorithms and data-structures used in designing the software for FPGA placement and routing.

Chapter 5 provides the study of the existing variants of 2D tree-based FPGA architecture and the impact of 3D migration on its topology. We have seen numerous studies showing the characteristics of tree-based interconnect networks, how they scale in terms of area and performance and empirically how they relate to particular designs. Nevertheless, we have not had any breakthrough in optimizing these network topologies to exploit the advantages in area and power consumption and neither know how to deal with the larger wire-length issues that impede performance of tree-based FPGA architecture. Through the course of this book, we try to make the readers understand that, it is nearly impossible to optimize the area and speed, unless we break the very backbone of the tree-based interconnect network and resurrect again by using 3D technology. The 3D-ICs can alleviate interconnect delay issues by offering flexibility in system design, placement and routing. A new set of 3D FPGA architecture exploration tools and technologies developed to validate the advance in performance and area. Modern FPGAs have become a viable alternative to cell-based design technology by providing reconfigurable computing platforms with improved performance and higher density. While the reconfigurability provides flexibility, two-dimensional FPGAs also lead to area and performance overhead in comparison to cell-based custom integrated circuits (ICs). Thus, to combine the advantages of both FPGAs and custom ICs, modern FPGAs have emerged as an attractive solution for system-on-chip implementations. Modern FPGAs include design components such as digital signal processors, on chip memory blocks, multipliers, adders and entire processors. In Chap. 6 our primary focus is on validation of architecture exploration and optimization methodologies of 3D homogeneous and heterogeneous tree-based and mesh-based FPGAs.

A 3D-IC system consists of disparate materials with considerably different thermal properties including semiconductor, metal, dielectric and possibly polymer layers used for inter-plane bonding. Although the power consumption of these circuits is expected to decrease due to the considerably shorter interconnects, the power density increases since there is a greater number of devices per unit volume compared to a 2D circuit. As the power density increases, the temperature of the planes non-adjacent to the heat sink of the package can rise, resulting in degraded performance or thermal gradients that can accelerate wear out mechanisms. Design methodologies at various stages of the IC design flow, such as synthesis, floor-planning, placement and routing, which maintain the temperature of a circuit within specified limits or alleviate thermal gradients among the planes of the 3D circuit, are therefore necessary. Two key elements are required to establish a successful 3D thermal management strategy: a 3D thermal model, to characterize the thermal behaviour of a circuit and design techniques that alleviate thermal gradients among the physical planes of a 3D-IC system, while maintaining the operating temperature within acceptable levels. The primary requirements of a thermal model are high

accuracy, low complexity and reasonably fast, while thermal design techniques should produce high-quality circuits without incurring long computational design time. To reduce the complexity of the modelling process, standard methods to analyse heat transfer, such as finite difference, finite element and boundary element methods, have been adopted to evaluate the temperature of a 3D circuit. Simpler analytic expressions have also been developed to characterize the temperature within a 3D system. The discussion culminates in Chap. 7 where design and implementation three-dimensional thermal model and thermal design techniques to improve the thermal profile and 3D-IC system and Chap. 7 focus its attention more on thermal analysis of 3D FPGAs.

Design techniques for three-dimensional (3D) ICs considerably lag the significant strides achieved in 3D manufacturing technologies. Advanced design methodologies for two-dimensional (2D) circuits are not sufficient to manage the added complexity caused by the third dimension. Consequently, design methodologies that efficiently handle the added complexity and inherent heterogeneity of 3D circuits are necessary. These 3D design methodologies should support robust and reliable 3D circuits while considering different forms of vertical integration, such as system-in-package and 3D-ICs with fine grain vertical interconnections. Global signalling issues, such as clock and power distribution networks, are further exacerbated in vertical integration due to the limited number of package pins, the distance of these pins from other planes within the 3D system and the impedance characteristics of the through silicon vias (TSVs). In addition to these dedicated networks, global signalling techniques that incorporate the diverse traits of complex 3D systems are required. One possible approach, potentially significantly reducing the complexity of interconnect issues in 3D circuits, is by optimizing the number of vertical interconnects (TSVs). Design methodologies that exploit the diversity of 3D structures to further enhance the performance of multi-plane integrated systems are necessary. Chapter 8 introduce new 3D physical design methodology and verification tools developed. This chapter also discuss the development of 3D physical design methodology and tools using existing 2D CAD tools for the implementation of 3D tree-based FPGA demonstrator. During the course of design process, we addressed many specific issues that 3D designers will encounter dealing with tools that are not specifically designed to meet their needs. In contrast, the thermal performance is expected to worsen with the use of 3D integration. In this Chapter, we examined precisely how thermal behaviour scales in 3D integration and determine how the temperature can be controlled using thermal design techniques.

A concerted effort has been made to present three-dimensional integration and high performance tree-based FPGA design using newly developed 3D physical design tools and VLSI design methodologies. Three-dimensional integration is an interdisciplinary field that relies on many experts working together at every design level. Emphasis is placed on illustrating the interaction among the different field. For example, 3D thermalware physical design described in Chap. 7 is a classic case

of thermal, mechanical and electrical engineers working together to develop high performance three-dimensional integrated circuits. Few emerging research areas and possible future lines of research and applications of 3D-IC described in Chap. 9.

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