

Low Power Programmable Gain Analog to Digital Converter for Integrated Neural Implant Front End

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Abstract. Integrated neural implants interface with the brain using biocompatible electrodes to provide high yield cell recordings, large channel counts and access to spike data and/or field potentials with high signal-to-noise ratio. By increasing the number of recording electrodes, spatially broad analysis can be performed that can provide insights on how and why neuronal ensembles synchronize their activity. However, the maximum number of channels is constrained by noise, area, bandwidth, power, thermal dissipation and the scalability and expandability of the recording system. In this chapter, we characterize the noise fluctuations on a circuit-architecture level for efficient hardware implementation of programmable gain analog to digital converter for neural signal-processing. This approach provides key insight required to address signal-to-noise ratio, response time, and linearity of the physical electronic interface. The proposed methodology is evaluated on a prototype converter designed in standard single poly, six metal 90-nm CMOS process.

1 Introduction

Bio-electronic interfaces allow the interaction with neural cells by both recording, to facilitate early diagnosis and predict intended behavior before undertaking any preventive or corrective actions [1], and stimulation devices, to prevent the onset of detrimental neural activity, such as the one resulting in tremor. Monitoring large scale neuronal activity and diagnosing neural disorders has been accelerated by the fabrication of miniaturized micro-electrode arrays, capable of simultaneously recording neural signals from hundreds of channels [2]. By increasing the number of recording electrodes, spatially broad analysis of local field potentials can be performed to provide insights into how and why neuronal ensembles synchronize their activity. Studies on body motor systems have uncovered how kinematic parameters of movement control are encoded in neuronal spike time-stamps [3] and inter-spike intervals [4]. Neurons produce spikes of nearly identical amplitude near to the soma, but the measured signal depends on the position of the electrode relative to the cell. Additionally, the signal quality in neural interface front-end, beside the specifics of the electrode material and the electrode/tissue interface, is limited by the nature of the bio-potential signal and its biological background noise, dictating system resources.

For any portable or implantable device, micro-electrode arrays require miniature electronics locally to amplify the weak neural signals, filter out noise and out-of band

interference and digitize for transmission. A single-channel [5] or a multi-channel integrated neural amplifiers and converters provide the front-line interface between recording electrode and signal conditioning circuits and, thus, face critical performance requirements. Multi-channel, fully differential designs allow for spatial neural recording and stimulation at multiple sites [6–8]. The maximum number of channels is constrained by noise, area, bandwidth, power [9], which has to be supplied to the implant from outside, thermal dissipation e.g. to avoid necrosis of the tissues even with a moderate heat flux [10], and the scalability and expandability of the recording system.

The block diagram of a typical neural recording system architecture is illustrated in Fig. 1(a). When a neuron fires an action potential, the cell membrane becomes depolarized by the opening of voltage-controlled neuron channels leading to a flow of current both inside and outside the neuron. Since extracellular media is resistive [11], the extracellular potential is approximately proportional to the current across the neuron membrane [12]. The membrane roughly behaves like an RC circuit and most current flows through the membrane capacitance [13]. The data acquired by the recording electrodes is conditioned using analog circuits. As a result of the small amplitude of neural signals and the high impedance of the electrode tissue interface, amplification and band-pass filtering of the neural signals is performed before the signals can be digitized by a successive approximation register (SAR)-based analog to digital converter (ADC) [14]. To avoid the large capacitive DACs found in the SAR ADC, and to lower demands on driving capabilities of the amplifier and relax power, noise and cross-talk requirements, in the alternative architecture illustrated in Fig. 1(b), the programmable gain amplifier (PGA) and ADC are combined and embedded in every recording channel.

The programmable gain analog to digital converter (PG ADC) implements simultaneously both signal acquisition and amplification, and data conversion. As illustrated in Fig. 2 [15], the schematic incorporates a fully-differential operational transconductance

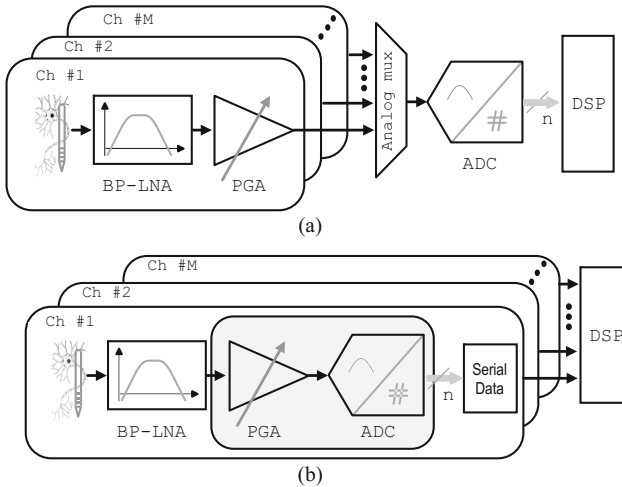


Fig. 1. Multichannel neural interfaces: (a) An ADC is multiplexed between M channels, (b) An ADC per channel with serial interfacing.

amplifier (OTA), a comparator and circuitry for control of the acquisition and amplification operation set by the clock phases ϕ_{s1} , ϕ_{s2} and ϕ_{s3} and output generation data conversion operation, controlled by the clock phases ϕ_1 and ϕ_2 . The recorded signals are capacitively coupled to the input of the amplifier to reject the dc polarization. The differential input signal is sampled, amplified by the capacitance ratio (gain G^A is adjustable by implementing C_3 as a programmable capacitor array, $G^A = C_3/C_4$), and transferred to the integration capacitors C_4 at the feedback loop of the OTA. At data conversion operation, the differential signal stored in C_4 is converted to digital domain by successively adding or subtracting binary-scaled versions of the reference voltage to the integration capacitors. Voltage addition or subtraction is implemented by means of the four cross-coupled switches controlled by the signals ϕ_{2p} and ϕ_{2n} . Digital representation of the output signals are then sequentially stored in the SAR register for further processing.

A low-power monolithic digital signal processing (DSP) unit provides additional filtering and executes spike discrimination and sorting algorithms [16]. The relevant information is then transmitted to an outside receiver through the transmitter or used for stimulation in a closed-loop framework. Understanding the role of noise in such systems is one of the central challenges in the heterogeneous neural simulation and neural rehabilitation [17]. In this chapter, we try to characterize the noise fluctuations on a circuit-architecture level for efficient hardware implementation of neural signal-processing circuitry. This approach provides the key insight required to address signal-to-noise ratio (SNR), response time, and linearity of the physical electronic interface (i.e., saturation level).

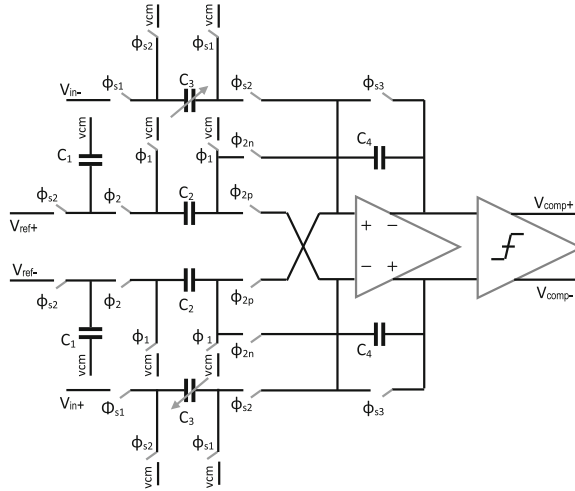


Fig. 2. Schematic of a programmable gain ADC.

2 Noise Characterization

2.1 Noise Models

Neural Cell Noise Model. In the Hodgkin and Huxley framework, the configuration of the neural channel is determined by the states of its constituent subunits, where each subunit can be either in an open or closed state [18]. Adding a noise term $\chi_x(V, t)$ ($x = m, h$, or n) to the deterministic ordinary differential equation (ODE) of Hodgkin and Huxley is consistent with the behavior of the Markov process for channel gating [19]. Such process can be contracted to a Langevin description (via a Fokker–Planck equation) and expressed as delta-correlated noise processes $\Gamma_{neuron}(t + \tau, t) = 1/\kappa[\alpha_x(1-x) + \beta_x x]\delta(\tau)$, where κ is the total number of neural channels, and the transition rates $\alpha_x(t)$ and $\beta_x(t)$ are instantaneous functions of the membrane potential $V(t)$. Dirac’s delta function δ designates that the noise at different times is uncorrelated and the variables m , h , and n represent the aggregated fraction of open subunits of different types, aggregated across the entire cell membrane.

Electrode-Tissue Interface Noise Model. The overall noise of an electrode-tissue interface has contributions from the tissue/bulk thermal noise, the electrode-electrolyte interface noise, and the electronic noise. The most important types of electrical noise sources (thermal, shot, and flicker noise) in passive elements and integrated circuit devices have been investigated extensively, and appropriate models derived [20] as stationary and in [21] as nonstationary noise sources. We adapt model descriptions as defined in [21], where thermal and shot noise are expressed as $\Gamma_{thermal}(t + \tau, t) = 2kTG(t)\delta(\tau)$ and $\Gamma_{shot}(t + \tau, t) = qI_D(t)\delta(\tau)$, respectively, where k is Boltzmann’s constant, T is the absolute temperature, G is the conductance, q is the electron charge, and I_D is the current through the junction. These noise processes correspond to the current noise sources, which are included in the models of the integrated circuit devices. Tissue noise is modelled as the thermal noise generated by the solution/spreading or tissue/encapsulation resistance [13] and the electrode noise is the thermal noise generated by the charge transfer resistor [22]. The noise of the recording electronic circuits is mainly determined by the thermal and flicker noise generated by the input amplifier. Although the preamplifier can provide first-order low-pass filtering, dedicated low-pass filters are used to further minimize high-frequency noise. The cut-off frequency of the low-pass filters is set to $f_{Neuron} = 10$ kHz, where f_{Neuron} is the signal bandwidth of the action potential.

A/D Converter Noise Model. Sampled data systems operate on the series of discrete-time samples taken at the end of the sampling period. Although the details of the processing during each period result in nonstationary noise voltages and currents, the same operation is performed each clock cycle, leading to the same signal statistics at each cycle. Consequently, such stochastic process can be described as wide-sense cyclostationary.

The special case of a white noise input source is of particular importance since the majority of the noise sources can be traced back to white noise generated in circuit components. For a white noise step input, the autocorrelation is a delta function, where S_{xo} is the one-sided white noise power spectral density (PSD) of the underlying noise process. By using Parseval's theorem, the variance of the output as a function of the autocorrelation simplifies to $\Gamma(t + \tau, t) = 1/2 S_{xo}(t) \delta(\tau)$ [23]. The one-sided noise PSD of the sampled output can then be found from the sum of the filtered and shifted two-sided input noise PSD $S_x(f)$ [24]. Measurements of the output codes for a dc input signal to the A/D converter can be used to obtain an input-referred noise PSD estimate, $S_{ADC}(f)$. The noise of the input sampler and the converter quantization noise add to the input-referred noise PSD to give the total input noise PSD $S_{total}(f) = S_{sample}(f) + S_{ADC}(f) + S_q(f)$, where $S_{sample}(f) = (kT/C_s)/(f_s/2)$ is the noise PSD from the input sampler over the Nyquist range ($0 \leq f_{Neuron} \leq f_s/2$) and $S_q(f) = (V_{LSB}^2/12)/(f_s/2)$ is the A/D converter quantization noise.

2.2 Noise Analysis of Programmable Gain Analog to Digital Converter

A fundamental technique to reduce the noise level, or to increase the signal-to-noise ratio of a programmable gain ADC, is to increase the size of the sampling capacitors, or by either over-sampling or with calibration. However, for a fixed input bandwidth specification, the penalty associated with these techniques is the increased power consumption. Consequently, a fundamental trade-off exists between noise, speed, and power dissipation. For discrete-time analog signal-processing circuits, analog signals are acquired and processed consecutively, and a sample of the signal is taken periodically, according to a clock signal. As the sampling circuit cannot differentiate the noise from the signal, part of this signal acquisition corresponds to the instantaneous value of the noise at the moment the sampling takes place. In this context, when the sample is stored as charge on a capacitor, the root-mean-square total integrated thermal noise voltage is kT/C_4 , where kT is the thermal energy. This noise usually comprises two major contributions - the channel noise of the switches, which is a function of the channel resistance and the OTA noise.

The OTA output noise is, in most cases, dominated by the channel noise of the input transistors, where the thermal noise and the $1/f$ noise both contribute. If the input transistors of the OTA are biased in saturation region to derive large transconductance g_m , impact ionization and hot carrier effect will enhance their thermal noise level [25]. Similarly, the $1/f$ noise increases as well, due to the reduced gate capacitance resulted from finer lithography and, therefore, shorter minimum gate length. As a consequence, an accurate consideration of the intrinsic noise sources in such a circuit should have the thermal noise of switches and all amplifier noises readily included. Nevertheless, the input-referred noise v_n (the total integrated output noise as well) still takes the form of kT/C , with some correction factor χ_1 ,

$$\overline{v_n^2} = \chi_1 kT/C_4 \quad (1)$$

kT/C Noise. During the acquisition process, the kT/C noise is sampled on the capacitors C_4 along with the input signal. To determine the total noise charge sampled onto the capacitor network, the noise charge Q_{ns} is integrated over all frequencies

$$\overline{Q_{ns}^2} = \int_0^\infty \left| \frac{V_{ns}(C_4 + C_p + C_{OTA})}{1 + j\omega R_{on}(C_4 + C_p + C_{OTA})} \right|^2 d\omega = kT(C_4 + C_p + C_{OTA}) \quad (2)$$

where R_{on} is the resistance of the switch, V_{ns} is the noise source, C_p is the parasitic capacitance and C_{OTA} is the input capacitance of the OTA. Then, in the conversion mode, the sampling capacitor C_4 , which now contains the signal value and the offset of the OTA, is connected across the OTA. The total noise charge will cause an output voltage of

$$\overline{v_{ns(out)}^2} = \frac{\overline{Q_{ns}^2}}{C_4^2} = kT \frac{(C_4 + C_p + C_{OTA})}{C_4^2} = \frac{1}{\beta} \frac{kT}{C_4} \quad (3)$$

where β is the feedback factor. For differential implementation of the circuit, the noise power of the previous equation increases by a factor of 2, assuming no correlation between positive side and negative side, since the uncorrelated noise adds in power. Thus, input referred noise power, which is found by dividing the output noise power by the square of the gain ($G^A = C_3/C_4$), is given by

$$\overline{v_{ns(in)}^2} = \frac{\overline{v_{ns(out)}^2}}{(G^A)^2} = \frac{1}{\beta(G^A)^2} \frac{kT}{C_4} \quad (4)$$

OTA Noise in Conversion Mode. The resistive channel of the MOS devices in OTA has also thermal noise and contributes to the input referred noise of the PG ADC circuit. The noise power at the output is found from

$$\overline{v_{ns(out)}^2} = \int_0^\infty \left(\left| H(s|_{j\omega}) \right|^2 \times \overline{i_{ns}^2} \right) d\omega = \frac{kT\gamma}{C_{LT}} \frac{G_m R_o}{(1 + G_m R_o \beta)} = \frac{\gamma}{\beta} \frac{kT}{C_{LT}} \quad (5)$$

where R_o is the output resistance and C_{LT} is the capacitance loading at the output

$$C_{LT} = C_L + \beta \times (C_p + C_{OTA}) \quad (6)$$

The thermal noise coefficient γ depends on the effective mobility and channel length modulation [26]; it is 2/3 for older technology nodes and between 0.6 and 1.3 for submicron technologies [27]. Assuming $G_m R_o \beta \gg 1$, and gain of the conversion operation $G^C = C_2/C_4$, the input referred noise variance is

$$\overline{v_{ns(in)}^2} = \frac{\gamma}{\beta(G^C)^2} \frac{kT}{C_{LT}} \quad (7)$$

Total Input Referred Noise. The noise from acquisition and conversion mode can be added together to find the total input referred noise assuming that the two noise sources are uncorrelated. Using the results from (4) and (7), the total input referred noise power for differential input is given by

$$\overline{v_{ns(in)}^2} = \frac{2\gamma}{\beta(G^C)^2 C_{LT}} \frac{kT}{C_{LT}} + \frac{2}{\beta(G^A)^2} \frac{kT}{C_4} = 2\gamma \frac{1}{\beta} \left(\frac{1}{(G^C)^2 C_{LT}} + \frac{1}{\gamma(G^A)^2 C_4} \right) \cdot kT \quad (8)$$

The optimum gate capacitance of the OTA is proportional to the sampling capacitor $C_{OTA,opt} = \chi_2 C_4$, where χ_2 is a circuit-dependent proportionality factor. The drain current I_D yields

$$I_D = \frac{\chi_1^2 L^2 \omega_1^2 C_4}{\mu \chi_2} \quad (9)$$

where μ is the carrier mobility, ω_1 is the gain-bandwidth product, and L is the channel length. For a noise dominated by kT/C , the total power consumption P_T is found as

$$P_T \propto I_D V_{DD} = \frac{\chi_1^2 L^2 \omega_1^2 SNR \cdot 8kT}{\mu \chi_2} \frac{V_{DD}}{V_{max}^2} \quad (10)$$

For a given speed requirement and signal swing, a two times reduction in noise voltage requires a four times increase in the sampling capacitance value and the OTA size. This means that the PG ADC circuit power *quadruples* for every additional bit resolved for a given speed requirement and supply voltage as illustrated in Figs. 3 and 4. Notice that for a small sampling capacitor values, the thermal noise limits the SNR, while for a large sampling capacitor, the SNR is limited by the quantization noise and the curve flattens out. Improving the power efficiency beyond topological changes of the OTA and supply voltage reduction require smart allocation of the biasing currents.

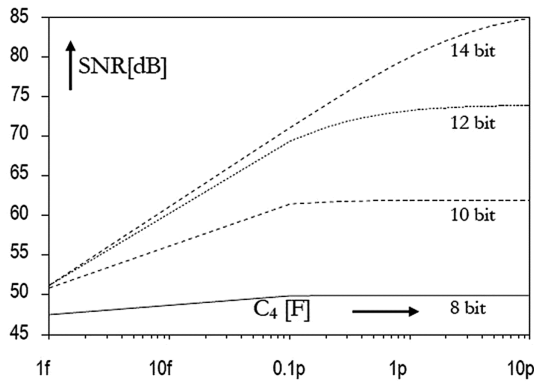


Fig. 3. Maximum achievable SNR for different sampling capacitor values and resolutions.

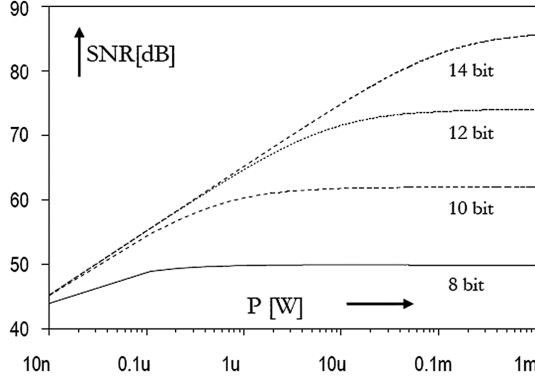


Fig. 4. SNR vs. Power dissipation.

Hence, techniques such as current reuse [28, 29], time multiplexing [4, 29] and adaptive duty-cycling of the entire analog front end [30, 31] can be used to improve power efficiency by exploiting the fact that neurons spikes are irregular and have low frequency. Choosing the OTA bandwidth too high increases the noise and, additionally, demands unnecessarily low on-resistance of the switches and, thus, large transistor dimensions. The optimum time constant remains constant regardless of the circuit size (or I_D) because C_L scales together with C_4 and the parasitic capacitance C_p . The choice of the hold capacitor value is a trade-off between noise requirements on one hand and speed and power consumption on the other. The sampling action adds kT/C noise to the system, which can only be reduced by increasing the hold capacitance C_4 .

A large capacitance, on the other hand, increases the load of the operational amplifier and, thus, decreases the speed for a given power. The OTA size and its bias current for a given speed requirement and minimum power dissipation are determined using τ -vs.- C_4 curves, as in Fig. 5. Note that for low frequency operation (where τ/τ_t is large), the C_{OTA} that achieves the minimum power dissipation for given settling time and noise requirements, usually, does not correspond to the minimum time constant point. This is a consequence of setting the C_4/C_{OTA} ratio of the circuit to the minimum time constant point, which requires larger C_{OTA} and results in power increase and excessive bandwidth. Near the speed limit of the given technology (where the ratio τ/τ_t is small), however, the difference in power between the minimum power point and the minimum time constant point becomes smaller, as the stringent settling time requirement forces the C_4/C_{OTA} ratio (Fig. 6) to be at its optimum value to achieve the maximum bandwidth.

2.3 The OTA Noise

The OTA in PG ADC circuit has some unique requirements; the most important is the input impedance, which must be purely capacitive so as to guarantee the conservation of charge. Consequently, the OTA input has to be either in the common source or the source follower configuration. Another characteristic feature is the load at the OTA output, which is typically purely capacitive and, as a result, the OTA output impedance

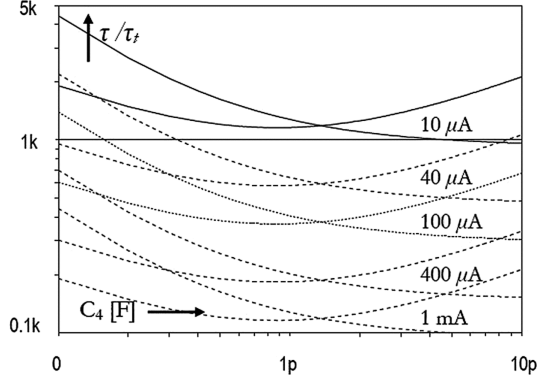


Fig. 5. Closed loop normalized time constant vs. Hold capacitance C_H for different biasing conditions; case for $C_4 = 3C_L$, $C_L = C_p$. The time constant is normalized to the $\tau_t (= 1/f_{t,intrinsic})$ of the device, which is approximately (C_G/g_m) .

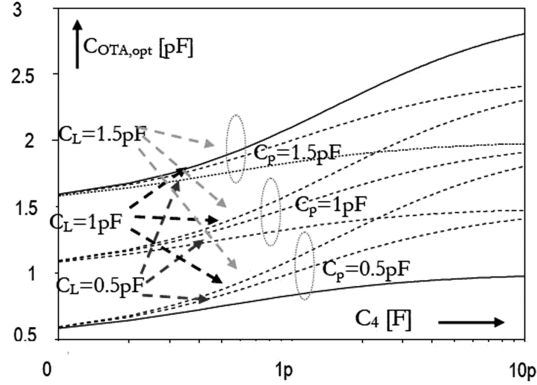


Fig. 6. Optimum gate capacitance $C_{OTA,opt}$ vs. Hold capacitance C_4 for different loading and parasitic conditions.

must be high. The benefit of driving solely capacitive loads is that no output voltage buffers are required. The implemented folded-cascode OTA and dynamic latch are illustrated in Fig. 7. The input stage of the OTA is provided with two extra transistors T_{10} and T_{11} in a common-source connection, having their gates connected to a desired reference common-mode voltage at the input, and their drains connected to the ground [32]. The advantage of this solution is that the common-mode range at the output is not restricted by a regulation circuit, and can approach a rail-to-rail behavior very closely.

The transistors of the output stage have two constraints: (i) the g_m of the cascading transistors $T_{5,6}$ must be high enough, in order to boost the output resistance of the cascode, allowing a high enough dc gain and (ii) the saturation voltage of the active loads $T_{3,4}$ and $T_{7,8}$ must be maximized, in order to reduce the extra noise contribution of the output stage. These considerations underline a tradeoff between fitting the saturation

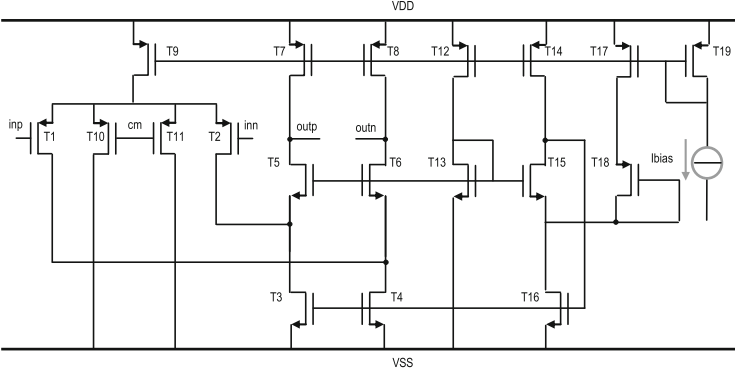


Fig. 7. OTA schematic.

voltage into the voltage headroom and minimizing the noise contribution. A good compromise is to make the cascading transistors larger than the active loads: in such a way, the g_m of the cascading transistors is maximized, boosting the dc gain, while their saturation voltage is reduced, allowing for a larger saturation voltage for the active loads, without exceeding the voltage headroom. The output SNR is equal to

$$SNR_{out} = \frac{C_L}{2\gamma kT} \frac{A^2 \times g_{m1,2} R_{out}}{g_{m1,2} + g_{m3,4} + g_{m7,8}} \quad (11)$$

where A is the amplitude of the input signal and R_{out} denotes the open-loop output resistance of the OTA. From (11), it can be concluded that in order to maximize the output SNR, C_L must be maximized, which means that the bandwidth must be minimized. The noise contribution of the individual transistors are shown in Fig. 8.

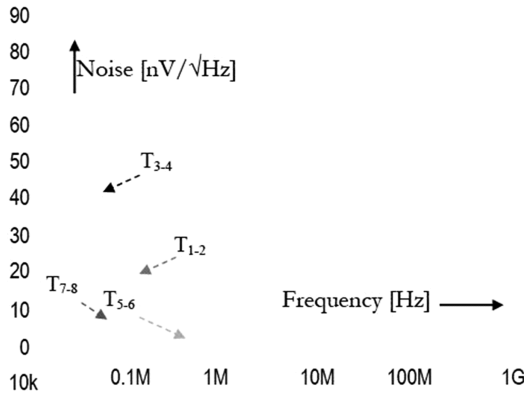


Fig. 8. Noise contribution of the individual transistors in the OTA.

The input-referred noise of the OTA input pair is reduced by increasing the g_m , increasing the current, or increasing the aspect ratio of the devices. The effect of the last method, however, is partially canceled by the increase in the noise excess factor. When referred to the OTA input, the noise voltages of the transistors used as current sources (or mirrors) in the first stages are multiplied by the g_m of the device itself and divided by the g_m of the input transistor, which again suggests that maximizing input pair g_m minimizes noise. It can be further reduced by decreasing the g_m of the current sources. Since the current is usually set by other requirements, the only possibility is to decrease the aspect ratio of the device. This leads to an increase in the gate overdrive voltage, which, as a positive side effect, also decreases γ . Increasing L to avoid short channel effects is also possible, although with a constant aspect ratio it increases the parasitic capacitances.

2.4 The Comparator Noise

The dynamic latch illustrated in Fig. 9 consists of the pre-charge transistors T_{14} and T_{17} , the cross-coupled inverter T_{12-13} and T_{15-16} , the differential pair T_{10} and T_{11} and the switch T_9 , which prevent the static current flow at the resetting period [33]. When the latch signal is low (resetting period), the drain voltages of T_{10-11} are $V_{DD}-V_T$ and their source voltage is V_T below the latch input common mode voltage. Therefore, once the latch signal goes high, the n -channel transistors T_{11-13} immediately go into the active region. As each transistor in one of the cross-coupled inverters turns off, there is no static power dissipation from the latch, once the latch outputs are fully developed. A large portion of the total comparator current is allocated to the input branches to boost the input gm . Similarly, the noise from the non-gain element, i.e. the load transistor, is minimized, by applying a small biasing current. Additionally, small width and a large length for their gate dimensions are chosen.

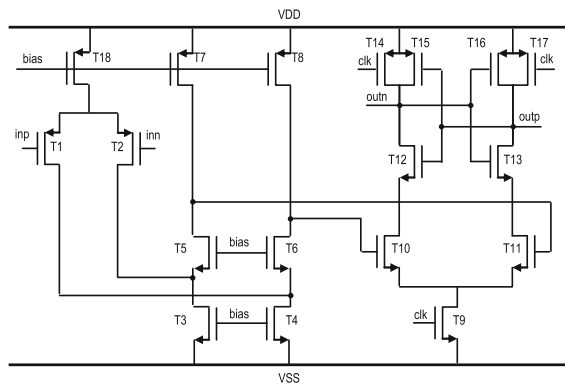


Fig. 9. Comparator schematic.

3 Experimental Results

The time series representation of neuron signal (Fig. 10) are composed of a spike burst, plus additive Gaussian white noise (grey area with 1000 randomly selected neural channel compartments, Fig. 11). In typical electrode-tissue interface, we are relying on the current measurement to sense these neural signals. Hence, by maintaining a constant current density, the relative uncertainty of the current becomes inversely proportional to the square of the interface area. The electrode noise spectral density has an approximate dependence of -10 dB/dec for small frequencies. However, for frequencies higher than $1\text{--}10$ kHz, capacitances at the interface form the high-frequency pole and shape both the signal and the noise spectrum; the noise is low-pass filtered to the recording amplifier inputs. After band-pass filtering and amplification, the noisy neural signal is further processed with programmable gain analog to digital converter. The fluctuation of the voltage on the sampling capacitor is inversely proportional to the capacitance (the variance of the capacitor voltage is kT/C at any given time). This implies that with scaling, the uncertainty of the sampled voltage increases.

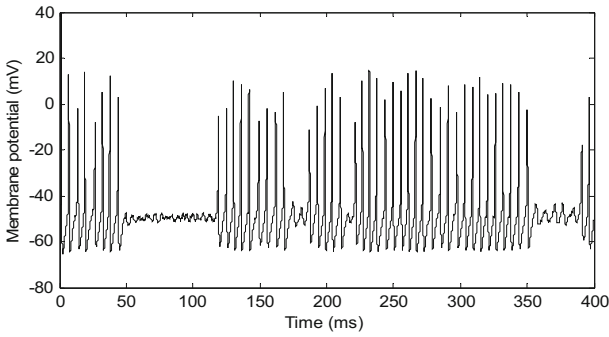


Fig. 10. Nominal (without noise) voltage trace of the neuron cell activity; the complex spike burst is followed by a pause in the spike activity.

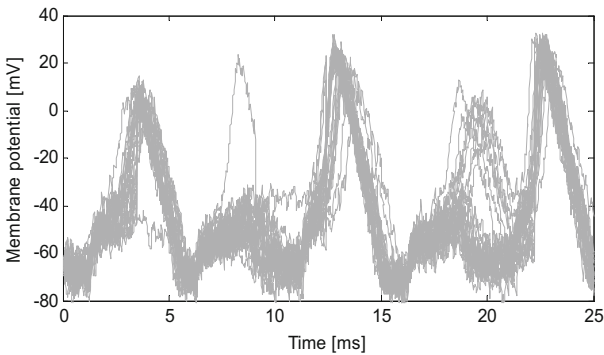


Fig. 11. Statistical voltage trace of the neuron cell activity; grey area - voltage traces from 1000 randomly selected neural channel compartments.

It can be seen that in both scenarios, in electrode-tissue interface and in PG ADC, the noise in the neural interface front end greatly increases, as the interface size reduces. The interface's input equivalent noise voltage decreases, as the gain across the amplifying stages increase, e.g. the ratio of the square of the signal power over its noise variance can be expressed as

$$SNR = A^2 / \left[\overline{v_{ns(neural)}^2} + \overline{v_{ns(electrode)}^2} + \sum_i \left(\prod_j G_j^{-1} \right) \overline{v_{ns(amp,i)}^2} \right] \quad (12)$$

where $v_{ns(amp,i)}^2$ represents the variance of the noise added by the i th amplification stage with gains G_j . The variance of the electrode is denoted as $v_{ns(electrode)}^2$ and $v_{ns(neural)}^2$ is the variance of the biological neural noise. The observed SNR of the system also increases as the system is isomorphically scaled up, which suggests a fundamental trade-off between the SNR and the speed of the system. This lower bound on the speed in a converter loop is primarily a function of the technology's gate delay and the kT/C noise multiplied by the number of SAR cycles necessary for one conversion. All PG ADC simulations were performed with a 1.2 V supply voltage at room temperature (25 °C). Spectral signature of PG ADC is illustrated in Fig. 12. The circuit offers a programmable amplification of 0–18 dB by digitally scaling the input capacitance C_3 .

As shown in Fig. 13, the Signal-to-Noise and Distortion Ratio (SNDR), Spurious-Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD) remain constant at different gain settings. The THD in the range of 10–100 kS/s is above 54 dB for a f_{in} of 5 kHz (Fig. 14). Within the bandwidth of neural activity of up to 5 kHz, SNDR is above 44 dB and SFDR more than 57 dB. The degradation with a higher input signal is mainly due to the parasitic capacitance, the clock non-idealities and the substrate switching noise. The parasitic capacitance decreases the feedback factor resulting in an increased settling time constant. The non-idealities of the clock such as the clock jitter, the non-overlapping period time, the finite rising and the fall time, and unsymmetrical duty cycle are other causes for this degradation. The three latter errors reduce the time allocated for the setting time.

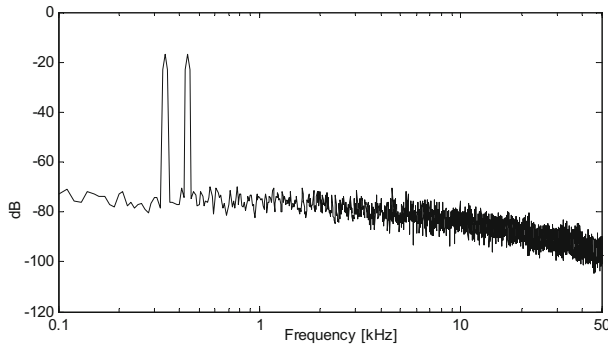


Fig. 12. Spectral signature of programmable gain A/D converter-two tone test.

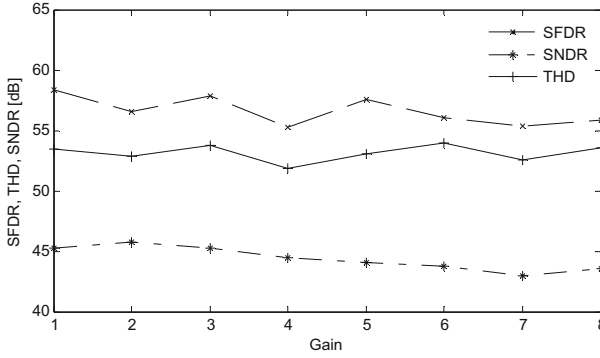


Fig. 13. SFDR, SNDR and THD vs. Gain settings.

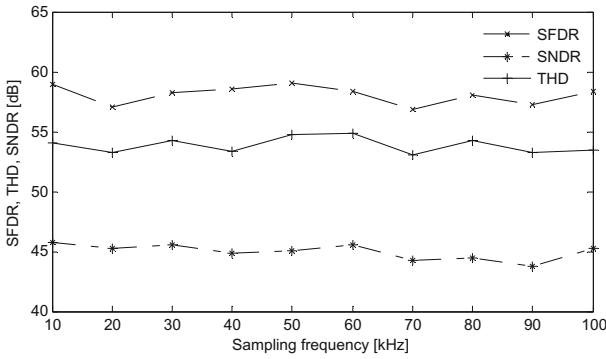


Fig. 14. SFDR, SNDR and THD vs. Sampling frequency, with $f_{in} = 5$ kHz and gain set to one.

4 Conclusions

The high density of neurons in neurobiological tissue requires a large number of electrodes for accurate representation of neural activity. To develop neural prostheses capable of interfacing with single neurons and neuronal networks, multi-channel neural probes and the electrodes need to be customized to the anatomy and morphology of the recording site. The increasing density and the miniaturization of the functional blocks in these multi-electrode arrays, however, presents significant circuit design challenge in terms of area, bandwidth, power, and the scalability, programmability and expandability of the recording system. In this chapter, for one such functional block, programmable analog to digital converter, we evaluate the trade-off between noise, speed, and power dissipation and characterize the noise fluctuations on a circuit-architecture level. This approach provides the key insight required to address SNR, response time, and linearity of the physical electronic interface.

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