2 Resistive Diode Frequency Multipliers

Although there is a persistent tendency to higher operating frequencies of direct signal generation concepts, frequency multipliers are still used to provide phase locked signal stimuli at millimeter-wave frequencies. Multipliers are required for the local oscillator and signal path of synthetic automatic test systems and traditional instruments (Fig. 1.1, 1.2, 1.3, 1.4). The considerations of this chapter are restricted to resistive nonlinearities (varistor Schottky diodes). Section 2.1 outlines the theoretical conversion loss limitations of resistive diode frequency multipliers. An entire modelling procedure for hybrid Schottky diodes is given in section 2.2. Semiconductor physics of the Schottky junction is presented first in subsection 2.2.1. This is followed by a comparison of several common diode architectures. Modelling procedures for the linear part of the diode, undepleted epilayer and buffer layer, are given in subsection 2.2.3. Drude's dispersion model is applied and effective material parameters are derived, which are required for analytical or 3D EM considerations. The subsection ends with a market overview of Schottky diodes. Section 2.3 explains single tone large signal analysis of nonlinear circuits and serves as a basis for large signal / small signal analysis (LSSS) of subsection 4.2.1. Different multiplier architectures, optimum embedding impedances and the author's frequency multiplier design flow are explained in section 2.4. The author's experimental results are given in section 2.5 to section 2.7. An octave bandwidth tripler for 20 to 40 GHz utilizing bilateral finlines on PCB is presented in section 2.5. Two frequency doublers for 50 to 110 GHz and three triplers for 60 / 67 to 110 GHz on thin-film processed alumina are illustrated in section 2.6. Sec-

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tion 2.7 includes a D-band frequency doubler and Y-band frequency tripler. In subsection 2.7.1 the design equations of Dolph-Chebyshev waveguide tapers are presented. An uncertainty analysis of spectral power measurements above 50 GHz is given in subsection 2.7.2.

2.1 Theoretical Limitations of Resistive Diode Frequency Multipliers

Fig. 2.1 shows a shunt mounted diode, excited with DC, RF and LO voltage components $V_{\mathrm{DC}}, v_{\mathrm{RF}}(t)$ and $v_{\mathrm{LO}}(t)$.

$$\begin{aligned} v_{\mathrm{LO}}(t) &= \hat{v}_{\mathrm{LO}} \cos\left(\omega_{\mathrm{LO}} t + \varphi_{\mathrm{LO}}\right) = V_{\mathrm{LO}} e^{j\omega_{\mathrm{LO}} t} + V_{\mathrm{LO}}^{\star} e^{-j\omega_{\mathrm{LO}} t} \\ v_{\mathrm{RF}}(t) &= \hat{v}_{\mathrm{RF}} \cos\left(\omega_{\mathrm{RF}} t + \varphi_{\mathrm{RF}}\right) = V_{\mathrm{RF}} e^{j\omega_{\mathrm{RF}} t} + V_{\mathrm{RF}}^{\star} e^{-j\omega_{\mathrm{RF}} t} \end{aligned} \tag{2.1}$$

The individual signal branches are isolated by ideal LC bandpass filters, showing short circuit behaviour at the corresponding signal frequencies $\omega = 0, \omega_{\mathrm{RF}}, \omega_{\mathrm{LO}}$ and open circuit behaviour at all other frequencies. Due to the nonlinear voltage-current dependency of the diode, the diode's voltage and current spectral contents include a DC component, RF harmonics $n\,\omega_{\mathrm{RF}}$, LO harmonics $m\,\omega_{\mathrm{LO}}$ and components at the mixing frequencies $n\,\omega_{\mathrm{RF}} + m\,\omega_{\mathrm{LO}}$ (Eq. (2.2)).

$$\omega_{nm} = 2\pi f_{nm} = n\,\omega_{\mathrm{RF}} + m\,\omega_{\mathrm{LO}} \qquad n, m \in \pm\mathbb{N}_0 \tag{2.2}$$

Each spectral component ω_{nm} is filtered out in additional branches with individual load impedances Z_{nm} (Fig. 2.1), called embedding impedances or idle impedances[1]. The circuit of Fig. 2.1 and its dual circuit with series mounted diode in Fig. 2.2 constitute the most versatile mixer equivalent circuits. Choosing appropriate values of the source and embedding impedances, modelling of every practical mixer and frequency multiplier circuit is possible. If all idle impedances in Fig. 2.1 are open circuits $Z_{nm} \to \infty$, in the notation of Saleh [1]

[1] As these appear in parallel to the diode, they are called current idlers. In case of series connection with the diode, they are called voltage idlers.

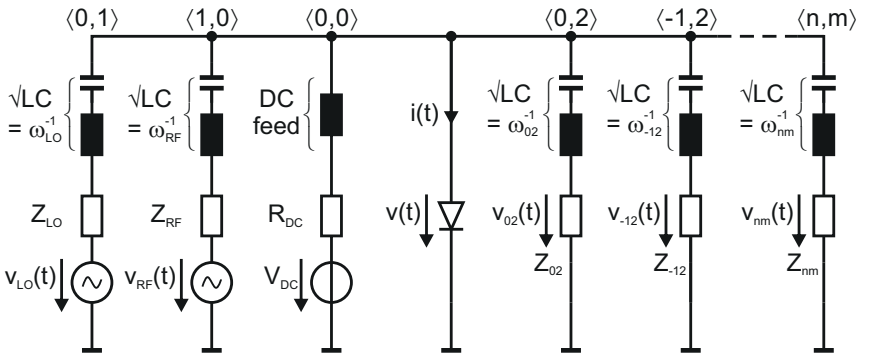

Figure 2.1: Equivalent circuit of frequency mixer consisting of shunt mounted diode, DC, RF, LO sources, load impedances and current idlers in shunt branches.

this is called a Z-mixer or impedance mixer because its small signal conversion matrix (compare subsection 4.2.1) is an impedance matrix. In this sense, the circuit of Fig. 2.2 is called a Y-mixer if all idle impedances are short circuits.

In 1958, Pantell [2] derived fundamental power relationships between source and load power of the circuit in Fig. 2.1, which are presented in the following. Within the work of Pantell, the diode is modelled as positive nonlinear resistor, which means a positive voltage derivative of current $\mathrm{d}i(t)/\mathrm{d}v(t) \geq 0$. All voltage idlers consist of resistive impedances only.

$$\begin{aligned} g : \mathbb{R} \to \mathbb{R}, v \mapsto i = g(v) \\ g \text{ infinitely differentiable,} \\ \text{and } \mathrm{d}i(t)/\mathrm{d}v(t) \geq 0 \\ Z_{\mathrm{RF}}, Z_{\mathrm{LO}}, Z_{nm} \in \mathbb{R} \end{aligned} \tag{2.3}$$

V_{nm} and I_{nm} cover the spectral content of voltage and current across the diode at each combination frequency ω_{nm}. These phasors are related to half of the peak amplitude values $\hat{v}_{nm}/2, \hat{i}_{nm}/2$ and

phases φ_{nm} of the corresponding time waveforms, likewise Eq. (2.1), and as usual for double sided complex Fourier[2] series.

$$\begin{aligned} v_{nm}(t) &= \hat{v}_{nm} \cos\left[(n\omega_{\mathrm{RF}} + m\omega_{\mathrm{LO}})t + \varphi_{nm}\right] \\ &= V_{nm} e^{jn\omega_{\mathrm{RF}}t + jm\omega_{\mathrm{LO}}t} + V_{-n-m} e^{-jn\omega_{\mathrm{RF}}t - jm\omega_{\mathrm{LO}}t} \end{aligned} \tag{2.4}$$

The resulting voltage and current time waveforms $v(t), i(t) \in \mathbb{R}$ across the diode are given by Eq. (2.5). These expressions are sums of phasors rather than double sided complex Fourier series' because the individual spectral components are not only harmonics. As a consequence of $v(t), i(t)$ being real, $V_{nm} = V^{\star}_{-n-m}, I_{nm} = I^{\star}_{-n-m}$ holds true.

$$\begin{aligned} v(t) &= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} V_{nm} \exp\left(jn\omega_{\mathrm{RF}}t + jm\omega_{\mathrm{LO}}t\right) = \\ &= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} V_{nm} \exp\left(j\omega_{nm}t\right) \\ i(t) &= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} I_{nm} \exp\left(jn\omega_{\mathrm{RF}}t + jm\omega_{\mathrm{LO}}t\right) = \\ &= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} I_{nm} \exp\left(j\omega_{nm}t\right) \\ V_{nm} &= V^{\star}_{-n-m}, \quad I_{nm} = I^{\star}_{-n-m} \end{aligned} \tag{2.5}$$

Eq. (2.6) includes the average real P_{nm} and reactive power R_{nm} at the nonlinear diode and mixing frequency $\langle \mathrm{RF}, \mathrm{LO} \rangle = \langle n, m \rangle$.

$$\begin{aligned} P_{nm} &= V_{nm} I^{\star}_{nm} + V^{\star}_{nm} I_{nm} = P_{-n-m} \\ R_{nm} &= jV^{\star}_{nm} I_{nm} - jV_{nm} I^{\star}_{nm} \end{aligned} \tag{2.6}$$

[2] Jean Baptiste Joseph Fourier (1768−1830), French mathematician.

In [2] Pantell shows the following general power relationships are valid.

$$\begin{aligned}\sum_{n=0}^{\infty}\sum_{m=-\infty}^{\infty} n^2 P_{nm} &= \frac{1}{4\pi^2}\int_0^{2\pi} \mathrm{d}(\omega_{\mathrm{LO}}t)\int_0^{2\pi}\frac{\mathrm{d}i}{\mathrm{d}v}\left(\frac{\mathrm{d}v}{\mathrm{d}(\omega_{\mathrm{RF}}t)}\right)^2 \mathrm{d}(\omega_{\mathrm{RF}}t)\\ \sum_{n=-\infty}^{\infty}\sum_{m=0}^{\infty} m^2 P_{nm} &= \frac{1}{4\pi^2}\int_0^{2\pi} \mathrm{d}(\omega_{\mathrm{RF}}t)\int_0^{2\pi}\frac{\mathrm{d}i}{\mathrm{d}v}\left(\frac{\mathrm{d}v}{\mathrm{d}(\omega_{\mathrm{LO}}t)}\right)^2 \mathrm{d}(\omega_{\mathrm{LO}}t)\end{aligned} \tag{2.7}$$

Because $\mathrm{d}i/\mathrm{d}v \geq 0$ both expressions in Eq. (2.7) are greater than or equal to zero.

$$\begin{aligned}\sum_{n=0}^{\infty}\sum_{m=-\infty}^{\infty} n^2 P_{nm} &\geq 0\\ \sum_{n=-\infty}^{\infty}\sum_{m=0}^{\infty} m^2 P_{nm} &\geq 0\end{aligned} \tag{2.8}$$

The amount of power across the diode at each fundamental and mixing frequency strongly depends on the input power level and **all** the embedding impedances, including RF, LO, DC source impedances, shown in Fig. 2.1. Analytical solutions to this problem do not exist, numerical transient and balance methods (section 4.2) have to be applied. Anyway the above relations allow for an estimation of the maximum conversion efficiency or minimum conversion loss of mixers and multipliers. In case of fundamental mixing, Eq. (2.8) becomes Eq. (2.9), with P_{01} as fundamental LO power and the fundamental RF power P_{10}.

$$\begin{aligned}P_{01} + n^2 P_{nm} &\geq 0\\ P_{10} + m^2 P_{nm} &\geq 0\\ R_{nm} &\geq 0\end{aligned} \tag{2.9}$$

The conversion gain is given by Eq. (2.10).

$$\frac{|P_{nm}|}{P_{01}+P_{10}} \geq \frac{1}{n^2+m^2} \tag{2.10}$$

Therefore the maximum conversion gain for fundamental mixers ($m = n = 1$) is -3 dB (**!**). The conventional definition of mixer conversion gain does not involve the local oscillator power. Hence, fundamental **and** harmonic mixers can achieve 0 dB conversion gain. Comments on the difference between commutative mixers and multipliers are given in section 4.1.

Similarly for resistive diode frequency multipliers generating the m-th harmonic, the maximum conversion gain is given by Eq. (2.11).

$$\frac{|P_{0m}|}{P_{01}} \geq \frac{1}{m^2} \tag{2.11}$$

Which is -6 dB, -9.5 dB and -12 dB for doublers, triplers and quadruplers. These results were given earlier by Page [3] in 1956.

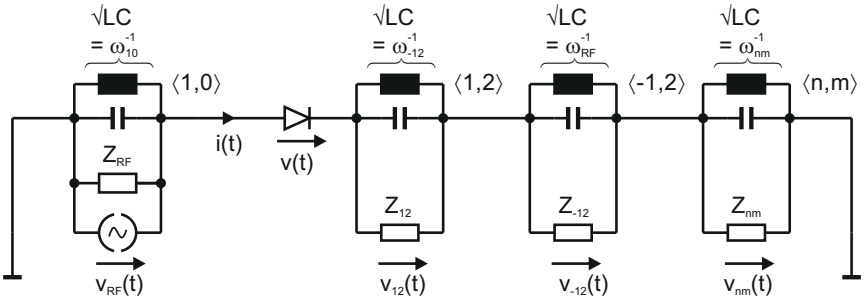

Figure 2.2: Equivalent circuit of frequency mixer consisting of series mounted diode, DC, RF, LO sources, load impedances and voltage idlers in series connection.

2.2 Schottky Barrier Diode Modelling

2.2.1 Junction Modelling

Fig. 2.3 shows energy band diagrams of metal (left side), n-type semiconductor (middle) and metal to n-type semiconductor junction (right side) with applied voltage v_j. The free space energy level of an electron is denoted by W_0. The necessary amount of energy to emit an electron from the lower edge of the metal conduction band W_Cm, which equals the Fermi[3] energy level W_Fm, is called the metal work function $q_\mathrm{e}\Phi_\mathrm{m}$. The n-type semiconductor's band gap, shown in Fig. 2.3, is given by $W_\mathrm{Cs} - W_\mathrm{Vs}$. Within the semiconductor, the Fermi energy level W_Fs differs from the conduction band level W_Cs by the amount of $q_\mathrm{e}V_\mathrm{n} = W_\mathrm{Cs} - W_\mathrm{Fs}$.

$$\begin{aligned} q_\mathrm{e}V_\mathrm{n} &= W_\mathrm{Cs} - W_\mathrm{Fs} \\ W_\mathrm{Fs} &= W_\mathrm{Cs} - q_\mathrm{e}V_\mathrm{n} \end{aligned} \tag{2.12}$$

Hence, the required energy to emit electrons to free space, the electron affinity $W_\chi = q_\mathrm{e}\Phi_\chi$, is lower than the metal work function $W_\chi < q_\mathrm{e}\Phi_\mathrm{m}$. Establishing infinitesimal distance (interatomic distance) between two such materials (m-n) builds the so called Schottky[4] junction (right side of Fig. 2.3). After connecting metal and semiconductor, the lower edge of the conduction band $W_\mathrm{C}(x)$ and the upper edge of the valence band $W_\mathrm{V}(x)$ become functions of location x. The Fermi energy level of the semiconductor equalizes to W_Fm, by emission of electrons to the metal ($v_\mathrm{j} = 0$). This leads to negative surface charge in the metal and positive space charge in the semiconductor. The latter is due to positively charged ionized donor atoms in the n-type material. Consequently, the arising barrier for electrons emitting

[3] Enrico Fermi (1901−1954), Italian physicist.
[4] Walter Hermann Schottky (1886−1976), German physicist.

from n-type semiconductor to metal equals the Fermi energy level difference $q_e\Phi_{bi} = q_e(\Phi_m - \Phi_s) = q_e(\Phi_m - \Phi_\chi - V_n)$.

$$q_e\Phi_{bi} = q_e(\Phi_m - \Phi_s) = q_e(\Phi_m - \Phi_\chi - V_n) \tag{2.13}$$

Φ_{bi} is called built-in potential of the Schottky junction and also known as diffusion voltage or flatband voltage. The uncorrected barrier height Φ_{b0} for electrons emitting from metal to semiconductor is greater than Φ_{bi} and given by $\Phi_{b0} = \Phi_m - \Phi_\chi$.

With an applied voltage v_j, the semiconductor's Fermi energy level shifts by the amount of $q_e v_j$ and so does the barrier. Positive voltages, from metal (anode) to semiconductor (cathode), lower the barrier and vice versa.

The so called Schottky effect lowers Φ_{b0} to the effective barrier height $\Phi_b = \Phi_{b0} - \Delta\Phi_b$. If an electric field is applied, an electron in the semiconductor at position $x = 0 + dx$ displaces electrons in the metal. This leads to an induced positive charge (image charge) at the

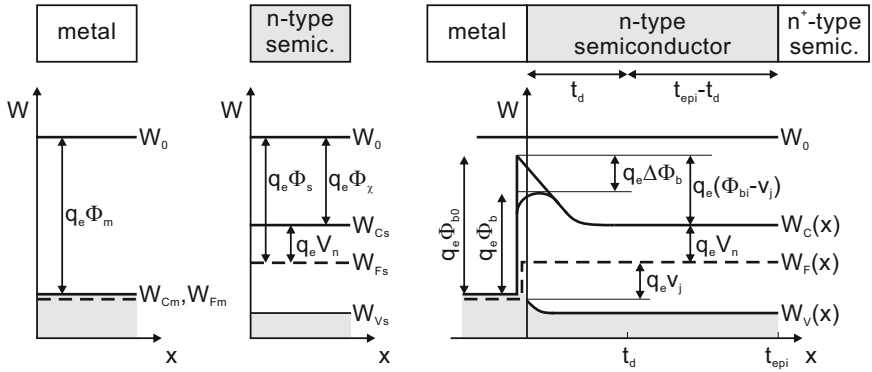

Figure 2.3: Energy band diagrams of metal (left), n-type semiconductor (midle) and metal to n-type semiconductor junction (right) with applied voltage v_j.

metal surface and an attractive force (image force) between electron and positive charge, resulting in $\Delta\Phi_\mathrm{b}$ [5].

In practice, the effective barrier heights Φ_b of m-n transitions are contrary to Eq. (2.13) almost independent of the metal work function $q_\mathrm{e}\Phi_\mathrm{m}$. At $x = 0$ the crystal lattice is disturbed, which leads to a large density of surface energy states in the semiconductor. This keeps the Fermi energy level $W_\mathrm{F}(0 + \mathrm{d}x)$ at a minimum level, greater than W_Fm, and makes the barrier height dependent on the semiconductor's surface only [5].

Derivation of Schottky Junction Capacitance From a technological point of view, the n-type semiconductor from Fig. 2.3 is an epitaxial layer (epilayer) with thickness t_epi, grown to highly doped n^+ substrate (buffer) material. In the following a derivation of the Schottky junction capacitance $C_\mathrm{j}(v_\mathrm{j})$ as a function of applied voltage v_j is presented. Without external voltage v_j, emitting electrons from n-type semiconductor to metal partly deplete the epilayer. The arising depleted epilayer with thickness t_d consists of positively charged ionized donor atoms hindering more electrons from emission to metal. The depletion layer's thickness and the corresponding junction capacitance are functions of v_j.

In the following, complete depletion is assumed, which means no electrons are left in the depletion region. This is known as depletion approximation. Furthermore, the epitaxial layer should be uniformly doped with donor concentration N_Depi, not a function of x. As a consequence, the space charge in the depletion layer does only depend on the positively charged ionized donor atoms and is constant for a given $t_\mathrm{d}(v_\mathrm{j})$. The charge per unit surface area S_j is therefore $Q_\mathrm{j}/S_\mathrm{j} = q_\mathrm{e}N_\mathrm{Depi}t_\mathrm{d}(v_\mathrm{j})$.

[5] In [4], the barrier height correction is given by $\Delta\Phi_\mathrm{b} \approx q_\mathrm{e}\sqrt{\frac{q_\mathrm{e}|E_\mathrm{max}|}{4\pi\epsilon_0\epsilon_\mathrm{r}}} \approx \sqrt[4]{\frac{q_\mathrm{e}^3 N_\mathrm{Depi}(\Phi_\mathrm{bi}-v_\mathrm{j})}{8\pi^2\epsilon_0^3\epsilon_\mathrm{r}^3}}$, with maximum electric field across the barrier E_max, the semiconductor's permittivity value ϵ_r and donor concentration N_Depi.

Fig. 2.4 illustrates the charge density $\rho(x)$ (top), charge per unit surface area $Q_\mathrm{j}/S_\mathrm{j}$ (middle) and electric field strength $E(x)$ (bottom) inside the m-n-n$^+$ system. On the metal surface, there is a negative surface charge, which equals the positive charge of the epilayer in magnitude. This is expressed using the Dirac[6] delta distribution in Fig. 2.4, for which the following properties hold true.

$$\delta(x) = \begin{cases} \infty & x = 0 \\ 0 & x \neq 0 \end{cases} \qquad \int_{-\infty}^{+\infty} \delta(x)\mathrm{d}x = 1 \tag{2.14}$$

According to Fig. 2.3, the potential difference (voltage) from $x = 0$ to $x = t_\mathrm{d}$ equals $(\Phi_\mathrm{bi} - v_\mathrm{j})$. The differential equation in Eq. (2.15) follows directly from the definition of voltage.

$$\begin{aligned} (v_\mathrm{j} - \Phi_\mathrm{bi}) &= -\int_0^{t_\mathrm{d}} E(x)\mathrm{d}x \\ \frac{\mathrm{d}\,(v_\mathrm{j} - \Phi_\mathrm{bi})}{\mathrm{d}x} &= -E(x) \\ \frac{\mathrm{d}^2\,(v_\mathrm{j} - \Phi_\mathrm{bi})}{\mathrm{d}x^2} &= -\frac{\mathrm{d}E(x)}{\mathrm{d}x} \end{aligned} \tag{2.15}$$

Gauss[7] law leads to Eq. (2.16).

$$\frac{\mathrm{d}E(x)}{\mathrm{d}x} = \frac{\rho(x)}{\epsilon_0 \epsilon_\mathrm{r}} \tag{2.16}$$

Comparing Eq. (2.15) with Eq. (2.16) the dependency of junction voltage v_j from charge density $\rho(x)$ is known.

$$\frac{\mathrm{d}^2\,(v_\mathrm{j} - \Phi_\mathrm{bi})}{\mathrm{d}x^2} = -\frac{\rho(x)}{\epsilon_0 \epsilon_\mathrm{r}} \tag{2.17}$$

[6]Paul Adrien Maurice Dirac (1902−1984), English physicist.
[7]Johann Carl Friedrich Gauss (1777−1855), German mathematician.

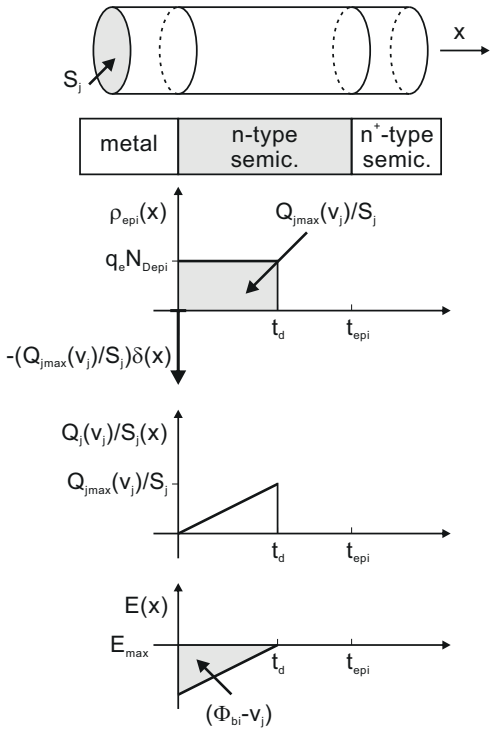

Figure 2.4: Charge density $\rho(x)$ (top), charge per unit surface area $Q_\mathrm{j}/S_\mathrm{j}$ (middle) and electric field strength $E(x)$ (bottom) inside the m-n-n^+ system.

Inserting charge density $\rho(x) = q_\mathrm{e} N_\mathrm{Depi}$, known from depletion approximation, into Eq. (2.17) and integrating twice over x leads to Eq. (2.18).

$$
\begin{aligned}
(v_\mathrm{j} - \Phi_\mathrm{bi}) &= -\frac{q_\mathrm{e}}{\epsilon_0 \epsilon_\mathrm{r}} \int_0^{t_d} \underbrace{\int_0^{x} N_\mathrm{Depi}(x^{'})\mathrm{d}x^{'}}_{\left[\frac{1}{2} N_\mathrm{Depi} x^2\right]_0^{t_\mathrm{d}}} \mathrm{d}x \\
(v_\mathrm{j} - \Phi_\mathrm{bi}) &= -\frac{q_\mathrm{e}}{\epsilon_0 \epsilon_\mathrm{r}} \frac{1}{2} N_\mathrm{Depi} t_\mathrm{d}^2
\end{aligned}
\tag{2.18}
$$

An expression of the voltage dependent depletion layer thickness $t_\mathrm{d}(v_\mathrm{j})$ is given by Eq. (2.19). The additional term $V_\mathrm{T} = \frac{kT}{q_\mathrm{e}}$, called thermal voltage, considers the contribution of the mobile carriers to the electric field ([5], p. 371). Whereas, k, T, q_e denote the Boltzmann[8] constant, temperature and elementary charge. The capacitance coefficient M allows for considering doping profiles different from uniform doping ($M_\mathrm{uniform} = 1/2$).

$$
\begin{aligned}
t_\mathrm{d}(v_\mathrm{j}) &= \sqrt{\frac{2\epsilon_0 \epsilon_\mathrm{r}}{q_\mathrm{e} N_\mathrm{Depi}} \left(\Phi_\mathrm{bi} - v_\mathrm{j}\right)} \\
t_\mathrm{d}(v_\mathrm{j}) &= \sqrt{\frac{2\epsilon_0 \epsilon_\mathrm{r}}{q_\mathrm{e} N_\mathrm{Depi}} \left(\Phi_\mathrm{bi} - v_\mathrm{j} - V_\mathrm{T}\right)} \\
\rightarrow t_\mathrm{d}(v_\mathrm{j}) &= \left[\frac{2\epsilon_0 \epsilon_\mathrm{r}}{q_\mathrm{e} N_\mathrm{Depi}} \left(\Phi_\mathrm{bi} - v_\mathrm{j} - V_\mathrm{T}\right)\right]^M
\end{aligned}
\tag{2.19}
$$

Hence, the junction charge per unit surface area $Q_\mathrm{j}/S_\mathrm{j}$ is known as a function of v_j.

$$
\begin{aligned}
Q_\mathrm{j}(v_\mathrm{j})/S_\mathrm{j} &= \int_{0-\mathrm{d}x}^{0+\mathrm{d}x} \rho(x)\mathrm{d}x = \int_{0+\mathrm{d}x}^{t_d} \rho(x)\mathrm{d}x = q_\mathrm{e} N_\mathrm{Depi} t_\mathrm{d}(v_\mathrm{j}) \\
Q_\mathrm{j}(v_\mathrm{j})/S_\mathrm{j} &= q_\mathrm{e} N_\mathrm{Depi} t_\mathrm{d}(v_\mathrm{j}) = \sqrt{2\epsilon_0 \epsilon_\mathrm{r} q_\mathrm{e} N_\mathrm{Depi} \left(\Phi_\mathrm{bi} - v_\mathrm{j} - V_\mathrm{T}\right)}
\end{aligned}
\tag{2.20}
$$

[8] Ludwig Eduard Boltzmann (1844–1906), Austrian physicist.

The capacitance per unit surface area $C_\mathrm{j}/S_\mathrm{j}$ is derived using a parallel plate capacitor model (Eq. (2.21)), where ϵ_r is the semiconductor's relative permittivity. The expressions are valid, as long as the epilayer is thick enough to prevent the depletion region from punching through to the substrate at high reverse voltages.

$$\begin{aligned} C_\mathrm{j}/S_\mathrm{j} &= \frac{\mathrm{d}Q_\mathrm{j}/S_\mathrm{j}}{\mathrm{d}v_\mathrm{j}} = \epsilon_0\epsilon_\mathrm{r}\frac{1}{t_d(v_\mathrm{j})} \\ C_\mathrm{j}/S_\mathrm{j} &= \left(\frac{q_\mathrm{e}\epsilon_0\epsilon_\mathrm{r}N_\mathrm{Depi}}{2\left(\Phi_\mathrm{bi}-v_\mathrm{j}-V_\mathrm{T}\right)}\right)^M \\ C_\mathrm{j}/S_\mathrm{j} &= \frac{C_\mathrm{jmax}/S_\mathrm{j}}{\left[1-v_\mathrm{j}/\left(\Phi_\mathrm{bi}-V_\mathrm{T}\right)\right]} \\ C_\mathrm{jmax}/S_\mathrm{j} &= C_\mathrm{j}/S_\mathrm{j}\Big|_{v_\mathrm{j}=0} = C_\mathrm{j0}/S_\mathrm{j} = \left(\frac{q_\mathrm{e}\epsilon_0\epsilon_\mathrm{r}N_\mathrm{Depi}}{2\left(\Phi_\mathrm{bi}-V_\mathrm{T}\right)}\right)^M \end{aligned} \tag{2.21}$$

The simple parallel plate capacitor model predicts infinite capacitance if $t_\mathrm{d} = 0$, instead of zero capacitance. Hence, C_j from Eq. (2.21) becomes infinite at $v_\mathrm{j} = \Phi_\mathrm{bi} - V_\mathrm{T}$. To overcome this problem, junction capacitance is defined in a different way. In case of $v_\mathrm{j} \leq F_\mathrm{C}\left(\Phi_\mathrm{bi} - V_\mathrm{T}\right)$ the derived expression in Eq. (2.22) is valid.

$$C_\mathrm{j} = C_\mathrm{j0}\left(1-\frac{v_\mathrm{j}}{\Phi_\mathrm{bi}-V_\mathrm{T}}\right)^{-M} \tag{2.22}$$

If $v_\mathrm{j} > F_\mathrm{C}\left(\Phi_\mathrm{bi} - V_\mathrm{T}\right)$, Eq. (2.23) is used.

$$C_\mathrm{j} = \frac{C_\mathrm{j0}}{\left(1-F_\mathrm{C}^M\right)}\left\{1+\left[\frac{M}{(\Phi_\mathrm{bi}-V_\mathrm{T})(1-F_\mathrm{C})}\right]\left[v_\mathrm{j}-F_\mathrm{C}\left(\Phi_\mathrm{bi}-V_\mathrm{T}\right)\right]\right\} \tag{2.23}$$

The parameter F_C usually varies between 0.4 to 0.7 and is implemented within the common SPICE model DIODE (default value $F_\mathrm{C} = 0.5$, [6]). Alternatively, circuit simulators often prevent problems with infinite capacitance by using increments of charge to estimate displacement

current $i_{\mathrm{C}}(v_{\mathrm{j}}, t)$ through the capacitor instead of the capacitance function ([7, 8]).

$$i_{\mathrm{C}}(v_{\mathrm{j}}, t) = \frac{\mathrm{d}Q_{\mathrm{j}}}{\mathrm{d}t} = \left.\frac{\mathrm{d}Q_{\mathrm{j}}}{\mathrm{d}v}\right|_{v=v_{\mathrm{j}}(t)} \frac{\mathrm{d}}{\mathrm{d}t} v_{\mathrm{j}}(t) \tag{2.24}$$

Derivation of Schottky Junction Current In 1942 Bethe[9] studied the current transport mechanism through the Schottky barrier based on pure thermionic emission [9]. It assumes all electrons with sufficiently high velocity component perpendicular to the barrier emit through the barrier. With Maxwell velocity distribution, the current from n-type semiconductor material to metal i_{jSM} and vice versa i_{jMS} is given by Eq. (2.25).

$$\begin{aligned} i_{\mathrm{jSM}} &= I_{\mathrm{S}} \left[\exp\left(\frac{v_{\mathrm{j}}}{V_{\mathrm{T}}}\right)\right] \\ i_{\mathrm{jMS}} &= -I_{\mathrm{S}} \\ I_{\mathrm{S}} &= A^{\star} T^2 S_{\mathrm{j}} \exp\left(\frac{-q_{\mathrm{e}}\Phi_{\mathrm{b}}}{kT}\right) \\ A^{\star} &= \frac{4\pi q_{\mathrm{e}} m^{\star} k^2}{h^3} \end{aligned} \tag{2.25}$$

Whereas $A^{\star}$ is the Richards constant from Richardson[10] law, $m^{\star}$ is the effective electron mass [10] and the total junction current i_{j} is the sum of i_{jSM} and i_{jMS}.

$$i_{\mathrm{j}}(v_{\mathrm{j}}) = i_{\mathrm{jSM}} + i_{\mathrm{jMS}} = I_{\mathrm{S}} \left[\exp\left(\frac{v_{\mathrm{j}}}{V_{\mathrm{T}}}\right) - 1\right] \tag{2.26}$$

Four years earlier, in 1938 Schottky[11] derived an expression for the junction current based on the diffusion theory (Fick's[12] first law,

[9] Hans Albrecht Bethe (1906−2005), German physicist.
[10] Sir Owen Willans Richardson (1879−1959), British physicist.
[11] Walter Hermann Schottky (1886−1976), German physicist.
[12] Adolf Eugen Fick (1829−1901), German physician and physiologist.

[11]). The result has the form of Eq. (2.26), which is also known as Shockley[13] equation, but suggests a different expression for the reverse saturation current.

$$I_{\mathrm{S}} = \underbrace{\mu_{\mathrm{e}} N_{\mathrm{C}} \sqrt{\frac{2q_{\mathrm{e}}(\Phi_{\mathrm{bi}} - v_{\mathrm{j}})N_{\mathrm{Depi}}}{\epsilon_0 \epsilon_{\mathrm{r}}}}}\, S_{\mathrm{j}} \exp\left(\frac{-q_{\mathrm{e}}\Phi_{\mathrm{b}}}{kT}\right) \tag{2.27}$$

The thermionic emission-diffusion theory from Crowell and Sze unifies the approaches from Bethe and Schottky and also accounts for the probability of quantum mechanical tunneling (field emission) of electrons through the barrier. It suggests the introduction of the modified Richards constant $A^{\star\star}$ in Eq. (2.28), which is not a true constant (compare [5] for detailed derivation).

$$I_{\mathrm{S}} = A^{\star\star} T^2 S_{\mathrm{j}} \exp\left(\frac{-q_{\mathrm{e}}\Phi_{\mathrm{b}}}{kT}\right) \tag{2.28}$$

Supplementing Eq. (2.28) with the ideality factor $\eta = 1 \ldots 2$ allows for modelling parasitic effects, neglected in the above derivations ([12], p. 19).

$$I_{\mathrm{S}} = A^{\star\star} T^2 S_{\mathrm{j}} \exp\left(\frac{-\Phi_{\mathrm{b}}}{\eta V_{\mathrm{T}}}\right) \quad V_{\mathrm{T}} = \frac{kT}{q_{\mathrm{e}}} \tag{2.29}$$

Reported values of $A^{\star\star}$ differ significantly[14]. Fortunately, when extracting the barrier height $\Phi_{\mathrm{b}} \sim \ln(1/A^{\star\star})$ from Eq. (2.29) the value of $A^{\star\star}$ has little effect on accuracy.

2.2.2 Diode Architectures

Fig. 2.5 illustrates a 3D view and cut through (BB′) a planar GaAs Schottky diode, intended for use in hybrid systems as discrete com-

[13] William Bradford Shockley Jr. (1910−1989), American physicist.

[14] Room temperature values in units of $\mathrm{A}/\left(\mathrm{cm}^2\mathrm{K}^2\right)$ are [4] $A^{\star\star} \approx 100$, [13] $A^{\star\star}_{\mathrm{n-Si}} \approx 7.92$, $A^{\star\star}_{\mathrm{n-GaAs}} \approx 230.4$, [12] $A^{\star\star}_{\mathrm{Si}} \approx 96$, $A^{\star\star}_{\mathrm{GaAs}} \approx 4.4$, [5] $A^{\star\star}_{\mathrm{n-Si}} \approx 252$, $A^{\star\star}_{\mathrm{n-GaAs}} \approx 7.2 \ldots 144$.

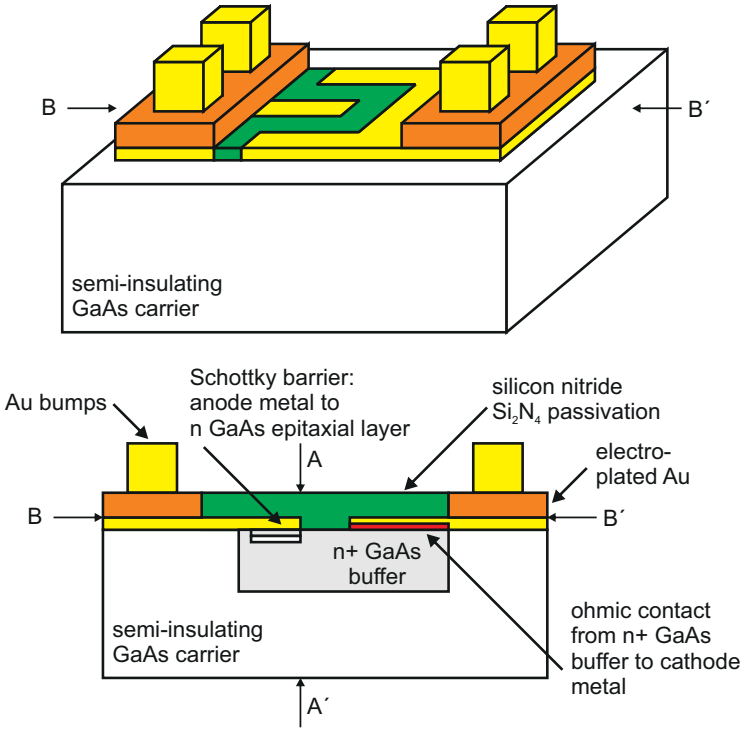

Figure 2.5: 3D view (top) of a planar buried epitaxial layer GaAs Schottky diode like UMS DBES105a and BB´ cutaway view (bottom), showing epilayer, buffer layer and ohmic contact.

ponent. The n-type epitaxial layer is grown on highly doped n^+ GaAs buffer substrate (gray), which is surrounded by semi-insulating GaAs carrier. On the left side, the anode metal contacts the epilayer, whereas on the right side an ohmic contact (red) from cathode metal to the buffer is realized. Silicon nitride (Si_2N_4) passivation is shown in green. Electroplated Au at anode and cathode, together with bumps allow for easy assembly to planar circuits.

The cross-sectional view AA´ and a topview are shown in Fig. 2.6 and Fig. 2.7, respectively. This architecture is called buried epi-

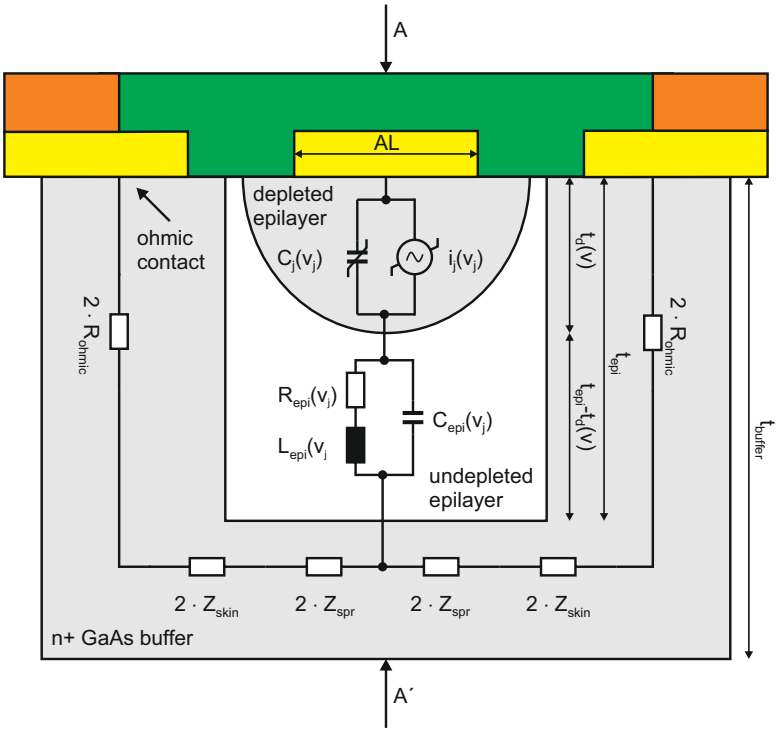

Figure 2.6: AA´ cutaway view of a planar buried epitaxial layer GaAs Schottky diode from Fig. 2.5.

taxial layer Schottky diode. The frequency multipliers, presented in sections 2.6, 2.7 utilize such a diode, the DBES105a from United Monolithic Semiconductors (UMS).

Fig. 2.6 further includes an equivalent circuit model. Beside the nonlinear epilayer junction capacitance $C_\mathrm{j}(v_\mathrm{j})$ from Eq. (2.21, 2.22, 2.23) and the nonlinear diode current $i_\mathrm{j}(v_\mathrm{j})$ from Eq. (2.26, 2.29), linear components of the undepleted epilayer $R_\mathrm{epi}(v_\mathrm{j})$, $L_\mathrm{epi}(v_\mathrm{j})$, $C_\mathrm{epi}(v_\mathrm{j})$ and buffer layer Z_spr, Z_skin, R_ohmic are included.

There are several different planar diode architectures for microwave, millimeter-wave and terahertz applications. Some of which are illus-

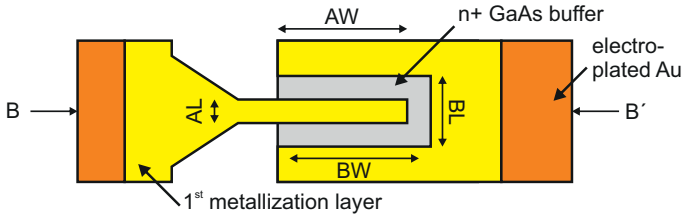

Figure 2.7: Top view of a planar buried epitaxial layer GaAs Schottky diode from Fig. 2.5.

trated in Fig. 2.8. From top to bottom, Fig. 2.8 shows the buried epitaxial layer Schottky diode #1, followed by an architecture with air bridge anode metal #2 and an etched surface channel to reduce parasitic capacitances. Some diodes utilize air bridges at anode and cathode, contacting the epilayer and buffer layer mesa #3. The bulk diode #4 exhibits vertical current flow from top to bottom and is either used for low frequency applications in through-hole-technique (THT) or manufactured several times on a single wafer (honeycomb array structure, [14]) for whisker contacting. The architecture #5 is a planar realization of #4 with quasi-vertical current flow from anode to backside metal [15]. Process techniques are explained in [16, 17].

For all these architectures, the epilayer dimensions are small compared to the minimum wavelength $\lambda_{\min} = c_0/\left(\sqrt{\epsilon_r} f_{\max}\right)$ and therefore lumped description of the actual Schottky junction $C_j, i_j\left(v_j\right)$ and the undepleted epilayer Z_{epi} is possible. The other linear parameters of the equivalent circuit of Fig. 2.9, Z_{spr}, Z_{skin}, and the influence of the first metallization layer, electroplated Au, passivation and semi-insulating GaAs carrier are not inherent diode properties but strongly depend on the interaction with the electromagnetic field. An extreme contrast is depicted in Fig. 2.10. It compares hybrid integration (left) to monolithic microwave integrated circuit (MMIC) usage (right) of a planar diode. In the hybrid case, the semi-insulating GaAs carrier constitutes a parasitic element with an electromagnetic field penetration that depends on the chosen planar waveguide, sub-

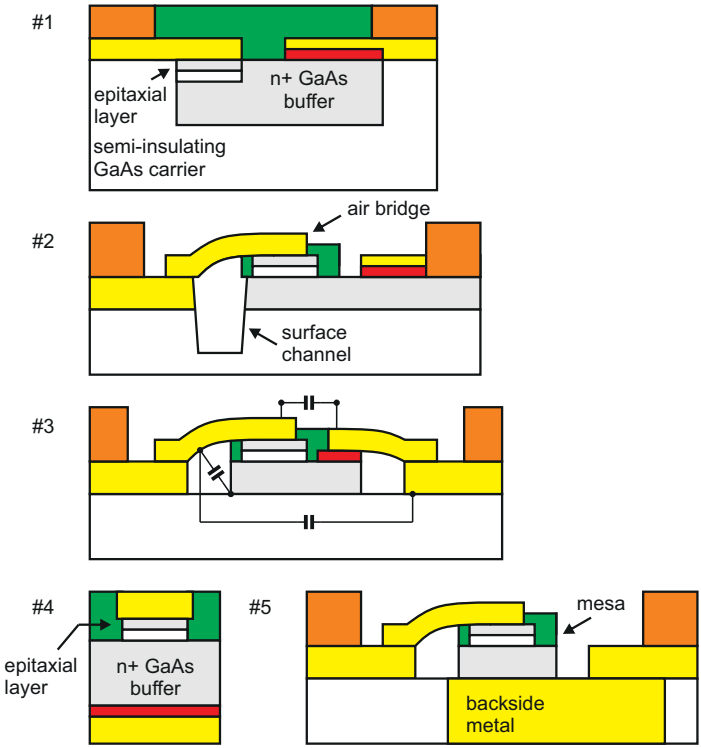

Figure 2.8: Different planar diode architectures. From top to bottom, buried epitaxial layer, anode finger bridge with surface channel, mesa diode with anode and cathode finger bridge and surface channels, bulk diode (e.g. part of whisker contacted diode array) and mesa diode with vertical current flow to cathode.

strate material and interconnect solution. In this sense, a coplanar waveguide (CPW) incorporates less interaction with the carrier than it is with microstrip line (MSL) and the capacitances, shown in the third row of Fig. 2.8, have smaller values. In case of monolithic integration, the semi-insulating GaAs carrier acts as the substrate material of the feeding waveguide and therefore has severe influence

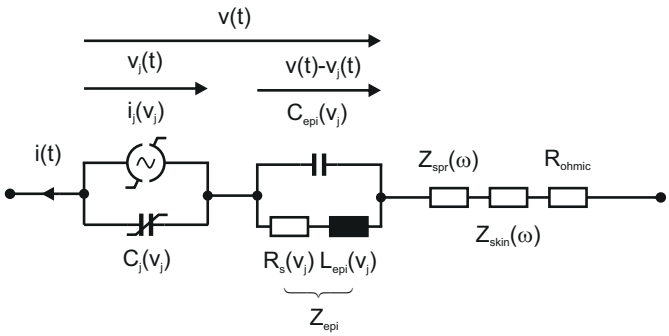

Figure 2.9: Equivalent circuit of a planar GaAs Schottky diode, including the effects of epilayer, buffer layer and ohmic contacts. The influence of the semi-insulating GaAs carrier and waveguide interconnection are not covered.

on the characteristic impedance and propagation coefficient but is not necessarily parasitic.

An analytical modelling approach of the diode's linear circuit part is presented in the next section, toegether with comments on 3D EM modelling of the buffer layer, compact modelling and the SPICE model DIODE.

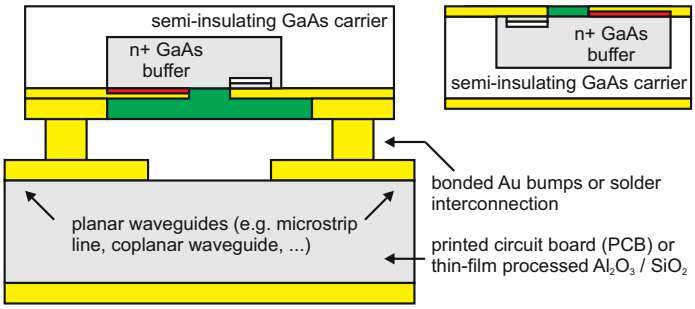

Figure 2.10: Planar diode as a discrete component for hybrid integration (left) and planar diode as part of a monolithic microwave integrated circuit (right).

2.2.3 Linear Parts of Diode Model

In the following we derive analytical equations to describe the linear parts of the diode model, the undepleted epilayer Z_{epi}, highly doped buffer layer $Z_{\mathrm{spr}} + Z_{\mathrm{skin}}$ and ohmic contacts R_{ohmic}. In both cases simple models are chosen as a starting point. To cover the high frequency behaviour, enhanced modelling of the material properties, electrical permittivity and conductivity, is applied. This last fact allows for covering arbitrary geometries with 3D EM simulations based on dispersive materials. Whereas, the analytical equations are valid for rather simple geometries only.

Undepleted Epitaxial Layer The modelling approach for the undepleted epilayer with thickness $t_{\mathrm{u}}(v_{\mathrm{j}}) = t_{\mathrm{epi}} - t_{\mathrm{d}}(v_{\mathrm{j}})$ in Fig. 2.9 includes three components, covering resistive effects R_{epi}, displacement current C_{epi} and carrier inertia effects L_{epi}. The undepleted epilayer is the main contributor to the diode's series resistance.

$$Z_{\mathrm{epi}} = (R_{\mathrm{epi}} + j\omega L_{\mathrm{epi}}) \parallel (j\omega C_{\mathrm{epi}})^{-1} \tag{2.30}$$

In the following derivations, the simple cylindrical geometry of Fig. 2.11, with the anode diameter a and buffer radius b, is assumed. Utilizing the standard lumped resistor model (Pouillet's[15] law) $R = 1/\sigma \frac{\ell}{S}$ the element R_{epi} at DC is given by Eq. (2.31).

$$\begin{aligned} R_{\mathrm{epi}}(v_{\mathrm{j}})\Big|_{f=0} &= \frac{t_{\mathrm{u}}(v_{\mathrm{j}})}{\sigma_{\mathrm{epi}} S_{\mathrm{j}}} \\ \sigma_{\mathrm{epi}} &= q_{\mathrm{e}} \mu_{\mathrm{e}} N_{\mathrm{Depi}} \end{aligned} \tag{2.31}$$

In Eq. (2.31), the electron mobility in the epilayer μ_{e} depends on the doping concentration N_{Depi} and temperature T. Throughout this

[15] Claude Servais Mathias Pouillet (1791–1868), French physicist.

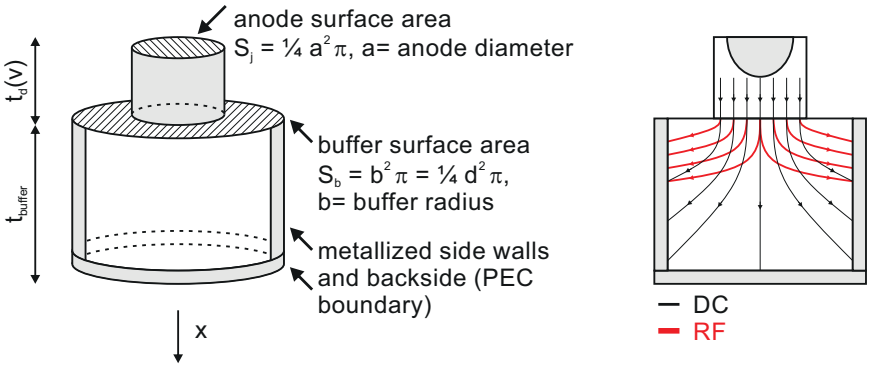

Figure 2.11: Simple cylindrical model of epilayer and buffer layer (left) for analytical analysis and current density lines at DC and RF (right).

work, the dependency is covered by the empirical low-field electron mobility model from [18], given by Eq. (2.32).

$$\mu_\mathrm{e}\left(N_\mathrm{D},T\right)=10^4\mu_\mathrm{min}+\frac{10^4\mu_\mathrm{max}\left(\frac{300\ \mathrm{K}}{T}\right)^{\theta_1}-10^4\mu_\mathrm{min}}{1+\left[\frac{10^{-6}N_\mathrm{D}}{10^{-6}N_\mathrm{ref}\left(\frac{T}{300\ \mathrm{K}}\right)^{\theta_2}}\right]^{\theta_3}} \tag{2.32}$$

The results of Fig. 2.12 are based on the parameters for electrons in GaAs (Eq. (2.33)).

$$\begin{aligned}&\mu_\mathrm{min}/\mu_\mathrm{max}=0.94/0.05\ \mathrm{m^2V^{-1}s^{-1}}\\&N_\mathrm{ref}=6\cdot10^2\ \mathrm{m^{-3}}\quad\theta_1=2.1\quad\theta_2=3.0\quad\theta_3=0.394\end{aligned} \tag{2.33}$$

The planar junction model of Eq. (2.31) holds true as long as the effective anode diameter a is large compared to the epilayer thickness. Typical values are $t_\mathrm{epi}\leq0.1$ µm and $a\approx1$ to 6 µm. R_epi has only weak dependency on v_j, due to $t_\mathrm{u}(v_\mathrm{j})=t_\mathrm{epi}-t_\mathrm{d}(v_\mathrm{j})$. It has a maximum value at high forward bias, which advises to use $t_\mathrm{epi}=\max\left(t_\mathrm{u}(v_\mathrm{j})\right)$ as worst case approximation. Empirical models are available to include the increase of R_epi due to carrier velocity saturation at high drive

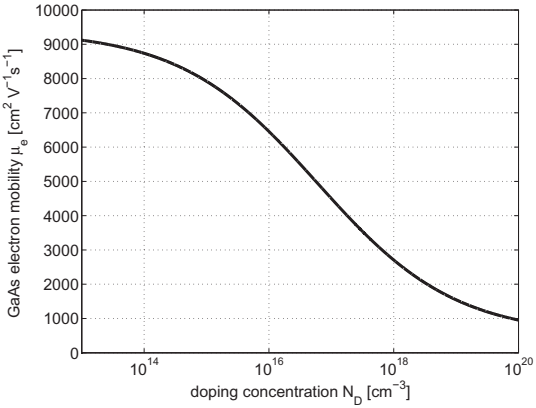

Figure 2.12: Empirical low-field electron mobility μ_e of GaAs versus doping concentration N_D from [18].

level (DC and / or RF, [19]). Beside resistive effects R_{epi}, displacement current through the undepleted epilayer and carrier inertia effects, due to nonzero effective mass $m_e^\star \sim m_e$ of the electrons [10], are covered by C_{epi} and L_{epi}.

Drude's Dispersion Model Derivation is based on Drude's[16] dispersion model [20, 21]. The undepleted epilayer is assumed to consist of a negatively charged electron gas (plasma), the valence electrons, and a positively charged background, the donor atoms. The electrons move under the influence of an applied electric field. The electron's (mean) drift velocity component ($v_d \parallel x$) in parallel with the electric field $E(x)$ increases up to a maximum value v_{dmax} before collision (scattering event) with lattice atoms leads to randomization of v_d. The average time between such scattering effects (collision time) is the reciprocal of the scattering frequency $\omega_s = \frac{q_e}{m^\star \mu_e}$, which is assumed to be constant for all involved electrons. With Newton's[17] second law,

[16] Paul Karl Ludwig Drude (1863−1906), German physicist.
[17] Sir Isaac Newton (1642−1727), English physicist.

this leads to an equation of motion for electrons, which belongs to a simplified version of the Lorentz[18] oscillator model (Eq. (2.34)).

$$\begin{aligned} m^\star \frac{\mathrm{d}^2 x(t)}{\mathrm{d}t^2} + m^\star \omega_\mathrm{s} \frac{\mathrm{d}x(t)}{\mathrm{d}t} &= q_\mathrm{e} E(x) \\ m^\star \frac{\mathrm{d}v_\mathrm{d}}{\mathrm{d}t} + m^\star \omega_\mathrm{s} v_\mathrm{d} &= q_\mathrm{e} E(x) \end{aligned} \tag{2.34}$$

The complete Lorentz oscillator model does further include a spring force F_spring, according to Hooke's law[19]. This allows for modelling of bound electrons and Eq. (2.34) takes the form of Eq. (2.35). Bound electrons are neglected in the following.

$$\underbrace{m^\star \frac{\mathrm{d}^2 x(t)}{\mathrm{d}t^2}}_{\text{inertial}} + \underbrace{m^\star \omega_\mathrm{s} \frac{\mathrm{d}x(t)}{\mathrm{d}t}}_{\text{damping}} + \underbrace{m^\star \omega_\mathrm{bound}^2 x(t)}_{\text{restoring},F_\mathrm{spring}} = \underbrace{q_\mathrm{e} E(x)}_{\text{driving}} \tag{2.35}$$

The scattering frequency ω_s is found from the static solution of Eq. (2.34). At DC, it is $\frac{\mathrm{d}^2 x(t)}{\mathrm{d}t^2} = 0$ and $\frac{\mathrm{d}x(t)}{\mathrm{d}t} = v_\mathrm{d} = \text{constant}$. Hence, Eq. (2.34) becomes Eq. (2.36).

$$\omega_\mathrm{s} = \frac{q_\mathrm{e} E(x)}{m^\star v_\mathrm{d}} \tag{2.36}$$

The drift velocity is given by $v_\mathrm{d} = \frac{J(x)}{q_\mathrm{e} N}$, with Ohm's law[20] $J(x) = \sigma_\mathrm{DC} E(x)$ this leads to $v_\mathrm{d} = \frac{\sigma_\mathrm{DC}}{q_\mathrm{e} N} E(x)$ and ω_s.

$$\omega_\mathrm{s} = \frac{q_\mathrm{e}^2 N}{m^\star \sigma_\mathrm{DC}} \tag{2.37}$$

[18] Hendrik Antoon Lorentz (1853−1928), Dutch physicist.
[19] Robert Hooke (1635−1703), English scientist.
[20] Georg Simon Ohm (1789−1854), German physicist.

Replacing the bulk DC conductivity $\sigma_{\mathrm{DC}} = q_{\mathrm{e}}\mu_{\mathrm{e}}N$, the scattering frequency becomes

$$\omega_{\mathrm{s}} = \frac{q_{\mathrm{e}}}{m^{\star}\mu_{\mathrm{e}}}. \tag{2.38}$$

Inserting the trial solution $x(t) = x_0 \exp(j\omega t)$ into Eq. (2.34) leads to the electron displacement $x(t)$.

$$x(t) = \frac{q_{\mathrm{e}}E(x)}{-m^{\star}\omega^2 + j\omega\omega_{\mathrm{s}}m^{\star}} \tag{2.39}$$

Dielectric polarization density per unit volume $\mathbf{P}(x)$ is defined as sum of the dipole moments per unit volume. Dipole moments of the electron gas are given by the electron's charge q_{e} times electron displacement $x(t)$. Hence, the dielectric polarization density for the one-dimensional case is

$$\begin{aligned} P_{\mathrm{e}} &= q_{\mathrm{e}}x(t)N \\ P_{\mathrm{e}} &= \frac{q_{\mathrm{e}}^2 N E(x)}{-m^{\star}\omega^2 + j\omega\omega_{\mathrm{s}}m^{\star}}. \end{aligned} \tag{2.40}$$

P_{D} covers the polarization density of the positively charged background (donor atoms). For GaAs, the relative permittivity ϵ_{r} equals 12.9 and is often referred to as ϵ_{∞} in literature.

$$P_{\mathrm{D}} = \epsilon_0\chi E = \epsilon_0\left(\epsilon_{\mathrm{r}} - 1\right)E \tag{2.41}$$

Inserting Eq. (2.40) and Eq. (2.41) into Maxwell's[21] constitutive relations,[22] it is possible to derive an expression for the frequency

[21] James Clerk Maxwell (1831−1879), Scottish physicist.
[22] Eq. (2.42) includes Maxwell's equations in integral and differential form,

dependent, intrinsic bulk permittivity $\epsilon(\omega)$ of the semiconductor (electron gas and donor atoms) as a function of the polarization density.

$$\begin{aligned} D = \epsilon(\omega)E &= \epsilon_0 E + P_\mathrm{D} + P_\mathrm{e} \\ &= \epsilon_0 E + \epsilon_0 \left(\epsilon_\mathrm{r} - 1\right) E + P_\mathrm{e} \\ &= \epsilon_0 \epsilon_\mathrm{r} E + P_\mathrm{e} \\ \epsilon(\omega) &= \epsilon_0 \epsilon_\mathrm{r} \left(1 + \frac{P_\mathrm{e}}{\epsilon_0 \epsilon_\mathrm{r} E}\right) \end{aligned} \tag{2.43}$$

Inserting Eq. (2.37) and Eq. (2.40) into Eq. (2.43) leads to Eq. (2.44).

$$\epsilon(\omega) = \epsilon_0 \epsilon_\mathrm{r} \left(1 + \frac{\frac{q_\mathrm{e}^2 N}{\epsilon_0 \epsilon_\mathrm{r} m^\star}}{-\omega^2 + j\omega\omega_\mathrm{s}}\right) = \epsilon_0 \epsilon_\mathrm{r} \left(1 + \frac{\omega_\mathrm{s} \frac{\sigma_\mathrm{DC}}{\epsilon_0 \epsilon_\mathrm{r}}}{-\omega^2 + j\omega\omega_\mathrm{s}}\right) \tag{2.44}$$

$$\begin{aligned} \text{Faraday's law:} \quad & \oint_\ell \mathbf{E}\mathrm{d}\boldsymbol{\ell} = -\frac{\partial}{\partial t} \int_\mathbf{S} \mathbf{B}\mathrm{d}\mathbf{S} \\ \text{Ampère's law:} \quad & \oint_\ell \mathbf{H}\mathrm{d}\boldsymbol{\ell} = \int_\mathbf{S} \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}\right) \mathrm{d}\mathbf{S} \\ \text{Gauss' law:} \quad & \oint_\mathbf{S} \mathbf{B}\mathrm{d}\mathbf{S} = 0 \qquad \oint_\mathbf{S} \mathbf{D}\mathrm{d}\mathbf{S} = Q \\ \text{Constitutive equations:} \quad & \mathbf{D} = \epsilon_0 \epsilon_r \mathbf{E} \qquad \mathbf{B} = \mu_0 \mu_r \mathbf{H} \\ \text{Faraday's law:} \quad & \mathrm{curl}\mathbf{E} = \nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \\ \text{Ampère's law:} \quad & \mathrm{curl}\mathbf{H} = \nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \\ \text{Gauss' law:} \quad & \mathrm{div}\mathbf{D} = \nabla \cdot \mathbf{D} = \rho \\ & \mathrm{div}\mathbf{B} = \nabla \cdot \mathbf{B} = 0 \\ \text{Constitutive equations:} \quad & \mathbf{D} = \epsilon_0 \epsilon_r \mathbf{E} \qquad \mathbf{B} = \mu_0 \mu_r \mathbf{H} \end{aligned} \tag{2.42}$$

With the abbreviation $\omega_\mathrm{d} = \frac{\sigma_\mathrm{DC}}{\epsilon_0 \epsilon_\mathrm{r}}$, called dielectric relaxation frequency, Eq. (2.44) simplifies to the final result Eq. (2.45).

$$\epsilon(\omega) = \epsilon_0 \epsilon_\mathrm{r} \left(1 - \frac{\omega_\mathrm{s} \omega_\mathrm{d}}{\omega^2 - j\omega\omega_\mathrm{s}} \right) \tag{2.45}$$

Drude's Dispersion expressed by Effective Material Properties
$\epsilon(\omega)$ has been introduced as the frequency dependent, intrinsic bulk permittivity in Maxwell's constitutive relations. With Ampère's law[23] in the frequency domain (Eq. (2.46)), the effective permittivity $\epsilon_\mathrm{eff}(\omega)$ and effective conductivity σ_eff are introduced, which both cover conductor and displacement current phenomena.

$$\begin{aligned}
\mathrm{curl}\mathbf{H} &= \mathbf{J} + j\omega\mathbf{D} \\
\mathrm{curl}\mathbf{H} &= \left[\sigma(\omega) + j\omega\epsilon(\omega)\right]\mathbf{E} = \sigma_\mathrm{eff}\mathbf{E} \\
\mathrm{curl}\mathbf{H} &= j\omega\left[\epsilon(\omega) - j\frac{\sigma(\omega)}{\omega}\right]\mathbf{E} = j\omega\epsilon_\mathrm{eff}\mathbf{E} \\
\epsilon_\mathrm{eff}(\omega) &= \epsilon_0\epsilon_\mathrm{r}\left[1 + \frac{\sigma(\omega)}{j\omega\epsilon_0\epsilon_\mathrm{r}}\right] \\
\sigma_\mathrm{eff}(\omega) &= j\omega\epsilon_\mathrm{eff}
\end{aligned} \tag{2.46}$$

Assuming an intrinsic bulk conductivity $\sigma(\omega) = \frac{\sigma_{DC}}{1+j\omega/\omega_s}$ and inserting into the expression of effective permittivity from Eq. (2.46) leads to the result of Eq. (2.47), which equals the expression in Eq. (2.45). The geometric average of the dielectric relaxation frequency and the scattering frequency is called plasma frequency $\omega_\mathrm{p} = \sqrt{\omega_\mathrm{d}\omega_\mathrm{s}}$.

$$\epsilon_\mathrm{eff}(\omega) = \epsilon_0\epsilon_\mathrm{r}\left[1 - \frac{\omega_\mathrm{s}\omega_\mathrm{d}}{\omega^2 - j\omega\omega_\mathrm{s}}\right] = \epsilon_0\epsilon_\mathrm{r}\left[1 - \frac{\omega_\mathrm{p}^2}{\omega^2 - j\omega\omega_\mathrm{s}}\right] \tag{2.47}$$

[23] Andrè-Marie Ampère (1775–1836), French physicist.

The corresponding expression for the effective conductivity value is shown in Eq. (2.48).

$$\sigma_{\mathrm{eff}}(\omega) = \sigma(\omega) + j\omega\epsilon(\omega) = \frac{\sigma_{\mathrm{DC}}}{1 + j\omega/\omega_{\mathrm{s}}} + j\omega\epsilon_0\epsilon_{\mathrm{r}} \tag{2.48}$$

Hence, Drude's dispersion model is applied to Maxwell's equations by use of the effective permittivity $\epsilon_{\mathrm{eff}}(\omega)$ or effective conductivity $\sigma_{\mathrm{eff}}(\omega)$ with the intrinsic bulk conductivity $\sigma(\omega) = \frac{\sigma_{\mathrm{DC}}}{1+j\omega/\omega_{\mathrm{s}}}$ and intrinsic bulk permittivity $\epsilon(\omega) = \epsilon_0\epsilon_{\mathrm{r}}$. In combination with numerical 3D electromagnetic field solvers, covering the effects of arbitrarily shaped structures following Drude's dispersion is possible [22–24].

Replacing the DC conductivity σ_{epi} in the expression of R_{epi} (Eq. (2.31)) by the effective conductivity $\sigma_{\mathrm{eff}}(\omega)$ from Drude's dispersion model yields the complex impedance Z_{epi} (Eq. (2.49)). As Drude's model has been derived for bulk materials. Crowe [25] suggested to include the influence of the epilayer thickness on the scattering frequency. Hence, an effective scattering frequency for thin layers $\omega_{\mathrm{seff}} = \frac{q_{\mathrm{e}}}{m^\star\mu_{\mathrm{e}}} + \frac{v_{\mathrm{d}}}{t_{\mathrm{u}}}$ should be used, whereas the (mean) drift velocity is approximated by its maximum value. In GaAs it is $v_{\mathrm{dmax}} \approx 2 \cdot 10^5 \frac{\mathrm{m}}{\mathrm{s}}$.

$$\begin{aligned} R_{\mathrm{epi}} &= \frac{t_{\mathrm{u}}(v_{\mathrm{j}})}{\sigma_{\mathrm{epi}} S_{\mathrm{j}}} = \frac{t_{\mathrm{u}}(v_{\mathrm{j}})}{q_{\mathrm{e}}\mu_{\mathrm{e}} N_{\mathrm{Depi}} S_{\mathrm{j}}} \\ \sigma_{\mathrm{eff}}(\omega) &= \sigma_{\mathrm{DC}} \left[\frac{1}{1 + j\omega/\omega_{\mathrm{seff}}} + j\frac{\omega}{\omega_{\mathrm{d}}}\right] \\ Z_{\mathrm{epi}} &= R_{\mathrm{epi}} \left(\frac{1}{1 + j(\omega/\omega_{\mathrm{seff}})} + j\omega/\omega_{\mathrm{d}}\right)^{-1} \end{aligned} \tag{2.49}$$

Inspecting Eq. (2.49), the equivalent circuit elements R_{epi}, C_{epi}, and L_{epi} of the epilayer are all known (Eq. (2.50)).

$$\begin{aligned} L_{\mathrm{epi}}(v_{\mathrm{j}}) &= R_{\mathrm{epi}}(v_{\mathrm{j}})/\omega_{\mathrm{seff}} \\ C_{\mathrm{epi}}(v_{\mathrm{j}}) &= \epsilon_0\epsilon_{\mathrm{r}} \frac{S_{\mathrm{j}}}{t_{\mathrm{u}}(v_{\mathrm{j}})} \qquad t_{\mathrm{epi}} = t_{\mathrm{d}}(v_{\mathrm{j}}) + t_{\mathrm{u}}(v_{\mathrm{j}}) \end{aligned} \tag{2.50}$$

C_{epi} in Eq. (2.50) equals the parallel capacitor model. At the introduced dielectric relaxation frequency ω_{d}, the element values R_{epi} and $(\omega C_{\mathrm{epi}})^{-1}$ have equal values. Hence, displacement current becomes dominant at $\omega > \omega_{\mathrm{d}}$. Resonance between carrier inertia and electron displacement appears at the plasma frequency $\omega_{\mathrm{p}} = \sqrt{\omega_{\mathrm{s}}\omega_{\mathrm{d}}}$.

Buffer Layer According to Fig. 2.11, the epilayer and buffer layer are assumed to have cylindrical shapes with anode diameter a and buffer diameter $2b$. In 1967 Dickens [26], derived expressions for the spreading resistance R_{spr} and impedance due to skin effect Z_{skin}, both dependent on the geometry of Fig. 2.11. The increase of buffer layer resistance, due to current flow spreading into the n^+ buffer layer is considered by R_{spr}.

$$R_{\mathrm{spr}} = \frac{\operatorname{atan}\left(\frac{2b}{a}\right)}{\pi\sigma_{\mathrm{b}}a} \tag{2.51}$$

The complex impedance Z_{skin} covers the current concentration near the buffer layer surface as a function of frequency and geometry (right side of Fig. 2.11).

$$Z_{\mathrm{skin}} = \frac{(1+j)}{\sigma_{\mathrm{b}}\delta_{\mathrm{skin}}}\frac{1}{2\pi}\ln\left(\frac{2b}{a}\right) \quad \delta_{\mathrm{skin}} = \sqrt{\frac{2}{\omega\mu_0\sigma_{\mathrm{b}}}} \tag{2.52}$$

Dickens assumed conductive sidewalls and conductive backside together with a large buffer layer thickness $t_{\mathrm{b}} >> d$, $t_{\mathrm{b}} >> 2b$. These are simplifications, incorrect for both, whisker contacted Schottky diodes and planar Schottky diodes (compare Fig. 2.8). Dickens' expressions are good approximations, if appropriate effective values of anode diameter a_{eff} and buffer radius b_{eff} are chosen instead of the real physical values. If the buffer layer diameter is much larger than the anode diameter, it is

$$\lim_{(2b)/a\to\infty} \operatorname{atan}\left(\frac{2b}{a}\right) = \frac{\pi}{2} \tag{2.53}$$

and Eq. (2.51) simplifies to $R_{\mathrm{spr}} = \frac{1}{2\sigma_{\mathrm{b}} a}$.

Dickens' expression for Z_{skin} in Eq. (2.52) consists of the classical skin effect formula with skin depth δ_{skin} combined with a geometry dependent term.

As it is with other surface impedances, the skin effect impedance is derived from the intrinsic wave impedance for bulk materials Z_{w}. The wave impedance is defined as the phasor ratio of the electric and magnetic field strengthes perpendicular to the direction of propagation. Eq. (2.54) includes the dependency of Z_{w} from material parameters and the propagation coefficient γ.

$$\begin{aligned} Z_{\mathrm{w}} :=& \frac{E_{\perp}(x,y,z)}{H_{\perp}(x,y,z)} \\ Z_{\mathrm{w}} =& \sqrt{\frac{\mu(\omega)}{\epsilon_{\mathrm{eff}}(\omega)}} = \sqrt{\frac{j\omega\mu(\omega)}{\sigma_{\mathrm{eff}}}} = \frac{j\omega\mu(\omega)}{\gamma} \\ \gamma =& \frac{j\omega\mu(\omega)}{Z_{\mathrm{w}}} = \sqrt{j\omega\mu_0} \cdot \sqrt{\sigma_{\mathrm{eff}}} \end{aligned} \tag{2.54}$$

Inserting $\sigma_{\mathrm{eff}} = \sigma(\omega) + j\omega\epsilon(\omega) = \sigma_{\mathrm{DC}}$ into Eq. (2.54) leads to the complex skin impedance. Throughout this thesis, magnetic permeability is $\mu(\omega) = \mu_0$.

$$Z_{\mathrm{skin}} = \sqrt{\frac{j\omega\mu_0}{\sigma_{\mathrm{DC}}}} = \frac{j\omega\mu_0}{\sqrt{\sigma_{\mathrm{DC}} j\omega\mu_0}} = \frac{j\omega\mu_0}{\frac{1+j}{\delta_{\mathrm{skin}}}} = \frac{j\omega\mu_0}{\gamma} = \frac{(1+j)}{\sigma_{\mathrm{b}}\delta_{\mathrm{skin}}} \tag{2.55}$$

Comparing Eq. (2.54) and Eq. (2.55), we identify the term $\frac{(1+j)}{\delta_{\mathrm{skin}}}$ as the propagation coefficient γ within the buffer layer.

Applying Drude's dispersion model to Dicken's expressions of Eq. (2.51, 2.52) is possible if the DC buffer layer conductivity $\sigma_{\mathrm{DC}} = \sigma_{\mathrm{b}}$ is replaced by its effective, frequency dependent value (Eq. (2.56)).

$$\sigma_{\mathrm{eff}} = \sigma(\omega) + j\omega\epsilon(\omega) = \sigma_{\mathrm{b}} \left(\frac{1}{1 + j(\omega/\omega_{\mathrm{s}})} + j\omega/\omega_{\mathrm{d}} \right) \tag{2.56}$$

In addition, the term $(1+j)/\delta_{\text{skin}}$ in Eq. (2.52) is replaced by the propagation coefficient from Eq. (2.54).

$$\gamma = \sqrt{j\omega\mu_0} \cdot \sqrt{\sigma_{\text{eff}}} = \sqrt{j\omega\mu_0} \cdot \left(\frac{1}{1 + j(\omega/\omega_{\text{s}})} + j\omega/\omega_{\text{d}} \right)^{1/2} \tag{2.57}$$

This leads to a high frequency version of Dickens' formulas [27–30].

$$\begin{aligned} Z_{\text{spr}} &= \frac{\operatorname{atan}\left(\frac{2b}{a}\right)}{\pi\sigma_{\text{b}} a} \left(\frac{1}{1 + j(\omega/\omega_{\text{s}})} + j\omega/\omega_{\text{d}} \right)^{-1} \\ Z_{\text{skin}} &= \frac{\ln\left(\frac{2b}{a}\right)}{2\pi} \left(\frac{j\omega\mu_0}{\sigma_{\text{b}}} \right)^{1/2} \left(\frac{1}{1 + j(\omega/\omega_{\text{s}})} + j\omega/\omega_{\text{d}} \right)^{-1/2} \end{aligned} \tag{2.58}$$

As already mentioned, calculated effective permittivity or effective conductivity values are readily included within 3D EM simulations and hence arbitrarily shaped three-dimensional geometries can be considered. Commercial fullwave solvers do also offer a variety of two-dimensional boundary conditions,[24] to include the influence of dispersive media without the necessity of 3D mesh grids. Anyway, in case of commercially available Schottky diodes the required process and material data are generally not available. In the author's opinion, using simple models should be preferred over assuming complicated but erroneous models.

Exemplary results of the volume current density vector $\mathbf{J}_{\text{vol}}$ at $f = 85$ GHz inside the n^+ GaAs buffer layer are shown in Fig. 2.13. Results on the left side show how the current density extends into the buffer layer, whereas the results on the right side visualize the concentration of current density directly below the anode metal.

Ohmic Contacts The ohmic contact resistances R_{ohmic} from n^+ buffer layer to cathode metal are small compared to the other equivalent

[24] Ansys High Frequency Structure Simulator (HFSS™) offers standard impedance boundary (IB), layered impedance boundary (LIB) and finite conductivity boundary (FCB).

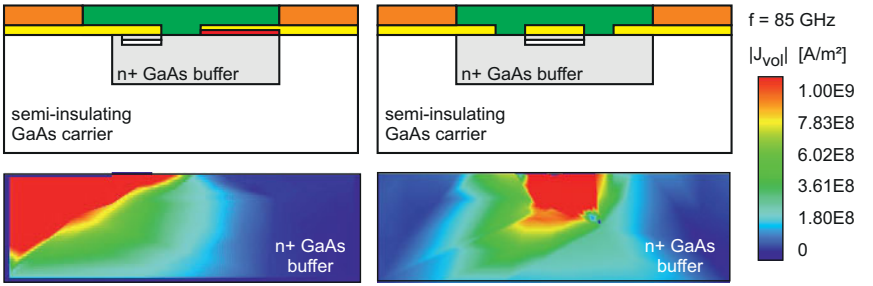

Figure 2.13: Simulated volume current density vector $\mathbf{J}_{\mathrm{vol}}$ at $f = 85$ GHz inside the n^+ GaAs buffer layer. Cross-sectional view in parallel to (left) and perpendicular to (right) to the direction of wave propagation.

circuit elements in Fig. 2.9. In general, ohmic contacts between metal and semiconductor are either realized by choosing an appropriate metal with work function $q_{\mathrm{e}}\Phi_{\mathrm{M}}$ lower than the semiconductor's work function $\Phi_{\mathrm{s}} = \Phi_{\chi} - V_{\mathrm{n}}$, resulting in negative built-in potential $\Phi_{\mathrm{bi}} < 0$. Then electrons emit from metal to semiconductor and vice versa without a potential barrier (left side of Fig. 2.14).

$$q_{\mathrm{e}}\Phi_{\mathrm{bi}} < 0 \quad q_{\mathrm{e}}\Phi_{\mathrm{m}} < q_{\mathrm{e}}\left(\Phi_{\chi} + V_{\mathrm{n}}\right) \tag{2.59}$$

Another way to realize ohmic contacts is very high doping (n^{++}) of the semiconductor. According to Eq. (2.19), the thickness of the depletion width is indirect proportional to the square root of doping density.

$$t_{\mathrm{d}} \sim \sqrt{1/N_{\mathrm{D}}} \tag{2.60}$$

At very high doping, field emission (electron tunneling) becomes the dominant current mechanism through the thin barrier (right side of Fig. 2.14).

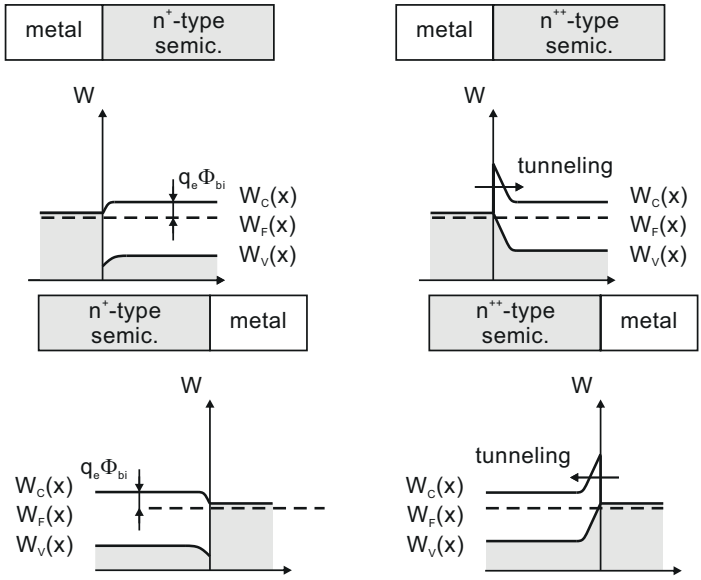

Figure 2.14: Energy band diagrams of ohmic contacts between metal and n-type semiconductor material. On the left side, the metal work function is lower than the semiconductor's work function, and on the right side, the ohmic contact is realized by field emission.

Details on ohmic contacts from a technological point of view can be found in [16, 31]. The ohmic contact resistance R_{ohmic} depends on the effective ohmic surface area S_{ohmic} and the specific ohmic contact resistance $(\ell_{\text{ohmic}}/\sigma_{\text{ohmic}})$, which is in the order of 10^{-10} Ωm^2 [32].

$$R_{\text{ohmic}} = \left(\frac{\ell_{\text{ohmic}}}{\sigma_{\text{ohmic}}}\right) \frac{1}{S_{\text{ohmic}}} \tag{2.61}$$

In case of $S_{\text{ohmic}} = 100/200/400/600$ µm^2, the resulting ohmic resistance values are $R_{\text{ohmic}} = 10/2.5/0.63/0.3$ mΩ.
Hence, it is $R_{\text{ohmic}} \ll |Z_{\text{spr}}|, |Z_{\text{skin}}|, |Z_{\text{epi}}|$ and R_{ohmic} is negligible.

Epilayer Impedance and Buffer Layer Impedance Calculations
Based on the derived analytical equations for frequency dependent epilayer impedance Z_{epi} (Eq. (2.49)) and buffer layer impedance Z_{buffer} (Eq. (2.58)), calculations are carried out at room temperature $T = 300$ K. The effective electron mass is assumed to be $m^{\star} = m_{\mathrm{e}} \cdot 0.067$ after [10]. The electron mobility $\mu_{\mathrm{e}}(N_D, T)$ is calculated from Eq. (2.32) and the GaAs semiconductor relative permittivity value is $\epsilon_{\mathrm{r}} = 12.9$.

Epilayer parameters:

- epilayer thickness $t_{\mathrm{epi}} = 0.1$ µm,
- worst case approximation of undepleted epilayer thickness $t_{\mathrm{u}} = t_{\mathrm{epi}} - t_{\mathrm{d}}(v_{\mathrm{j}}) \approx t_{\mathrm{epi}}$,
- doping concentration $N_{\mathrm{Depi}} = 2 \cdot 10^{23}$ m^{-3},
- $\mu_{\mathrm{e}}(N_{\mathrm{Depi}}, 300\ \mathrm{K}) = 0.3914\ \frac{\mathrm{m}}{\mathrm{Vs}}$,
- maximum drift velocity $v_{\mathrm{dmax}} \approx 2 \cdot 10^5 \frac{\mathrm{m}}{\mathrm{s}}$,
- anode width AW = 5 µm, anode length AL = 1 µm
  $\rightarrow$ effective anode diameter $a \approx 2.5$ µm,

With the above epilayer parameters, the DC conductivity value becomes $\sigma_{\mathrm{DC}} = \sigma_{\mathrm{epi}} = 1.2542 \cdot 10^4$ S/m, and the effective scattering frequency, dielectric relaxation frequency and plasma frequency are $\omega_{\mathrm{seff}}/(2\,\pi) = 1.39$ THz, $\omega_{\mathrm{d}}/(2\,\pi) = 17.48$ THz and $\omega_{\mathrm{p}}/(2\,\pi) = 4.92$ THz.

Buffer layer parameters:

- buffer layer thickness $t_{\mathrm{b}} \gg b$,
- doping concentration $N_{\mathrm{Db}} = 5 \cdot 10^{24}$ m^{-3},
- $\mu_{\mathrm{e}}(N_{\mathrm{Db}}, 300\ \mathrm{K}) = 0.1826\ \frac{\mathrm{m}}{\mathrm{Vs}}$,
- buffer width BW, buffer length BL,
- effective buffer radius $b \approx 250$ µm,

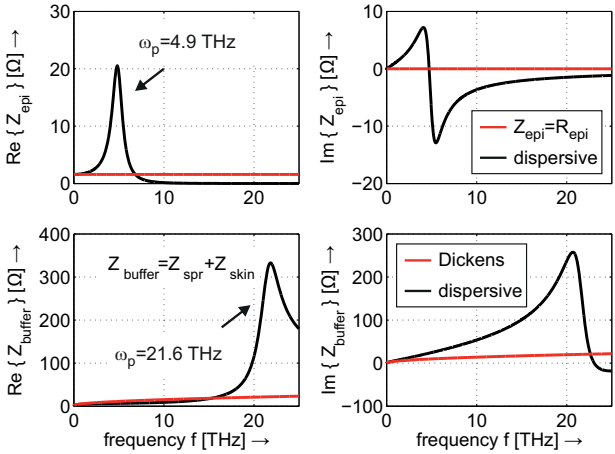

Figure 2.15: Calculated real and imaginary parts of epilayer impedance (top) Z_{epi} and buffer impedance (bottom) Z_{buffer} versus frequency.

With the above buffer layer parameters, the DC conductivity value becomes $\sigma_{\mathrm{DC}} = \sigma_{\mathrm{b}} = 1.4627 \cdot 10^5$ S/m, and the scattering frequency, dielectric relaxation frequency and plasma frequency are $\omega_{\mathrm{s}}/(2\,\pi) = 2.28$ THz, $\omega_{\mathrm{d}}/(2\,\pi) = 203.82$ THz and $\omega_{\mathrm{p}}/(2\,\pi) = 21.60$ THz.

Fig. 2.15 compares calculated real and imaginary parts of epilayer impedance (top) Z_{epi} and buffer impedance (bottom) Z_{buffer} versus frequency. Differences between the conventional solutions (red) and the high frequency ones (black) are significant only if frequencies are in the order of the plasma frequencies. The thin epitaxial layer has much lower plasma frequency than the buffer layer.

Fig. 2.16 contains the same data but illustrates the frequency range DC to 400 GHz only. Obviously, up to 400 GHz, there is no need to utilize the extended models. It further shows, the real part of Z_{buffer} varies between its static value and about 4 Ω at 400 GHz. According to Fig. 2.17, this frequency dependency is due to the skin effect, whereas the spreading impedance is almost a real value from DC to 400 GHz. The diode parameters roughly belong to the UMS

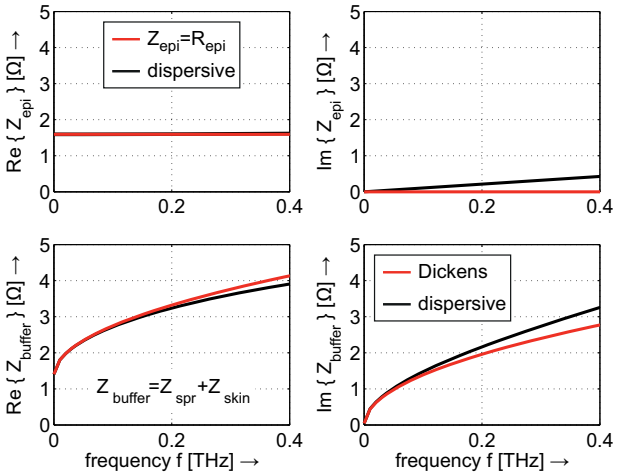

Figure 2.16: Calculated real and imaginary parts of epilayer impedance (top) Z_{epi} and buffer impedance (bottom) Z_{buffer} versus frequency. Maximum frequency $f = 400$ GHz.

DBES105a diode of section 2.6 and section 2.7, which is modelled with constant series resistance throughout this work.

The presented analysis allows for analytic calculation of the Schottky junction parameters (subsection 2.2.1) and the linear parts of the diode model (subsection 2.2.3). For the design of diode based frequency multipliers, mixers and detectors with commercial circuit simulators, the active part of the diode (Schottky junction) is best covered by the common Berkeley SPICE model DIODE [6, 33]. The linear diode parts are either described by the given equations or the effective material parameters are used in conjunction with 3D EM fullwave simulators, which is used to design the circuits of sections 2.5, 2.6, 2.7.

Detailed information about diode materials and geometry constitutes a precondition and are barely provided by the diode manufacturer. To offer accurate models without revealing business secrets, diode manufactures pay third party companies to build and sell black box models (e.g. Modelithics Inc. [34]).

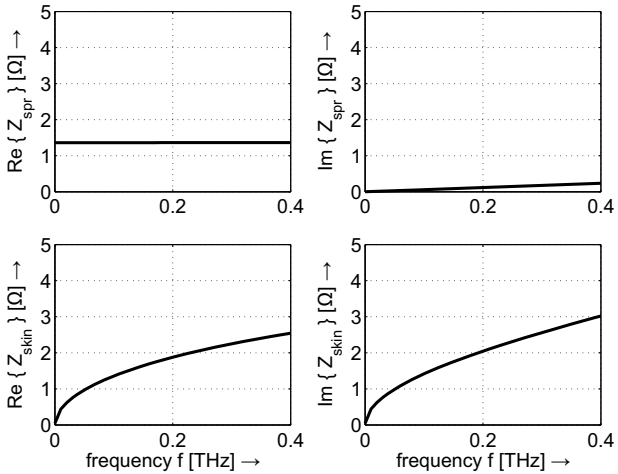

Figure 2.17: Calculated real and imaginary parts of spreading impedance (top) Z_{spr} and skin impedance (bottom) Z_{skin} versus frequency. Maximum frequency $f = 400$ GHz.

Semiconductor foundries offer design kits including diode models. These are often so called compact models. All parameters are given as a function of diode geometry and therefore the single compact model is valid for all the available diodes of the semiconductor process. Fig. 2.18 shows the equivalent circuit of the monolithic BES105 diode from the UMS buried epitaxial layer process (BES). Epilayer doping concentration and thickness (0.1 µm) are fixed by the BES process The diode has an anode length of AL = 1 µm, ideality factor $\eta = 1.204$ and built-in potential $\Phi_{\mathrm{bi}} = 0.97$ V. Anode widths AW are available in the range of 3 to 10 µm. The saturation current I_{S} and junction capacitance C_{j} are given as a function of the anode surface area $S_{\mathrm{j}} = \mathrm{AL} \cdot \mathrm{AW}$ in Eq. (2.62). Such compact models are also available for other semiconductor factories [35–37].

$$\begin{aligned} I_{\mathrm{S}} &= 7.04 \cdot 10^{-3} \frac{\mathrm{A}}{\mathrm{m}^2} \cdot S_{\mathrm{j}} = 7.04 \cdot 10^{-3} \frac{\mathrm{A}}{\mathrm{m}^2} \cdot 1\ \mu\mathrm{m} \cdot \mathrm{AW} \\ C_{\mathrm{j}}(\mathrm{fF}) &= C_{\mathrm{j0}} + C_{\mathrm{j1}}/(1 - v_{\mathrm{j}}/\Phi_{\mathrm{bi}})^M \qquad M = 1.82 \end{aligned} \tag{2.62}$$

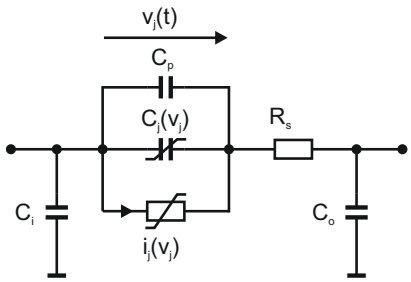

Figure 2.18: Underlying equivalent circuit of the monolithic UMS BES105 diode.

2.2.4 Market Overview

Table 2.1 summarizes characteristic parameters of several silicon and gallium arsenide Schottky diodes. It is average values, taken from the manufacturers datasheets. It includes the diode series resistance R_s, the junction capacitance at zero bias C_j0, saturation current I_s, ideality factor η and forward voltage at a certain DC current.

In addition, the cut-off frequency $f_\mathrm{c} = (2\pi R_\mathrm{s} C_\mathrm{T})^{-1}$ is calculated from R_s and the total capacitance $C_\mathrm{T} = C_\mathrm{j0} + C_\mathrm{parasitic}$. It serves as a rough figure of merit for the maximum operating frequency (compare explanations of [8] page 333 et seqq.). In case of antiparallel, series tee or quad diode configuration, the data corresponds to a single junction. Table 2.1 illustrates that commercial Schottky diodes are barely characterized by the manufacturers. For circuit design, individual parameter extractions from DC (current-voltage characteristics) and low frequency (junction capacitance) measurements are mandatory.

The reader should keep in mind, the diodes of Table 2.1 are either used within the author's circuit designs or constitute alternatives. Beside these, there are a lot more diodes available for millimeter-wave and sub-THz applications, like

- Technical Research Center (VTT) of Finland, www.vtt.fi,

- Advanced Compound Semiconductor Technologies (ACST) GmbH, spin-off from Technical University Darmstadt, Germany, www.acst.de,
- Jet Propulsion Laboratory, Pasadena, United States, www.jpl.nasa.gov,
- Hughes Research Laboratories (HRL), Malibu, United States, www.hrl.com,
- Teratech Components Ltd, spin-off from Science & Technology Facilities Council (STFC) Rutherford Appleton Laboratory (RAL), United Kingdom, www.teratechcomponents.com,
- Terahertz and Millimeter-Wave Laboratory at Chalmers University of Technology, Göteborg, Sweden, www.chalmers.se.

Table 2.1: Market Overview of Commercial Si and GaAs Schottky Diodes

diode	R_s [Ω]	C_{j0} [fF]	f_c [THz]	I_S [μA]	η	v_j [mV] at i_j [mA]	mat.	diode arch.	package	dim. [μm]
DBES105a ⋆	4	9.5	2.60	35E-9	1.2	750 at 1	GaAs	series tee	flipchip	530, 230, 100
after dicing ⋆ [38]	4	9.5	2.60	35E-9	2.2	750 at 1	GaAs	single	flipchip	140, 60, 30
VDI ZBD ⊛	19	15	0.34	11.9	1.21	70 at 0.1	GaAs	single	flipchip	600, 250, 100
VDI SD ⊛	4	n/a	1.11	n/a	n/a	475 at 1E-6	GaAs	single	flipchip	600, 250, 100
VDI AP ⊛	4	n/a	0.67	n/a	n/a	495 at 1E-6	GaAs	antiparallel	flipchip	600, 290, 100
VDI ST ⊛	4	n/a	1.17	n/a	n/a	500 at 1E-6	GaAs	series tee	flipchip	740,250,100
MGS801 †	7	50	0.45	(1.6 to 16)E-6	1.4	700 at 1	GaAs	antiparallel	flipchip	685, 275, 125
MGS801A †	5	75	0.42	(1.6 to 16)E-6	1.4	700 at 1	GaAs	antiparallel	flipchip	685, 285, 200
MGS904 †	7	60	0.38	(1.6 to 16)E-6	1.4	700 at 1	GaAs	quad ring	beamlead	450, 450, 90
MZBD-9161 †	50	30	0.11	12	1.2	$\Phi_{bi} = 230$	GaAs	single	beamlead	300, 300, 90
MSS30 PCR46 B47 †	10	100	0.16	(9.1 to 43)E-3	1.01	280 at 1	Si	crossed quad ring	beamlead	254, 254, 90
DC1346 •	8	10	0.66	n/a	1.28	720 at 2.5	GaAs	single	beamlead	800, 290, 50
HSCH-9161 ◇	20	35	0.17	12	1.2	$\Phi_{bi} = 230$	GaAs	single	beamlead	250, 250, 70
MA4E1317 ○	5.5	20	0.64	n/a	n/a	700 at 1	GaAs	single	flipchip	660, 330, 200
MA4E1310 ○	5.5	10	0.72	n/a	n/a	700 at 1	GaAs	single	flipchip	660, 330, 200
MA4E1318 ○	5.5	20	0.64	n/a	n/a	700 at 1	GaAs	antiparallel	flipchip	660, 330, 200
MA4E1319-1 ○	5.5	20	0.64	n/a	n/a	700 at 1	GaAs	series tee	flipchip	700, 475, 200
MA4E2160 ○	5.5	20	0.64	n/a	n/a	700 at 1	GaAs	antipar., uncon.	flipchip	370, 330 200
MS8150 ‡	3	45	0.82	200E-9	1.2	$\Phi_{bi} = 850$	GaAs	single	flipchip	660, 330, 140
MS8151 ‡	7	25	0.51	320E-9	1.01	$\Phi_{bi} = 850$	GaAs	single	flipchip	660, 330, 140
MS8250 ‡	3	45	0.82	320E-9	1.01	$\Phi_{bi} = 850$	GaAs	antiparallel	flipchip	660, 330, 140
MS8251 ‡	7	25	0.51	320E-9	1.01	$\Phi_{bi} = 850$	GaAs	antiparallel	flipchip	660, 330, 140
MS8350 ‡	3	45	0.82	320E-9	1.01	$\Phi_{bi} = 850$	GaAs	series tee	flipchip	710, 480, 140
MS8351 ‡	7	25	0.51	320E-9	1.01	$\Phi_{bi} = 850$	GaAs	series tee	flipchip	710, 480, 140
GC9901-QR1 ‡	20	100	0.08	n/a	n/a	340 at 1	Si	quad ring	beamlead	470, 470, 40
DMK2790 ∗	7	35	0.41	n/a	n/a	700 at 1	GaAs	single	flipchip	660, 330, 100
DMK2308 ∗	7	35	0.41	n/a	n/a	700 at 1	GaAs	antiparallel	flipchip	660, 330, 100

⋆ United Monolithic Semiconductors (UMS), www.ums-gaas.com, ⊛ Virginia Diodes Inc. (VDI), www.vadiodes.com, † Aeroflex Metelics, www.aeroflex.com,
• Linwave Technology Ltd., www.linwave.co.uk, ◇ Agilent Technologies, www.home.agilent.com, ○ M/A-COM Technology Solutions, www.macom.com
‡ Microsemi Corp., www.microsemi.com, ∗ Skyworks Solutions Inc., www.skyworksinc.com

2.3 Single Tone Large Signal (LS) Analysis

Single tone large signal analysis is required to analyze frequency multiplier circuits and is the basis of large signal / small signal (LSSS) mixer analysis in subsection 4.2.1. The latter assumes small signal RF and IF stimulus.

Following the design procedure of section 2.4, all linear circuit parts (embedding impedances) are covered by linear multiport scattering parameters from 3D EM simulation. Preferably, these do also include the linear parts of the diode models and are shown on the left side of Fig. 2.19.

Nonlinear models of the N Schottky junctions exist as SPICE models (right side of Fig. 2.19). This configuration is used to derive the

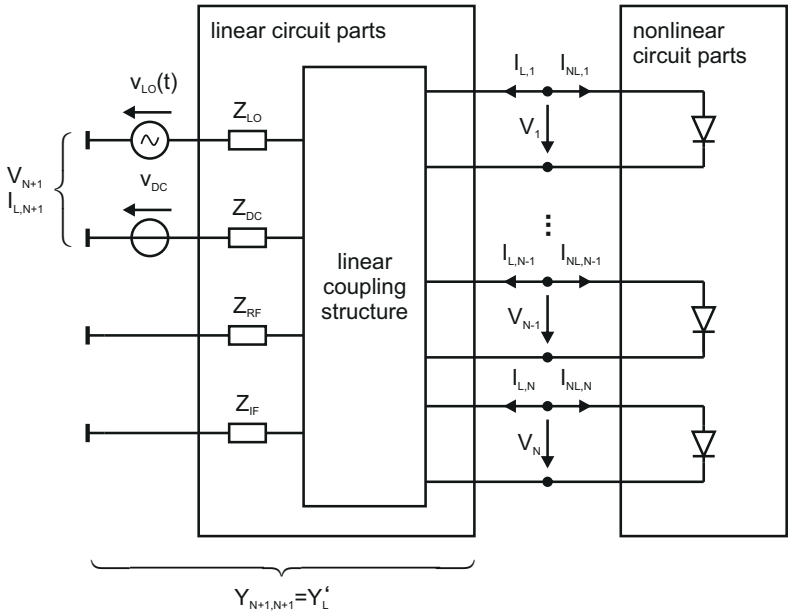

Figure 2.19: Arbitrary equivalent circuit of frequency multiplier with separated linear and nonlinear circuit parts.

harmonic balance equation in the following. Commercially available circuit simulators like Agilent ADS, Ansys Designer and many others[25] provide single and multi tone harmonic balance simulation, which is in addition easily combinable with many predefined equivalent models of commonly occurring devices.

A single large signal local oscillator voltage component $v_{\mathrm{LO}}(t) = \hat{v}_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \varphi_{\mathrm{LO}})$ and DC voltage component V_{DC} are applied and lead to a countably infinite number of voltage and current harmonics at each of the N nonlinear ports in Fig. 2.19. Up to H harmonics are considered in the following. A complex double sided Fourier series representation of such a large signal $v_{\mathrm{LS}}(t)$ including DC component is given by Eq. (2.63). Hence, two complex exponential functions $V_{\mathrm{LO}\,h} \cdot e^{hj\omega_{\mathrm{LO}}t}$ and $V_{\mathrm{LO}\,-h} \cdot e^{-hj\omega_{\mathrm{LO}}t}$ at each nonlinear port and harmonic number are required.

$$v_{\mathrm{LS}}(t) = V_{\mathrm{DC}} + \sum_{h=-H}^{h=+H} V_{\mathrm{LO}\,h} \cdot e^{hj\omega_{\mathrm{LO}}t} \tag{2.63}$$

Due to $v_{\mathrm{LS}}(t) \in \mathbb{R}$, $V_{\mathrm{LO}\,h} = V^{\star}_{\mathrm{LO}\,-h}$ holds true, and therefore only $(H+1)$ components $(h = 0 \ldots H)$ are enough for data processing (positive frequencies only).

$$v_{\mathrm{LS}}(t) \circ\!\!-\!\!\bullet\, V_{\mathrm{LO}\,h} \cdot e^{h\omega_{\mathrm{LO}}t} \quad h = 0 \ldots H \tag{2.64}$$

The reader should keep in mind, the linear coupling structure in Fig. 2.19 provides embedding impedances at all $(H+1)$ frequencies.

Linear Circuit Part According to Fig. 2.19 there are N $(n = 1 \ldots N)$ ports, at which the linear and nonlinear circuit parts interact. At each port, linear $\mathbf{I}_{\mathrm{L}\,n}$ and nonlinear $\mathbf{I}_{\mathrm{NL}\,n}$ current column vectors with $(H+1)$ rows are introduced (Eq. (2.65)). As well as a voltage column vector $\mathbf{V}_n$.

[25] Cadence SpectreRF, Synopsis Hspice, AWR Microwave Office.

$$\begin{aligned} \mathbf{I}_{\mathrm{NL}\,n} &= [I_{\mathrm{NL}\,n,0}, \ldots I_{\mathrm{NL}\,n,H}]^{\mathrm{T}} \quad \mathbf{I}_{\mathrm{L}\,n} = [I_{\mathrm{L}\,n,0}, \ldots I_{\mathrm{L}\,n,H}]^{\mathrm{T}} \\ \mathbf{V}_n &= [V_{n,0}, \ldots V_{n,H}]^{\mathrm{T}} \end{aligned} \tag{2.65}$$

An additional pair of linear voltage and current column vectors $\mathbf{V}_{\mathrm{L}N+1}, \mathbf{I}_{\mathrm{L}N+1}$ account for the DC and LO stimulus (Eq. (2.66)).

$$\begin{aligned} \mathbf{I}_{\mathrm{L}\,N+1} &= [I_{\mathrm{L}\,N+1,0}, \ldots I_{\mathrm{L}\,N+1,H}]^{\mathrm{T}} \\ \mathbf{V}_{N+1} &= [V_{N+1,0}, \ldots V_{N+1,H}]^{\mathrm{T}} \end{aligned} \tag{2.66}$$

These $(N+1)$ linear voltage and current vectors are components of the vectors $\mathbf{V}^{'}, \mathbf{I}_{\mathrm{L}}^{'}$, as shown in Eq. (2.67).

$$\mathbf{V}^{'} = \begin{bmatrix} \mathbf{V}_1 \\ \cdots \\ \mathbf{V}_N \\ \mathbf{V}_{N+1} \end{bmatrix} \quad \mathbf{I}_{\mathrm{L}}^{'} = \begin{bmatrix} \mathbf{I}_{\mathrm{L}\,1} \\ \cdots \\ \mathbf{I}_{\mathrm{L}\,N} \\ \mathbf{I}_{\mathrm{L}\,N+1} \end{bmatrix} \tag{2.67}$$

Due to Ohm'slaw, there is a $(N+1) \times (N+1)$ admittance matrix $\mathbf{Y}_{\mathrm{L}}^{'}$ transforming $\mathbf{V}^{'}$ into $\mathbf{I}_{\mathrm{L}}^{'}$.

$$\mathbf{I}_{\mathrm{L}}^{'} = \mathbf{Y}_{\mathrm{L}}^{'} \mathbf{V}^{'} \tag{2.68}$$

The submatrices $\mathbf{Y}_{\ell k}$ of $\mathbf{Y}_{\mathrm{L}}^{'}$ in Eq. (2.69) are diagonal matrices of size $(H+1) \times (H+1)$, that contain DC and harmonic transfer admittances between port ℓ and k. $\quad \ell, k \in \{1, \ldots, N+1\}$.

$$\begin{bmatrix} \mathbf{I}_{L,1} \\ \cdots \\ \mathbf{I}_{L,N} \\ \mathbf{I}_{L,N+1} \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{Y}_{1,1} & \cdots & \mathbf{Y}_{1,N+1} \\ \cdots & \cdots & \cdots \\ \mathbf{Y}_{N,1} & \cdots & \mathbf{Y}_{N,N+1} \\ \mathbf{Y}_{N+1,1} & \cdots & \mathbf{Y}_{N+1,N+1} \end{bmatrix}}_{\mathbf{Y}_{\mathrm{L}}^{'}} \begin{bmatrix} \mathbf{V}_{L,1} \\ \cdots \\ \mathbf{V}_{L,N} \\ \mathbf{V}_{L,N+1} \end{bmatrix} \tag{2.69}$$

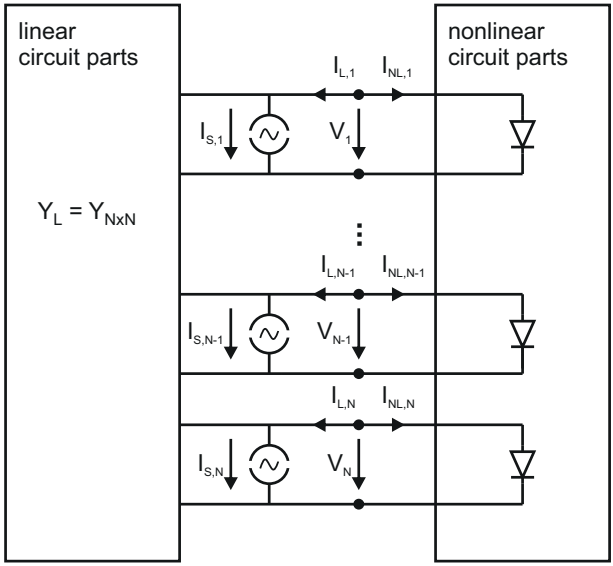

Figure 2.20: Arbitrary equivalent circuit of frequency multiplier with separated linear and nonlinear circuit parts, after transforming all sources into equivalent current sources.

Eq. (2.69) completely describes the linear circuit part of Fig. 2.19. In order to get a more compact description of the problem, the equivalent circuit is modified. The original sources of Fig. 2.19 are transformed into N current sources $\mathbf{I}_\mathrm{s}$ at the junctions between linear and nonlinear circuit parts, as shown in Fig. 2.20. The last column of $\mathbf{Y}_\mathrm{L}^{'}$ transforms the voltage stimulus $\mathbf{V}_{N+1}$ of Eq. (2.66) into $\mathbf{I}_\mathrm{s}$.

$$\mathbf{I}_\mathrm{s} = \begin{bmatrix} \mathbf{I}_{s,1} \\ \dots \\ \mathbf{I}_{s,N} \end{bmatrix} \qquad \mathbf{I}_\mathrm{s} = \begin{bmatrix} \mathbf{Y}_{1,N+1} \\ \dots \\ \mathbf{Y}_{N,N+1} \end{bmatrix} \Big[\mathbf{V}_{N+1} \Big] \tag{2.70}$$

The $(N \times N)$ admittance matrix $\mathbf{Y}_\mathrm{L}$ consists of the first N rows and N columns of $\mathbf{Y}_\mathrm{L}^{'}$. The column vectors $\mathbf{I}_\mathrm{L}, \mathbf{V}$ equal $\mathbf{I}_\mathrm{L}^{'}, \mathbf{V}^{'}$ without the

last row. The latter is considered by the current sources $\mathbf{I}_\mathrm{s}$. Then the linear circuit part of Fig. 2.20 is entirely covered by Eq. (2.71), which is the description of the Norton[26] equivalent circuit in a multiport, multi frequency scenario.

$$\mathbf{I}_\mathrm{L} = \mathbf{I}_\mathrm{s} + \mathbf{Y}_\mathrm{L}\mathbf{V} \tag{2.71}$$

Nonlinear Circuit Part Whereas the linear circuit part is discussed in the frequency domain, time domain analysis is preferred for the nonlinear circuit part. The charge per unit surface area as a function of Schottky junction voltage $Q_j/S_j\,(v_j)$ and the corresponding nonlinear displacement current $i_C(v_j, t)$ are derived in section 2.2, compare Eq. (2.20) and Eq. (2.24), respectively. As well as the nonlinear resistive Schottky diode junction current $i_j(v_j) = i_\mathrm{G}$ (Eq. (2.26)).

In the notation of this section, the nonlinear current vector $\mathbf{I}_\mathrm{NL}$ in Fig. 2.20, with its N components $\mathbf{I}_{\mathrm{NL}\,n},\ n \in \{1, \ldots, N\}$, is composed of a resistive $\mathbf{I}_\mathrm{G}$ and displacement current $\mathbf{I}_\mathrm{C}$.

$$\begin{aligned} \mathbf{I}_\mathrm{NL} = \mathbf{I}_\mathrm{G} + \mathbf{I}_\mathrm{C} &= [\mathbf{I}_{\mathrm{NL}\,1}, \ldots, \mathbf{I}_{\mathrm{NL}\,N}]^\mathrm{T} \\ \mathbf{I}_{\mathrm{NL}\,n} &= [I_{\mathrm{NL}\,n,0}, \ldots I_{\mathrm{NL}\,n,H}]^\mathrm{T} \end{aligned} \tag{2.72}$$

There are N resistive current time waveforms $i_{\mathrm{G}\,n}(t)$ and N charge time waveforms $Q_n(t)$, both dependent on all N components of the voltage vector $\mathbf{V}$. These consist of $(H + 1)$ spectral components in the frequency domain or a single voltage time waveform $\mathbf{V}_n = [V_{n,0}, \ldots V_{n,H}]^\mathrm{T} \bullet\!\!-\!\!\circ\, v_n(t)$.

$$\begin{aligned} i_{\mathrm{G}\,n}(t) &= i_{\mathrm{G}\,n}\,(t, v_1(t) \ldots v_N(t)) \\ Q_n(t) &= Q_n\,(t, v_1(t) \ldots v_N(t)) \end{aligned} \tag{2.73}$$

[26] Edward Lawry Norton (1898−1983), American engineer.

Fourier transform[27] maps the current waveform of the diode's conductance and charge time waveform of the diode's capacitor to the frequency domain. When choosing the number of harmonics as an integer power of $H = 2^p, p \in \mathbb{N}^+$, the number of time samples should be greater than $2H$ by an appropriate amount of time oversampling.

$$\begin{aligned} \{i_{\mathrm{G}\,1}(t) \dots i_{\mathrm{G}\,N}(t)\} &\circ\!\!-\!\!\bullet\, \mathbf{I}_{\mathrm{G}} = [\mathbf{I}_{\mathrm{G}\,1}, \dots, \mathbf{I}_{\mathrm{G}\,N}]^{\mathrm{T}} \\ \{Q_1(t) \dots Q_N(t)\} &\circ\!\!-\!\!\bullet\, \mathbf{Q} = [\mathbf{Q}_1, \dots, \mathbf{Q}_N]^{\mathrm{T}} \end{aligned} \tag{2.74}$$

The resistive current vector $\mathbf{I}_{\mathrm{G}}$ is known from Eq. (2.74). Displacement currents are the time derivatives of charge time waveforms $\mathrm{d}Q_n(t)/\mathrm{d}t$, which become multiplications with $j\omega$ in the frequency domain.

$$i_{\mathrm{C}\,n}(t) = \frac{\mathrm{d}Q_n(t)}{\mathrm{d}t} \circ\!\!-\!\!\bullet\, \mathbf{I}_{\mathrm{C}\,n} = [0, j\omega_{LO}Q_{n,1}, \dots, jH\omega_{LO}Q_{n,H}]^{\mathrm{T}} \tag{2.75}$$

Hence, the displacement current vector $\mathbf{I}_{\mathrm{C}}$ is given by Eq. (2.76), where $\mathbf{\Omega}$ is a diagonal matrix containing all considered frequencies.

$$\begin{aligned} \mathbf{I}_{\mathrm{C}} &= [\mathbf{I}_{\mathrm{C}\,1}, \dots, \mathbf{I}_{\mathrm{C}\,N}]^{\mathrm{T}} = j\mathbf{\Omega}\mathbf{Q} \\ \mathbf{\Omega} &= \mathrm{diag}\,[0, \omega_{LO}, \dots, H \cdot \omega_{LO}] \end{aligned} \tag{2.76}$$

Harmonic Balance Equation Applying Kirchhoff's[28] law (Eq. (2.77)) at each of the N ports in Fig. 2.20 and inserting Eq. (2.71), Eq. (2.72), Eq. (2.76) leads to the harmonic balance equation in Eq. (2.78).

$$\mathbf{I}_{\mathrm{L}} + \mathbf{I}_{\mathrm{NL}} = \mathbf{0} \tag{2.77}$$

[27] In case of multi tone harmonic balance, mappings different from classical Fourier transform are required (FFT-like).

[28] Gustav Robert Kirchhoff (1824−1887), German physicist.

$$\mathbf{F}\left(\mathbf{V}\right) = \mathbf{I}_{\mathrm{s}} + \mathbf{Y}_{\mathrm{L}}\mathbf{V} + \mathbf{I}_{\mathrm{G}} + \underbrace{j\boldsymbol{\Omega}\mathbf{Q}}_{\mathbf{I}_C} \stackrel{!}{=} \mathbf{0} \tag{2.78}$$

Every set of voltages $\mathbf{V}$ with the current error vector $\mathbf{F}\left(\mathbf{V}\right) = 0$ is a solution of the nonlinear large signal problem. A similar formulation can be found on the basis of scattering parameters instead of admittance parameters.

Starting with an estimated initial solution $v_n(t)^{\#0} \circ\!\!-\!\!\bullet\, \mathbf{V}^{\#0}$ at iteration step $\#s = \#0$, the harmonic balance equation is solved by numerical iteration techniques. Although implementation and user interface are different, commercial circuit simulators predominantly implement Newton[29]-Raphson[30] method.

$$\mathbf{J} = \frac{\mathrm{d}\mathbf{F}\left(\mathbf{V}\right)}{\mathrm{d}\mathbf{V}} = \mathbf{Y}_{\mathrm{L}} + \frac{\partial \mathbf{I}_{\mathrm{G}}}{\partial \mathbf{V}} + j\boldsymbol{\Omega}\frac{\partial \mathbf{Q}}{\mathbf{V}} \tag{2.79}$$

The latter utilizes the Jacobian[31] matrix $\mathbf{J}$ of the current-error vector $\mathbf{F}\left(\mathbf{V}\right)$, shown in Eq. (2.79), to solve for $\Delta\mathbf{V}$ of Eq. (2.80).

$$\mathbf{F}(\mathbf{V}^{\#s}) - \underbrace{\frac{\mathrm{d}\mathbf{F}(\mathbf{V})}{\mathrm{d}\mathbf{V}}}_{\mathbf{J}}\Bigg|_{\mathbf{V}=\mathbf{V}^{\#s}} \Delta\mathbf{V} = 0 \tag{2.80}$$

$$\Delta\mathbf{V} = \left(\mathbf{V}^{\#s} - \mathbf{V}^{\#s+1}\right) \tag{2.81}$$

This allows for calculating the estimate of the next iteration step $\mathbf{V}^{\#s+1}$ entirely from known data of step $\#s$ (Eq. (2.82)).

$$\mathbf{V}^{\#s+1} = \mathbf{V}^{\#s} - \mathbf{J}^{-1}\mathbf{F}(\mathbf{V}^{\#s}) \tag{2.82}$$

The iterative process of solution finding stops if $|\mathbf{F}\left(\mathbf{V}\right)|$ reaches a user defined minimum.

[29] Sir Isaac Newton (1642−1727), English physicist and mathematician.
[30] Joseph Raphson (1648−1715), English mathematician.
[31] Carl Gustav Jacob Jacobi (1804−1851), German mathematician.

The commercial circuit solvers used throughout this work offer two different methods for solving the system of linear equations in Eq. (2.80).

- Direct solver: LU decomposition
- Krylov solver: GMRES

The first implements Lower Upper (LU) decomposition and requires more computation time and memory than the Krylov solver but is more robust. The Krylov[32] subspace method known as generalized minimal residual method (GMRES) [39] is more effective with respect to computational time and memory consumption but suffers from convergence problems. The author uses Krylov method as a default and direct solver in case of convergence or accuracy problems only.

2.4 Frequency Multiplier Design

2.4.1 Multiplier Architectures

The series and shunt mounted diodes with individual signal branches for every spectral component of Fig. 2.1 and Fig. 2.2 in section 2.1 constitute the most versatile equivalent circuit models, capable of modelling every mixer / frequency multiplier scenario.

Utilizing frequency dependent impedances $Z_\mathrm{e}(\omega)$ and admittances $Y_\mathrm{e}(\omega)$ allows for building single diode equivalent circuits, as shown in Fig. 2.21. Summarizing multiple diodes is possible even if they are different by simultaneously modifying the embedding network $Z_\mathrm{e}, Y_\mathrm{e}$.

Within the scope of this section it is assumed, the single tone large signal (LS) analysis from section 2.3 has been applied to find a steady state solution of the nonlinear problem. Hence, all large signals are known as a function of time and at interesting frequencies $2\pi f = \omega = 0, \ldots, h\omega, \ldots, H\omega$ and power levels. The solution depends on all embedding impedances, including the diode mounting structure, and the diode's characteristics. The time to frequency domain mapping of

[32] Aleksey Nikolaevich Krylov (1863−1945), Russian mathematician.

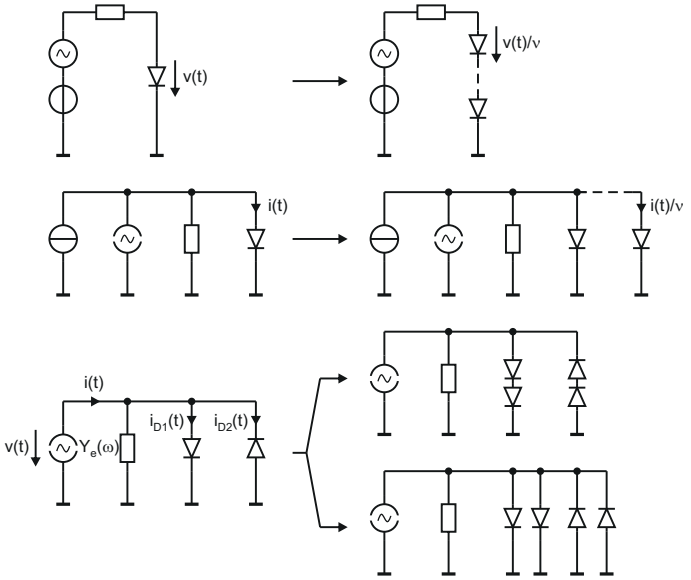

Figure 2.21: Equivalent circuits illustrating diode stacking in the form of series connection (top), parallel connection (middle) and series and parallel connection of an antiparallel diode pair (bottom).

this section is based on single sided complex Fourier series according to Eq. (2.83).

$$\begin{aligned} v(t) &\circ\!\!-\!\!\bullet\, V_h \quad h = 0 \ldots H \\ v(t) &= \mathrm{Re}\left\{ \sum_{h=0}^{\infty} V_h \cdot e^{jh\omega t} \right\} \end{aligned} \tag{2.83}$$

Diode Stacking To Influence Power Handling Capability In general, the diode's large signal impedance does not fit to the surrounding circuit at very low input power levels P_{in}. With increasing input power level the diode's impedance lowers until the best fit to the input and output embedding impedances is reached. At this input power level

$P_{\mathrm{in,opt}}$ the frequency multiplier operates with its maximum efficiency or minimum conversion loss[33].

One way, to influence the value of $P_{\mathrm{in,opt}}$ is DC biasing, which is unfavourable for many multiplier architectures and makes device performance dependent on the DC source parameters like temperature stability and noise.

A more promising solution is known as diode stacking (Fig. 2.21) and means replacing every Schottky junction by several (ν) identical junctions in series or parallel. The first enhances the diode's maximum voltage and impedance by factor ν and the latter extends the diode's maximum current and admittance by factor ν. In both cases the multiplier's power handling capability is increased by factor $\nu \rightarrow \nu \cdot P_{\mathrm{in,opt}}$. With respect to the maximum occurring frequency, the original and stacked configuration should both behave lumped and no additional phase changes must be introduced. This is normally guaranteed for MMIC designs. Fig. 2.22 shows the discrete Metelics MGS802 diode with two antiparallel Schottky junctions (left) and a close up view of a single junction (right). There are three junctions in parallel, whereas only the one in the middle is connected. In this case the anode widths AW and therefore surface junction areas differ and are intended to be used one at a time. But in the same way, identical junctions are stacked in MMIC designs.

In the way, Fig. 2.22 illustrates, diode manufacturers offer different diode versions in the same package, to allow for diode stacking in hybrid designs. From section 2.2, the approximative[34] relations in Eq. (2.84) are known.

$$\begin{array}{llll} I_{\mathrm{S}}, C_{\mathrm{j0}} & \sim S_{\mathrm{j}} & R_{\mathrm{s}} \approx R_{\mathrm{epi}} & \sim N_{\mathrm{Depi}} \\ R_{\mathrm{s}} \approx R_{\mathrm{epi}} & \sim S_{\mathrm{j}}^{-1} & C_{\mathrm{j0}} & \sim N_{\mathrm{Depi}}^{-1} \end{array} \tag{2.84}$$

[33] This holds true for every resistive frequency multiplier, although the occurring optimum condition does not necessarily equal the minimum achievable conversion loss.

[34] Saturation current depends on doping concentration and the actual metal-semiconductor combination as well, which is ignored in Eq. (2.84).

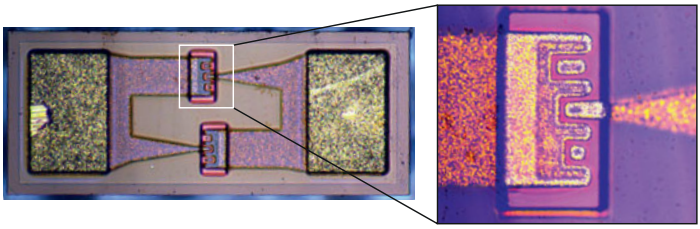

Figure 2.22: Photograph of discrete Aeroflex Metelics MGS802 diode with antiparallel configuration (left) and close up view of a single junction (right).

Hence, different anode surface areas (Fig. 2.22) lead to different but constant series resistance times maximum junction capacitance products $R_s C_{j0}$ = constant. In addition, for a given geometry S_j, increasing the doping concentration[35] allows for lowering R_s while increasing C_j0 and vice versa. This is basically the same as it is with parallel and series connection of identical Schottky junctions.

Stacking several discrete diodes (Fig. 2.5) in hybrid designs on the same carrier material does allow for changing the power handling capability as well, but leads to a different electromagnetic configuration and usually requires a complete redesign of the entire frequency multiplier.

Antiparallel Diodes The frequency multipliers in sections 2.5, 2.6, 2.7 make use of the antiparallel diode configuration to allow for balanced output circuitry in case of frequency doublers and to exhibit inherent filter effects in case of frequency triplers. The latter are discussed in the following, based on the simple equivalent circuit of Fig. 2.21. The time to frequency domain mapping of currents, voltages and admittances is shown in Eq. (2.85).

$$i(t), v(t), i_{\mathrm{D1}}(t), i_{\mathrm{D2}}(t), y_\mathrm{e}(t) \circ\!\!-\!\!\bullet\; I_h, V_h, I_{\mathrm{D1}\,h}, I_{\mathrm{D2}\,h}, Y_{\mathrm{e}\,h} \qquad h \in \{0, \ldots, H\} \tag{2.85}$$

[35] Higher doping concentration does also increase reverse breakdown voltage.

Considering the indication of current flow direction in Fig. 2.21, an expression of the total current time waveform is given by Eq. (2.86).

$$i(t) = \mathrm{Re}\left\{\sum_{h=0}^{H} \left(Y_{\mathrm{e}\,h} V_h + I_{\mathrm{D1}\,h} + I_{\mathrm{D2}\,h}\right) e^{jh\omega t}\right\} \tag{2.86}$$

Assuming identical diodes, the spectral current components $I_{\mathrm{D1}\,h}, I_{\mathrm{D2}\,h}$ of both diodes are equal in magnitude but π-phase shifted.

$$I_{\mathrm{D2}\,h} + I_{\mathrm{D1}\,h} e^{-jh\pi} = 0 \tag{2.87}$$

Hence, at fundamental frequency and odd order harmonics $(2h+1)$, both components are equal in magnitude and phase (Eq. (2.88)).

$$\begin{aligned} I_{\mathrm{D2}\,2h+1} &= I_{\mathrm{D1}\,2h+1} \underbrace{(-1)e^{-j(2h+1)\pi}}_{e^{-j\pi - j2h\pi - j\pi} = 1} = I_{\mathrm{D1}\,2h+1} \\ i_{\mathrm{odd}}(t) &= \mathrm{Re}\left\{\sum_{h=0}^{H} \left(Y_{\mathrm{e}\,2h+1} V_{2h+1} + 2I_{\mathrm{D1}\,2h+1}\right) e^{j(2h+1)\omega t}\right\} \end{aligned} \tag{2.88}$$

Whereas, at DC and even order harmonics $(2h)$ the diode current components cancel each other out, building a virtual short circuit at the common node (Eq. (2.89)). The even order currents circulate within the loop of the diodes and incorporate power loss, if there are resistive parts of the diode equivalent model.

$$\begin{aligned} I_{\mathrm{D2}\,2h} &= -I_{\mathrm{D1}\,2h} \quad V_{2h} = 0 \\ i_{\mathrm{even}}(t) &= \mathrm{Re}\left\{\sum_{h=0}^{H} \left(\underbrace{Y_{\mathrm{e}\,2h} V_{2h}}_{=0} + \underbrace{I_{\mathrm{D1}\,2h} - I_{\mathrm{D1}\,2h}}_{=0}\right) e^{j(2h)\omega t}\right\} = 0 \end{aligned} \tag{2.89}$$

Some textbooks (e.g. [7]) reduce multi diode frequency multipliers and mixers to single diode Thévenin or Norton equivalent circuits, as shown in Fig. 2.21, for comparison reasons. In the author's opinion, this is not a good idea. As explained before, the large signal quantities have to be determined by an iterative numerical method (section 2.3)

and the solution depends on all embedding impedances and input drive level. In this sense, an antiparallel diode configuration with its inherent filter effects constitutes a totally different case compared to series, shunt or bridge mounted diode configurations. Anyway, the statements of the preceding paragraph about diode stacking hold true for more complex multi diode circuits, as well, if stacking preserves the original diode configuration. The bottom of Fig. 2.21 shows series and parallel connection of an antiparallel diode pair.

Antiparallel Diodes With Single Ended Stimulus And Balanced Load The frequency doublers of section 2.6 and section 2.7 are based on the simple equivalent circuit of Fig. 2.23. The diodes are antiparallel with respect to the source and therefore the explanations of the preceding paragraph hold true. Fundamental and odd mode $(2h+1)$ grounding is established by the transformer circuit[36]. The currents i_{odd} of Eq. (2.88) flow through $Y_{\mathrm{e\,in}\,2h+1}$ but are isolated from $Z_{\mathrm{e\,out}}$. $Y_{\mathrm{e}\,2h+1}$ is chosen to equal zero for frequency doubling. The DC and even mode currents circulate within the diode loop and build a virtual short circuit at the common node but also produce load currents through $Z_{\mathrm{e\,out}}$ at the secondary coil of the transformer. Hence the circuit in Fig. 2.23 is suitable to build even order frequency multipliers with inherent isolation between source and load.

[36] The fundamental and odd mode currents constitute an even mode excitation to the primary coil of the transformer and are therefore short circuited in the transformer's center tap. The reader should keep in mind, several planar balun realizations have open circuit behaviour at even mode excitation instead. In such cases, circuit modifications are necessary to establish grounding.

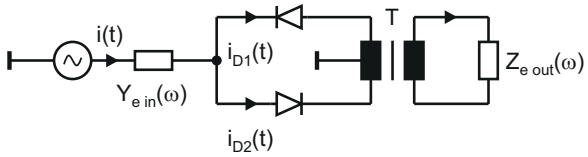

Figure 2.23: Simplified frequency doubler equivalent circuit with antiparallel diode configuration, single ended stimulus and balanced load.

2.4.2 Optimum Embedding Impedances

It is known from chapter 2.3 that all large signal quantities of any frequency multiplier circuit depend on all embedding impedances, the diode's characteristics and the input power level.

The manufactured frequency multipliers of sections 2.5, 2.6, 2.7 are planar realizations exclusively, which brings further restrictions into effect. The design flow is discussed in the next subsection.

In the following, general limitations of frequency doubler's and tripler's optimum performance with respect to the chosen embedding impedances are outlined. According to Fig. 2.24, a single diode Norton equivalent circuit of the frequency multiplier is discussed. A current source with an available power P_{in} (compare chapter 4) and shunt mounted, frequency dependent resistive $R(\omega)$ and reactive $X(\omega)$ elements forming the embedding network. In this context, the input, output and idle impedances are given by Eq. (2.90).

$$\begin{aligned} R_{\mathrm{in}}, \quad X_{\mathrm{in}} \quad &= R(1\cdot\omega), X(1\cdot\omega) \\ R_{\mathrm{out}}, \quad X_{\mathrm{out}} \quad &= R(d\cdot\omega), X(d\cdot\omega) \\ R_{\mathrm{idle}}, \quad X_{\mathrm{idle}} \quad &= R(h\cdot\omega), X(h\cdot\omega) \quad h \in \mathbb{N}_0 \setminus \{1, d\} \end{aligned} \tag{2.90}$$

The results in Fig. 2.24 are not restricted to an exemplary scenario, but are of general significance. The available source power is the

same in all cases. The minimum conversion loss $(P_{\mathrm{out}}/P_{\mathrm{in}})_{\mathrm{dB\,min}}$[37] or maximum real power across R_{out}, turns out, if the input and output impedances are tuned to their optimum values. These optimum values are different for every chosen series resistance and junction capacitance. All other impedances are either infinite (open idlers) or zero (short idlers). These procedures allow for determination of general limitations, more realistic than the limits of chapter 2.1, but still difficult to realize, especially in case of ultrawideband frequency multipliers.

The top of Fig. 2.24 shows an almost linear dependency between the minimum conversion loss and the diode's series resistance. Short idlers lead to higher conversion loss because of current flow through the diode's series resistance at the idle frequencies. The difference, compared to open idlers is about 2 dB in case of frequency doublers and about 5 dB in case of triplers. Both, frequency doubler's and tripler's minimum conversion loss, show little dependency of the diode's maximum junction capacitance if all idle impedances are short circuits. A slight increase is observed with open idlers. The bottom of Fig. 2.24 depicts the input and output impedances, necessary to achieve minimum conversion loss. The results of Fig. 2.24 correspond to a single frequency and are different at each frequency. There are planar design techniques, which allow for providing real source and load impedances to the diode, including mounting structure, over large bandwidth (compare Bode[38]-Fano[39] criterion). Whereas realization of defined reactive impedances $X_{\mathrm{in}}, X_{\mathrm{out}}$ is restricted to narrow operating bandwidth. R and X are shunt mounted components, therefore the higher the reactive components are, the more likely they can be ignored. Hence, ultrawideband realizations of frequency multipliers are more easily achieved if the idle impedances are set to zero. Although the minimum conversion loss values are higher than it is with open idlers.

[37] Output power is given by $P_{\mathrm{out}} = 1/2\,\mathrm{Re}\left\{R_{\mathrm{out}} \cdot I^2(d \cdot \omega)\right\}$ if complex phasors are related to peak amplitudes.

[38] Hendrik Wade Bode (1905−1982), American engineer.

[39] Robert Mario Fano (1917), Italian engineer.

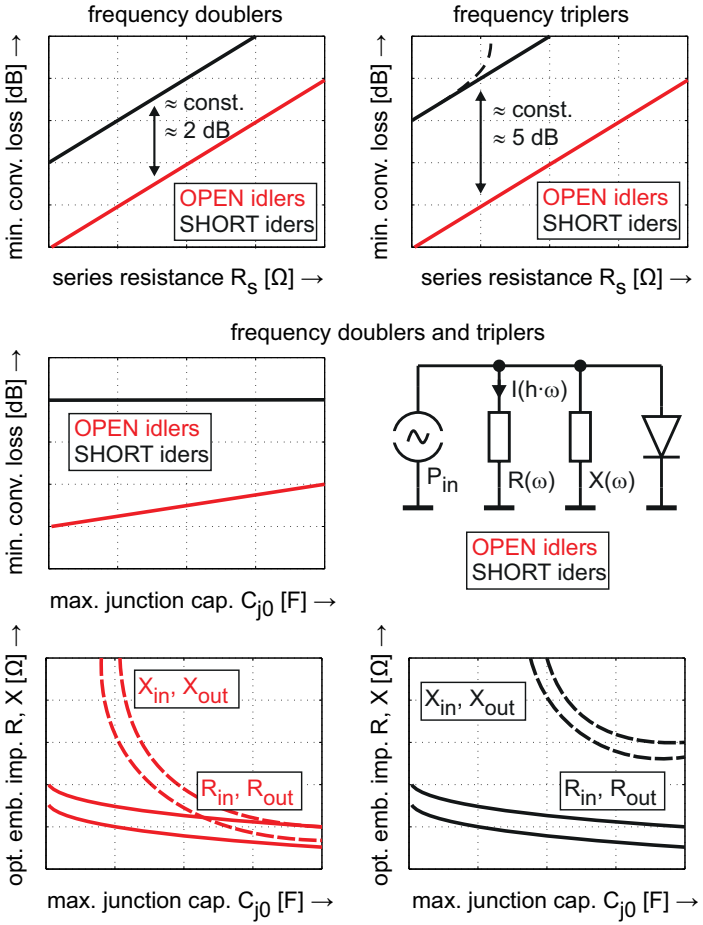

Figure 2.24: Performance dependency of frequency doublers and frequency triplers from open circuit (red) and short circuit embedding / idle impedances (black). Minimum conversion loss versus series resistance R_s (top), minimum conversion loss versus maximum junction capacitance C_j0 (middle) and optimum input $R_\mathrm{in}, X_\mathrm{in}$ and output embedding impedances $R_\mathrm{out}, X_\mathrm{out}$ versus C_j0 (bottom).

2.4.3 Design Flow

Fig. 2.25 illustrates the design flow of frequency multiplier synthesis and the correlation of several optimization objectives, which is mostly self-explaining. The following enumeration contains the most important requirements on the input and output circuitry in descending order.

1. Input: passband behaviour at 1^{st} harmonic and open / short circuit behaviour at desired output harmonic.
2. Output: passband at desired output harmonic and open / short circuit behaviour at 1^{st} harmonic.
3. Reflection phases from diodes to input / output circuitry below 180 ° to avoid destructive interference of 1^{st} and desired harmonic.
4. Find compromise between 1^{st} harmonic rejection and additional loss[40] of output filter.
5. Find compromise between input and output circuit symmetry (linear circuit part, not diode symmetry) and rejection of undesired harmonics.
6. Manipulate 4^{th} harmonic idle impedance in case of doublers and 5^{th} harmonic in case of triplers for minimum conversion loss (not possible for ultrawideband designs due to overlapping frequency ranges).
7. Tune other idle impedances.

Minimum conversion loss strongly depends on the operating frequency range and instantaneous bandwidth. For ultrawideband frequency doublers / triplers 10 dB / 15 dB conversion loss constitute excellent results. To achieve such values, the design must not violate

[40] Prediction of loss is best derived from thruline measurements and experiences, rather than simulations. The latter always underestimate real loss mechanisms.

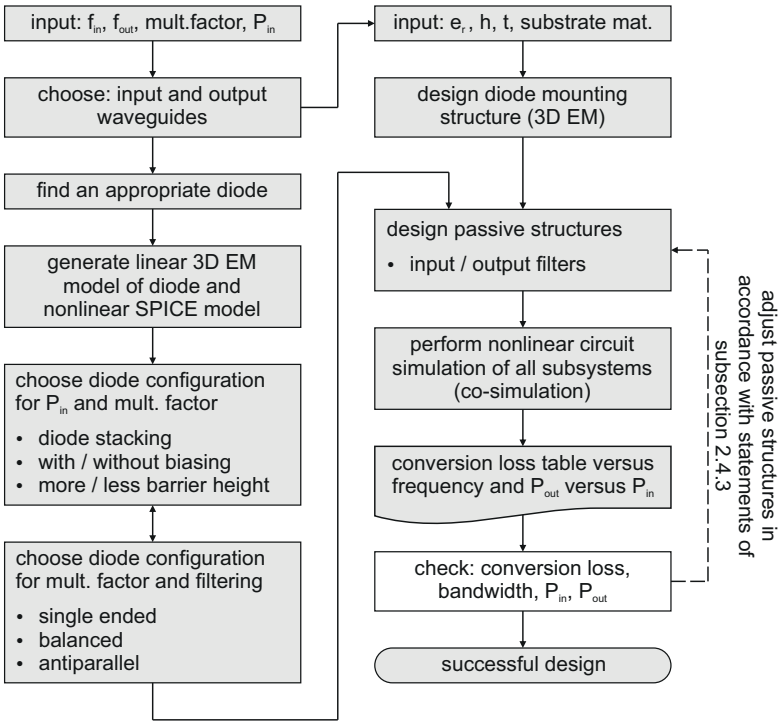

Figure 2.25: Flow chart illustrating the design flow of frequency multiplier synthesis.

one of the first three points in the above list. These requirements underly mutual influences and do also influence the idle impedances at undesired harmonics. These explanations together with facts of the preceding subsection make clear, optimizing conversion loss behaviour by defined tuning of single idle impedances is of importance for narrowband frequency multipliers only.

2.5 Octave Bandwidth Tripler for 20 to 40 GHz

Superheterodyne transceivers for synthetic automatic test systems require high frequency phase locked stimulus at the local oscillator mixer ports. Especially systems with high instantaneous signal bandwidth as shown in Fig. 4.34 of section 4.4 or Fig. 1.4 of chapter 1 make use of many different mixing cases. Fundamental, subharmonic, upper and lower sideband mixing is often utilized in a single module to ensure best spurious tone suppression at different input / output frequency ranges. This section presents a frequency tripler for 20 to 40 GHz, as it is required (LO) to downconvert signals below 20 GHz to several intermediate frequencies in lower sideband mixing configuration $\langle \mathrm{RF}, \mathrm{LO} \rangle = \langle -1, 1 \rangle$.

The presented tripler is an improved version of the author's earlier work [G2]. An equivalent circuit and photographs of the utilized antiparallel Schottky diodes from VDI are shown in Fig. 2.26. The basic circuit idea is from Albin, who reported a tripler design with unilateral finlines on fused silica substrate for Hewlett Packard source modules in 1988 [40]. The assembled diodes offer negligible deviations of both Schottky junctions. The parameters of a single junction are $I_\mathrm{S} = 157.5$ fA, $R_\mathrm{s} = 2.6\ \Omega$, $\eta = 1.175$ and $C_\mathrm{j0} = 0.07$ pF.

The tripler is manufactured on woven fiberglass reinforced, ceramic filled, PTFE based composite material AD600 $\epsilon_\mathrm{r} = 6.15$ from Arlon Micowave Materials [41]. Standard PCB processing is applied. Fig. 2.27 depicts a 3D model of the tripler for EM simulation. A transition from 1.85 mm coaxial connector to grounded coplanar waveguide (gCPW) is used at the circuit input and output. The fundamental signal in gCPW mode enters an 11^th order stepped impedance gCPW lowpass filter (LPF). Simulated scattering parameters of the LPF are given in Fig. 2.28. The first and last filter elements are shunt capacitances to ensure short circuit behaviour at stopband frequencies, as it is required for this circuit topology (Fig. 2.26). Fig. 2.29 illustrates the cross-sectional views of the low (C) and high (L) impedance gCPW, magnitude of the electric field strengths at 18 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_\mathrm{gCPW})$ of 50 Ω gCPW,

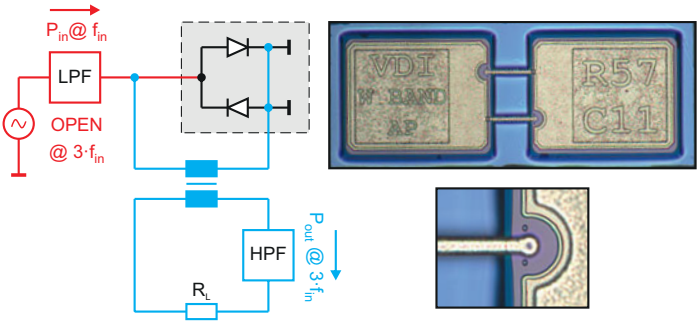

Figure 2.26: Equivalent circuit of the proposed 20 to 40 GHz frequency tripler and a photograph of Virginia Diodes Inc. (VDI) discrete anti-parallel Schottky diode with close up view of the anode finger. Diode dimensions are (250×600×100) µm^3.

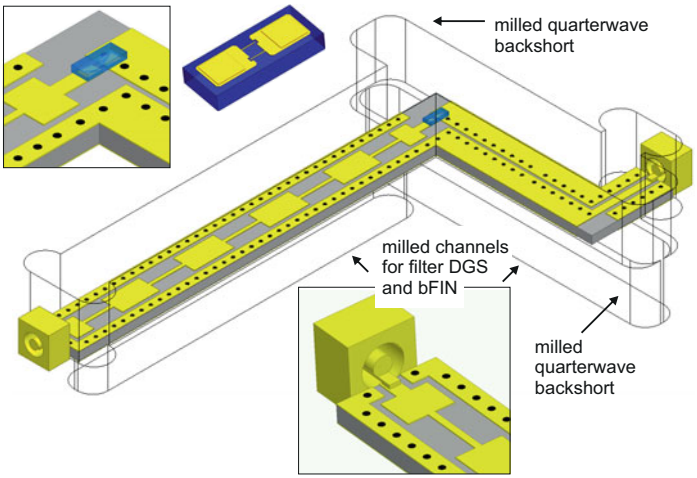

Figure 2.27: 3D model of the tripler for EM simulation and close up views of diode and transition to coaxial waveguide.

high and low gCPW versus frequency. Table 2.2 summarizes the filter parameters.

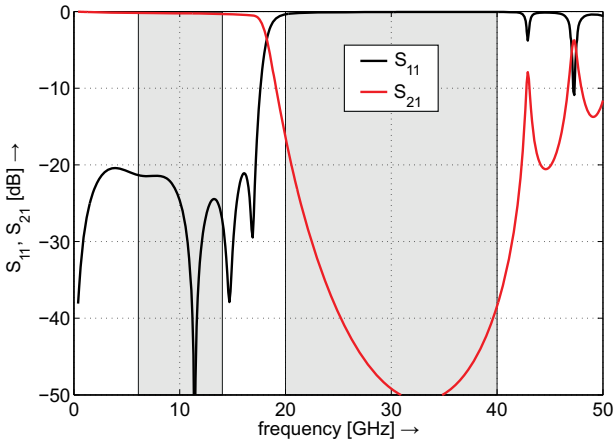

Figure 2.28: Simulated transmission (black) and reflection coefficients (red) of 11^{th} order stepped impedance gCPW lowpass filter.

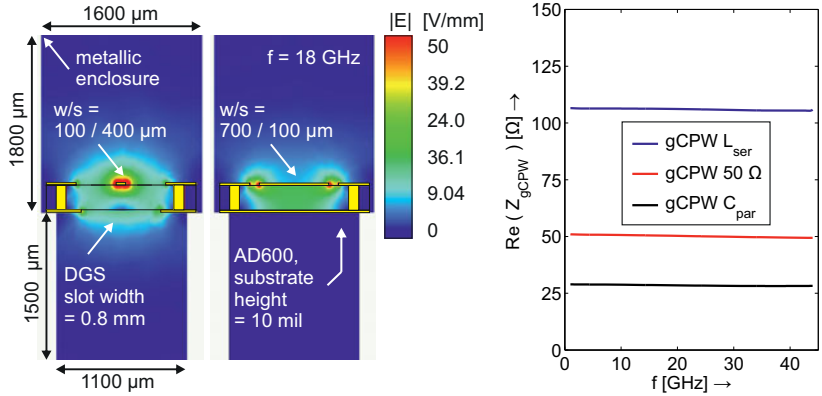

Figure 2.29: Cross-sectional views of the low (C) and high (L) impedance gCPW, magnitude of the electric field strengths at 18 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{gCPW}})$ of 50 Ω gCPW, high and low gCPW versus frequency. $\mathrm{Re}\,(Z_{\mathrm{gCPW-L}}) = 106.2\ \Omega, \mathrm{Re}\,(Z_{\mathrm{gCPW-C}}) = 28.5\ \Omega$ and the corresponding effective permittivities are $\epsilon_{\mathrm{reff-L}} = 3.00, \epsilon_{\mathrm{reff-C}} = 4.07$ at $f = 18$ GHz.

Table 2.2: 11^{th} order stepped impedance gCPW lowpass filter

filter elements	strip / slot widths [µm]	lengths [µm]	inductance and capacitance values at f_c
1 and 11	700/100	550	32.72 pH
2 and 10	100/400	935	220.6 fF
3 and 9	700/100	1223	72.77 pH
4 and 8	100/400	1129	266.4 fF
5 and 7	700/100	1307	77.76 pH
6	100/400	1156	272.8 fF

filter order $N = 11$, cut-off frequency $f_{c\,1\,\mathrm{dB}} = 17.5$ GHz,
$f_{c\,3\,\mathrm{dB}} = 18.1$ GHz, passband ripple $r_{\mathrm{dB}} = 0.01$ dB,
stopband rejection of 25 dB at $1.2 \times f_{c\,3\,\mathrm{dB}}$.

The antiparallel diodes generate two third harmonic signals propagating in bilateral finline (bFIN) mode. One of them is back reflected by the milled quarterwave backshort of Fig. 2.27. The design rule set of standard PCB processing allows for bFIN waveguides with $\mathrm{Re}\,(Z_{\mathrm{bFIN1}}) = 51.6\ \Omega$ at 20 GHz and $\mathrm{Re}\,(Z_{\mathrm{bFIN1}}) = 42.8\ \Omega$ at 40 GHz. Fig. 2.30 includes a cross-sectional view of the bFIN, magnitude of the electric field strengths at 30 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{bFIN}})$ of the first three hybrid modes versus frequency. Single mode operation from 20 to 40 GHz is achieved.

The length of the bFIN constitutes a tradeoff between fundamental signal rejection and third harmonic insertion loss. After the bFIN highpass filter, another transition to gCPW (Fig. 2.31) and 1.85 mm coaxial connector is utilized. Simulated scattering parameters of the transition from bFIN to gCPW are shown in Fig. 2.32. The fully assembled frequency tripler with its Au plated brass housing is depicted in Fig. 2.33.

The measured 3^{rd} harmonic output power levels P_{out} at the output frequencies $f_{\mathrm{out}} = 21.4,\ 25,\ 32,\ 40,\ 43$ GHz versus the fundamental

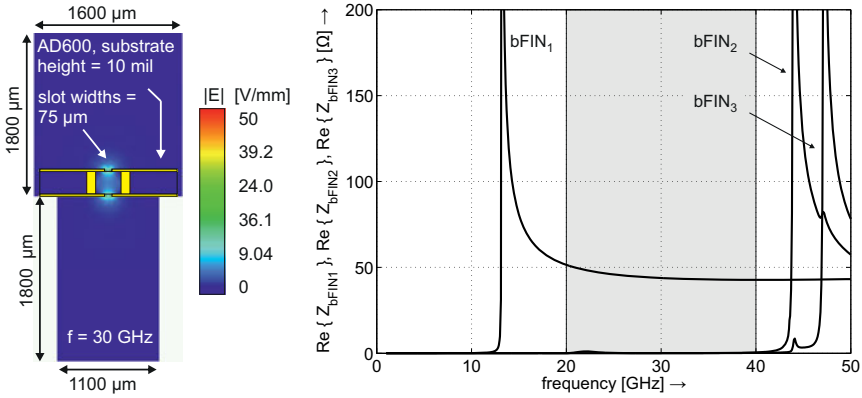

Figure 2.30: Cross-sectional view of the bilateral finline, magnitude of the electric field strengths at 30 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{bFIN}})$ of the first three hybrid modes versus frequency.

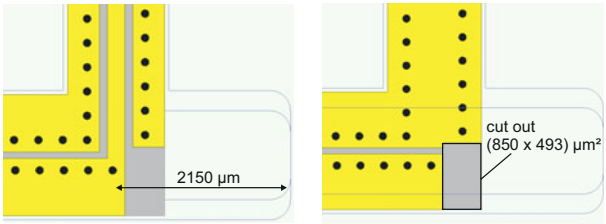

Figure 2.31: Top (left) and bottom (right) view of transition from gCPW to bilateral finline.

input power level P_{in} are given by Fig. 2.34. All measurement data from 21.4 to 40 GHz are within the gray shaded area. At center frequency a saturated output power level of -5 dBm is achieved.

Fig. 2.35 compares simulated and measured conversion loss values versus output frequency f_{out} at three input power levels $P_{\mathrm{in}} =$ 5.6, 7.6, 9.6 dBm. Results from co-simulation (section 2.4) are in reasonable agreement with measurement results. The measured conversion loss values are between 16 and 20 dB from 21 to 40 GHz. The frequency tripler is designed to substitute the MMIC tripler TGC1430G

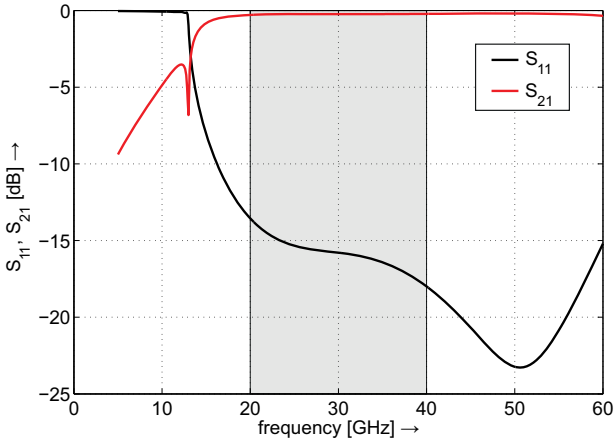

Figure 2.32: Simulated transmission (red) and reflection coefficients (black) of the transition from gCPW to bFIN, which is used for highpass filtering.

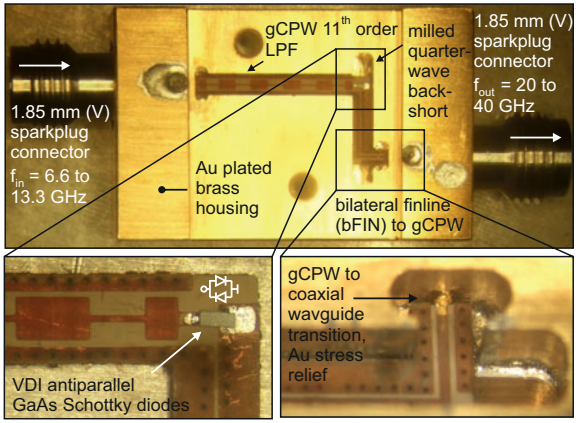

Figure 2.33: Photographs of the assembled frequency tripler with close up view of the diode mounting structure and transition from gCPW to coaxial connector.

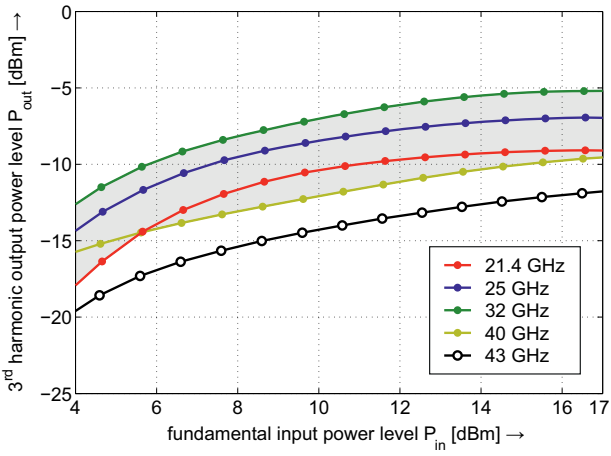

Figure 2.34: Measured 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 21.4,\ 25,\ 32,\ 40,\ 43$ GHz versus the fundamental input power level P_{in}. All measurement data from 21.4 to 40 GHz are within the gray shaded area.

from TriQuint Semiconductor [42]. Compared to TGC1430G (blue curve), the proposed tripler offers larger bandwidth with similar conversion efficiency. The reader should keep in mind, measurement results of the proposed tripler include insertion loss of the coaxial connectors and transitions to planar waveguide. Whereas the blue curve in Fig. 2.35 corresponds to bare die measurements.

Measured spectral output power levels up to the 5th harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 5.6$ dBm are shown in Fig. 2.36. Rejection of the even order harmonics is higher than 30 dB from 21 to 40 GHz. As a consequence of the antiparallel diode configuration, suppression of the 5th harmonic is quite poor. A filter bank of only two BPFs in cascade can fix this problem. The fundamental rejection is directly connected to the length of the bFIN waveguide. At the expense of conversion loss higher fundamental rejection is possible.

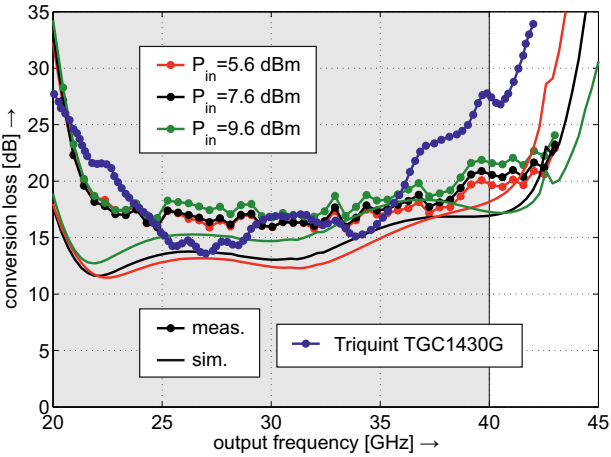

Figure 2.35: Simulated and measured conversion loss versus output frequency f_{out} at three input power levels $P_{\text{in}} = 5.6,\ 7.6,\ 9.6$ dBm. The blue curve belongs to the commercial MMIC tripler TGC1430G from TriQuint Semiconductor.

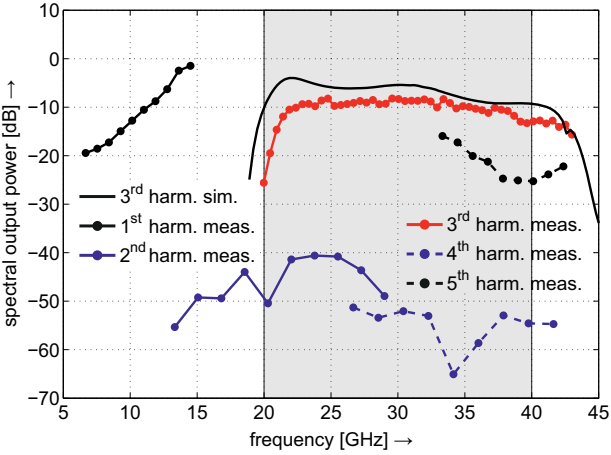

Figure 2.36: Measured spectral output power levels up to the 5$^{\text{th}}$ harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 5.6$ dBm. Compared to simulated 3$^{\text{rd}}$ harmonic output power levels (black, without markers).

2.6 Frequency Doublers and Triplers for 50/60 to 110 GHz

Although there is a persistent tendency to higher operating frequencies of direct signal generation concepts, frequency multipliers are still used to provide phase locked signal stimuli at millimeter-wave frequencies and beyond. Operation over preferably large bandwidths is especially required in system design of frequency extension modules for vector network analyzers (VNA), microwave signal generators and front end modules of semiconductor automatic testsystems (ATS). Varactor based multipliers have much better power efficiency, but they can hardly serve the bandwidth requirements (2.6). There is a constant output power level times output frequency range product ($P_{\text{out}} \cdot \Delta f_{\text{out}} = \text{const.}$) with varactor multipliers, which restricts the broadband varactor multipliers to rather low output power levels. Monolithic integrated circuit (MIC) technology is ideally suited to design active and passive varactor and varistor multipliers for the aforementioned fields of application [43–45], not least because of the opportunity to integrate the diode or transistor architecture into the optimization procedure of the multiplier design [46–49]. Another advantage is the integration of amplifier stages in cascade on the same die [50–52]. Nevertheless, hybrid designs offer advantages with respect to the achievable fundamental signal isolation, filter performance and manufacturing cost in case of low to medium quantities. The modules used in the envisaged fields of application have high complexity and great functionality. Therefore, multi-chip module realizations rather than fully MIC constructions are preferred. Ease of maintenance, module cost and thermal engineering reasons determine which component is best integrated as MIC, hollow waveguide component or hybrid planar device.

In the following, we focus on three planar resistive frequency triplers (#1, #2, #3, $f_{\text{out}} = [60, 110]$ GHz) and two frequency doublers (#4, #5, $f_{\text{out}} = [50, 110]$ GHz) based on commercially available gallium arsenide (GaAs) Schottky diodes and conventional thin-film processed

alumina (Al_2O_3) substrate with 5 µm Ni/Au metallization [I6, J2]. Synthesis is based on a co-simulation procedure between 3D electromagnetic field and nonlinear harmonic balance circuit simulations as explained in subsection 2.4.3.

If common substrate widths are used, restricted by dicing technology, 110 GHz constitutes almost the maximum operating frequency for planar designs on 5 mil Al_2O_3 substrates due to propagation of higher order modes. The reader should further keep in mind, plated-through vias establish diode ground connection. Hence, the mechanical length of this ground path equals the sum of substrate thickness and half of the via pad diameter. At higher frequencies, low permittivity substrates (e.g. fragile quartz SiO_2, BCB or PFTE) with thicknesses $h \leq 5$ mil have to be used (section 2.7). Innovative planar circuit designs are presented to overcome these restrictions. Different architectures are presented to account for the individual demands associated with multi-chip module designs.

Scalar and spectral measurement data over the focused output frequency ranges are presented. Conversion loss values around 18 dB from 60 to 95 GHz and below 22 dB from 60 to 110 GHz are achieved with frequency tripler #1. Frequency doubler #5 achieves conversion loss values below 15 dB from 50 to 89 GHz and below 22 dB from 50 to 110 GHz. A comprehensive comparison of the presented work with reported frequency multipliers is included (Table 2.6).

Schottky Junction Modelling and Co-Simulation Procedure The proposed multipliers are optimized for use with the United Monolithic Semiconductors (UMS) DBES105a diode, which is a discrete component with two Schottky junctions in series tee configuration from the UMS buried epitaxial layer (BES) process with anode finger dimensions of (5 µm × 1 µm). Each solder pad is equipped with two gold bumps ($\varnothing = 20$ µm). Fig. 5.14 depicts a 3D model for electromagnetic field (EM) simulation of the utilized diode. Within the proposed multiplier design, the junction geometry is small compared to the minimum wavelength $\lambda_{\min} = c_0/(\sqrt{\epsilon_{\text{reff}}} \cdot f_{\max})$, which allows for lumped port modelling of the junctions in 3D EM simulation.

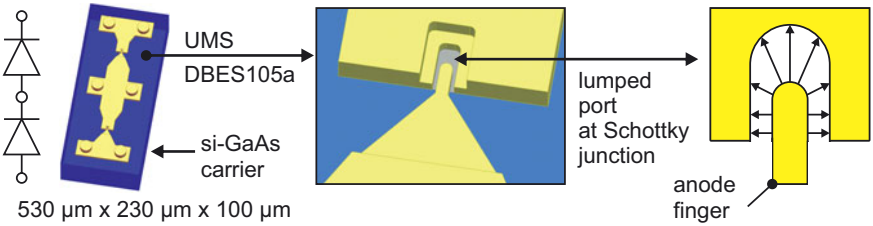

Figure 2.37: 3D EM model of the utilized commercial GaAs Schottky diode UMS DBES105a with close up view of lumped port Schottky junction modelling.

The multiplier synthesis is based on co-simulation between finite element 3D EM simulation in the frequency domain[41] and nonlinear harmonic balance circuit simulation[42]. As long as the chosen architectures allow for partitioning of the multiplier into a preferably high number of subsystems, which can be synthesized and optimized individually, the simulation time is significantly reduced. These subsystems are various required waveguide transitions, the input lowpass filter (LPF), the diode mounting structure including a 3D EM model of the diode and the output highpass filter (HPF). Accurate 3D modelling of the diode, including the semi-insulating GaAs carrier and the first metallization layer, allows for sufficient prediction of parasitic effects, such as pad to pad capacitance and harmonic generation due to asymmetries. Within the harmonic balance circuit simulator, the linear parts are connected with a rather simple circuit model of the Schottky junctions, Berkeley SPICE: DIODE, according to Fig. 2.38. The junction parameters are series resistance R_S, junction capacitance at zero bias C_{j0}, ideality factor η and saturation current I_S.

A more sophisticated junction modelling approach, e.g. [53], would be promising, but it requires disproportionate measurement effort or dimensions and material parameters of the Schottky junction that are difficult to obtain in case of proprietary diodes. With all

[41] Ansys, High Frequency Structure Simulator (HFSS™)
[42] Agilent, Advanced Design System (ADS™)

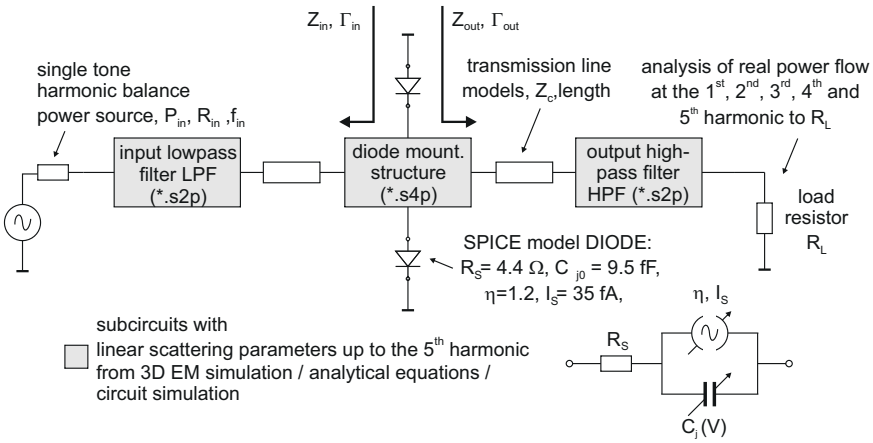

Figure 2.38: Block diagram of the harmonic balance schematic for frequency multiplier synthesis.

subsystems connected in a parameterized co-simulation, the multipliers conversion efficiency is optimized by tuning the embedding impedances $Z_{\mathrm{in}}(f)$, $Z_{\mathrm{out}}(f)$ at all involved harmonics [54]. The input lowpass filter in Fig. 2.38 provides resistive input impedance, which allows for ultrawideband operation, contrary to reactive matching with severe bandwidth limitations. To account for the strong near-field interaction of all subcircuits, it is necessary to perform a final simulation with all subsystems combined within the 3D EM simulation. Without the use of parallelization algorithms, such a 3D EM simulation takes less than two hours using an ordinary personal computer. The broadband frequency multipliers of this chapter [G2, I6, I7] are based on the outlined co-simulation approach. The same holds true for the triple balanced mixer of chapter 4 [I4] and the power detectors of chapter 5 [I8].

Waveguide Transitions The planar multipliers are intended to be used within highly integrated front end modules and are normally not directly connected to the module's output. Hence the multipliers

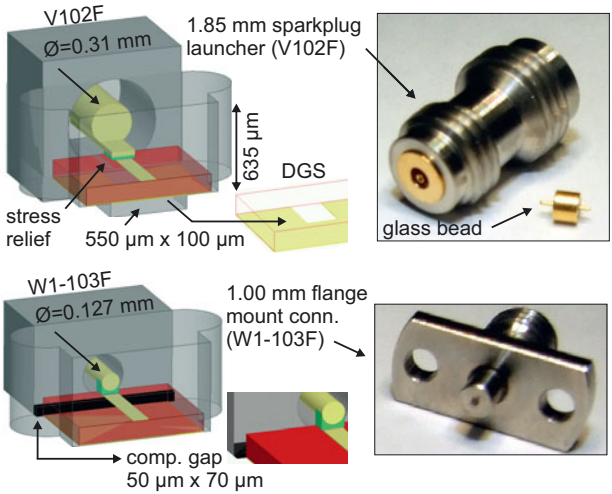

Figure 2.39: 3D EM models of transitions from 1.85 mm / 1.00 mm coaxial connectors to shielded microstrip line.

have to be connected to MICs or hollow waveguides or other planar substrates. Transitions to 1.85 mm and 1.00 mm coaxial waveguide are designed to ease measurement characterization. The proprietary coaxial connectors V102F and W1-103F from Anritsu GmbH and the corresponding transitions are shown in Fig. 2.39. The parasitics from both transitions can be modelled as shunt capacitances in equivalent circuits. Compensation in case of the 1.85 mm connector with stress relief is realized with a rectangular shaped defected ground structure (DGS). The equivalent shunt capacitance of the 1.00 mm connector is much smaller. A compensation gap of 50 µm width and 70 µm height is sufficient. The 3D EM models include the transitions from shielded microstrip line (MSL) to the first air-filled coaxial waveguide section, not the entire 1.85 mm and 1.00 mm connector. Fig. 2.39 further shows the dimensions of the milled channels that are chosen to avoid parasitic higher order modes like TE_{10} up to the maximum operating frequency.

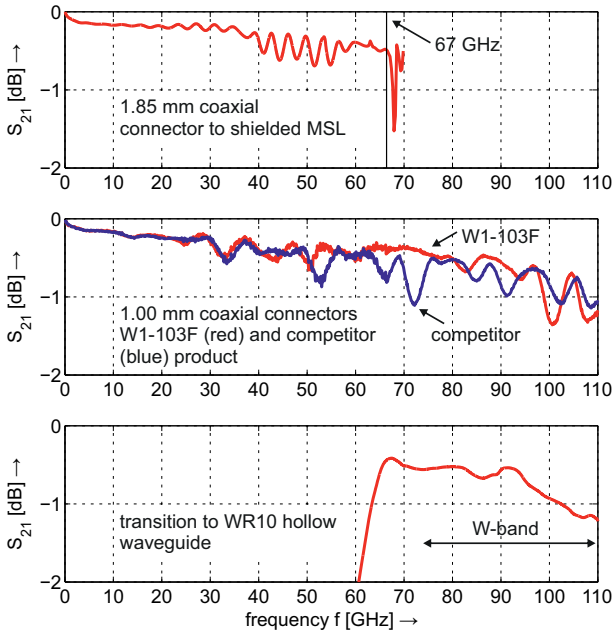

Figure 2.40: Measured magnitude of transmission coefficient S_{21} of single 1.85 mm connector, two different single 1.00 mm connectors and a single transition to WR-10 waveguide versus frequency.

There is no complete 3D model of the proprietary coaxial connectors available, therefore back to back measurements have been performed. Together with on-wafer measurements after enhanced-line-reflect-reflect-match (eLRRM) calibration [55] of the utilized Al_2O_3 thrulines, scattering parameters of the single connectors have been extracted. According to Fig. 2.40, insertion loss of the 1.85 mm connector is below 1 dB up to 67 GHz. Results from two different 1.00 mm connectors show insertion loss values below 1.5 dB from DC to 110 GHz (Fig. 2.40).

The 1.00 mm coaxial connector constitutes a costly but ultrawideband interconnect solution, covering the frequency range from DC to 110 GHz. If smaller output frequency ranges are acceptable, cost

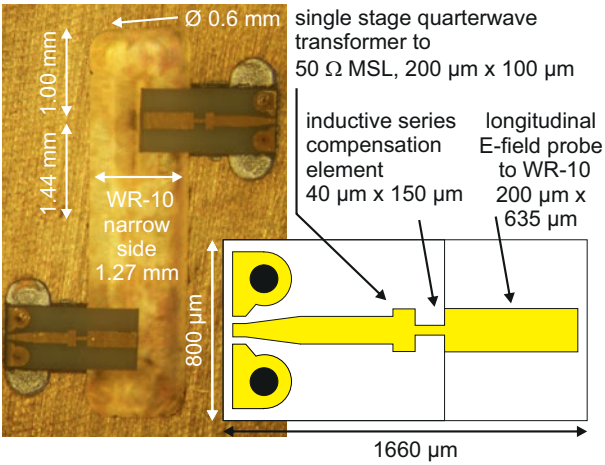

Figure 2.41: Photograph of MSL to WR-10 transition for back to back on-wafer measurement (second half of split-block not shown) and close up view of the planar transition.

effective hollow waveguides are preferred. Therefore longitudinal E-field probes to WR-10 waveguide have been developed. The transition in Fig. 2.41 allows for bondwire interconnection to the proposed frequency multipliers, other MICs or planar substrates. It is a split block construction, whereas Fig. 2.41 only shows the lower half of the mechanical housing. The E-field probe has half the length of the WR-10 hollow waveguide's narrow wall side. A large width of the probe is preferred to ensure high coupling, but it is limited by higher order modes. The probe's input impedance has a shunt capacitive behaviour. In conjunction with an inductive series compensation element, the remaining resistive input impedance is slightly below 50 Ω. A single stage quarterwave transformer allows for matching to 50 Ω. Dimensions are given in Fig. 2.41. The distance from E-field probe to the milled hollow waveguide backshort and the diameter of the milling tool determine the center frequency and influence the capacitance value of the probe. In back to back configuration with 2.88 mm WR-10 waveguide, a total insertion loss below 2.5 dB and

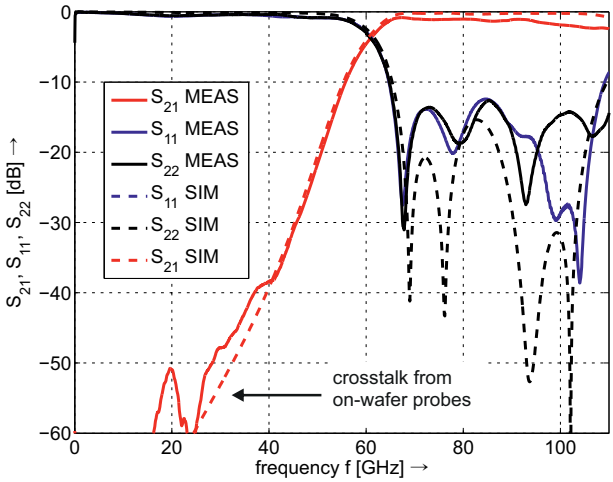

Figure 2.42: Scattering parameters of MSL to WR-10 transition in back to back configuration from 3D EM simulation and on-wafer measurement after eLRRM calibration versus frequency.

return loss greater than 13 dB from 63 to 110 GHz could be achieved (Fig. 2.42), which is an excellent result. Many similar transitions have been reported, e.g. [56], achieving less bandwidth and less return loss while incorporating comparable insertion loss values. With an Al_2O_3 substrate width of 0.8 mm, the same transition is easily redesigned for WR-15 and WR-12 waveguides. Lower permittivity and less substrate width is necessary to build similar transitions to WR-6 and WR-3 (section 2.7). Scattering parameters of a single transition have been extracted (Fig. 2.40). Insertion loss values are below 1.2 dB from 63 to 110 GHz.

Input Lowpass Filter Design Reflection of the generated harmonics at the circuit input of the proposed frequency multipliers is achieved by an 11^{th} order MSL stepped impedance LPF (Fig. 2.43) with 1 dB cut-off frequency at $f_{c\,1\,\text{dB}} = 52.5$ GHz and $f_{c\,3\,\text{dB}} = 54$ GHz. The design is based on the analytical synthesis procedure from Matthaei

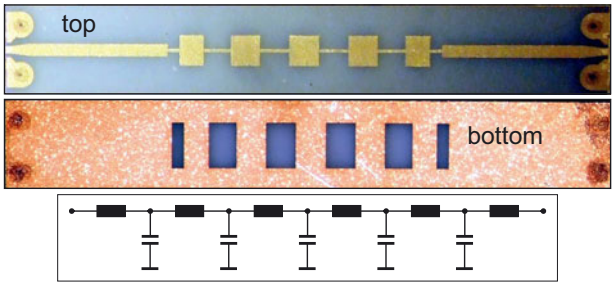

Figure 2.43: Photograph and circuit schematic of the 11$^{\text{th}}$ order stepped impedance MSL LPF filter. Top housing is not shown.

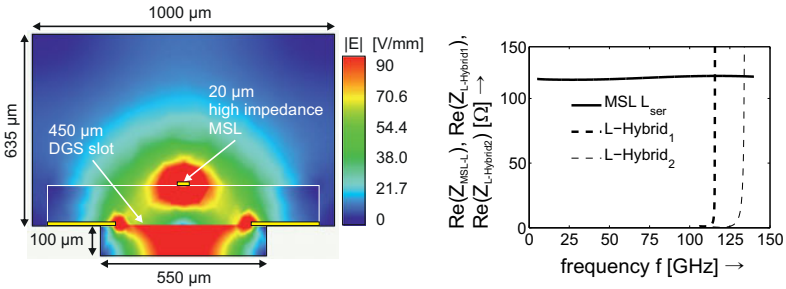

Figure 2.44: Cross-sectional view of the high impedance MSL with DGS, magnitude of the electric field strengths at 54 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_c)$ of MSL and the first two hybrid modes versus frequency. $\mathrm{Re}\,(Z_{c\,\mathrm{MSL}}) = 118.0\ \Omega$ and the corresponding effective permittivity is $\epsilon_{\mathrm{reff}} = 4.56$ at $f = 54$ GHz.

[57] with passband ripple of 0.01 dB, corresponding to 26 dB passband return loss, and stopband rejection of 25 dB at $1.2 \times f_{c\,3\,\mathrm{dB}} = 64.8$ GHz. The first and last filter elements are inductive to achieve open circuit stopband behaviour. The necessary inductance and capacitance values, extracted from the lowpass prototype filter at $f_{c\,3\,\mathrm{dB}}$, are summarized in column four of Table 2.3. 2D EM simulations in the frequency domain of the high (Fig. 2.44) and low (Fig. 2.45) impedance MSL cross-sections allow for extraction of effective permittivities ϵ_{eff} and real parts of the characteristic impedances $\mathrm{Re}\,(Z_c)$ at $f_{c\,3\,\mathrm{dB}}$. The

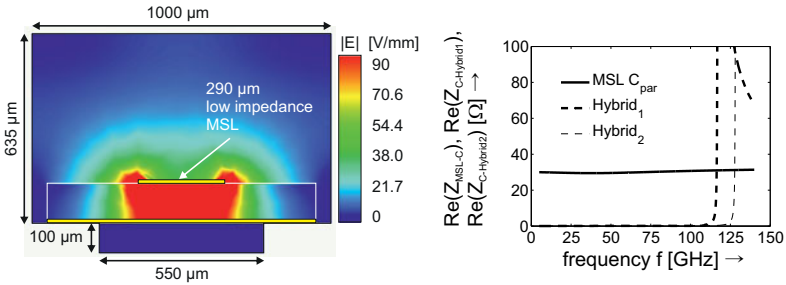

Figure 2.45: Cross-sectional view of the low impedance MSL, magnitude of the electric field strengths at 54 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_c)$ of MSL and the first two hybrid modes versus frequency. $\mathrm{Re}\,(Z_{c\,\mathrm{MSL}}) = 29.5\ \Omega$ and the corresponding effective permittivity is $\epsilon_{\mathrm{reff}} = 7.38$ at $f = 54$ GHz.

MSL frequency dispersion effects are not very pronounced. Fig. 2.44 and Fig. 2.45 show magnitudes of the electric field strengths at $f_{c\,3\,\mathrm{dB}}$ and the real parts of the characteristic impedances $\mathrm{Re}\,(Z_c)$ versus frequency of the fundamental and first two higher order hybrid modes. The MSL dimensions have been chosen to avoid higher order mode propagation up to 110 GHz. Hence, there is no need for ferrite absorber material within the milled channel. Due to the distributive nature of MSL, there is a second parasitic passband. The peak isolation and the achievable bandwidht of stopband increase with an increasing ratio of the high and low characteristic impedances $\mathrm{Re}\,(Z_{c\,\mathrm{L}})\,/\mathrm{Re}\,(Z_{c\,\mathrm{C}})$. To achieve a ratio of 4 and therefore greater than 20 dB stopband rejection from 60 to 110 GHz, the high impedance sections have been designed with 20 µm strip width and 450 µm DGS slot. To overcome insufficient peak isolation and bandwidth of stopband of preselector filters in ATS front end modules, several LPFs are arranged in cascade (compare Fig. 4.38). In case of ultrawideband frequency multipliers, we have to further design for preferably low reflection phase $\min\,(\arg S_{11})$ to avoid destructive interference of the incident desired harmonic with the backscattered one. Therefore, only filters with inherently good stopband behaviour are of interest. The analytical synthesis results in

Table 2.3: 11^{th} order stepped impedance MSL lowpass filter

filter elements	strip widths [µm]	lengths [µm]	inductance and capacitance values at f_c
1 and 11	20	126	105.8 pH
2 and 10	290	236	72.4 fF
3 and 9	20	281	236.0 pH
4 and 8	290	285	87.5 fF
5 and 7	20	301	252.8 pH
6	290	292	89.6 fF

filter order $N = 11$, cut-off frequency $f_{c\,1\,\text{dB}} = 52.5$ GHz,
$f_{c\,3\,\text{dB}} = 54$ GHz, passband ripple $r_{\text{dB}} = 0.01$ dB,
stopband rejection of 25 dB at $1.2 \times f_{c\,3\,\text{dB}}$.

LPFs with slightly different cut-off frequency. A single scaling factor $0.5 < \ell_{\text{scale}} < 1.5$ for the lengths of the inductive and capacitive filter elements within parameterized 3D EM model is sufficient to map the 1 dB cut-off frequency to 52.5 GHz. The final dimensions are summarized in Table 2.3.

3D EM simulated scattering parameters including the transition to 1.85 mm connector from Fig. 2.39 are compared to on-wafer measurements after eLRRM calibration in Fig. 2.46. Passband return loss values are greater than 20 dB. The parasitic passband and higher order mode effects only occur at frequencies greater than 120 GHz. The isolation discrepancies at around 95 GHz are due to crosstalk of the on-wafer probes. These results have been checked with thru-reflect-line (TRL) calibration [58], [B1]. To underpin suitability of the designed LPF, the gray shaded areas in Fig. 2.46 indicate the input $f_{\text{in}} = [20, 36.67]$ GHz and output frequency ranges $f_{\text{out}} = [60, 110]$ GHz of frequency tripler #1 to #3. To build frequency doublers with the same output frequency range, a filter order of at least $N = 15$ is required to establish passband behaviour at the highest input fre-

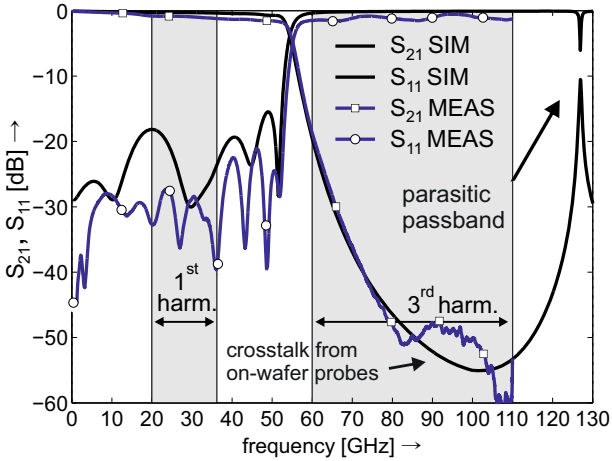

Figure 2.46: Scattering parameters of the 11th order LPF from 3D EM simulation (including transition to 1.85 mm) and on-wafer measurement after eLRRM calibration versus frequency.

quency along with sufficient stopband rejection at the lowest output frequency. However, within the applied dicing process the maximum substrate length of 6 mm does not allow for higher filter orders. Utilizing the presented LPF for frequency doubling (subsections 2.6.4 and 2.6.5), the achievable input and output frequency ranges are $f_{\text{in}} = [27.5, 53]$ GHz, $f_{\text{out}} = [53/55, 106]$ GHz. Fig. 2.47 compares simulated and measured insertion loss of the LPF. The input frequency ranges of both, triplers and doublers are indicated.

Multiplier Assembly As already outlined, coaxial connectors are used to ease experimental characterization. Fig. 5.15 shows the mechanical housing with 1.85 mm / 1.00 mm connectors. Within an integrated front end module, either split block constructions or lid (Fig. 5.15) can be used. The glass bead of the 1.85 mm connector from Fig. 2.39 is soldered to the Au-plated brass housing utilizing solder with high melting temperature ($T_{\text{M}} \approx 219$ °). The further assembly steps are illustrated in Fig. 2.49. Although the DBES105a diode pads are

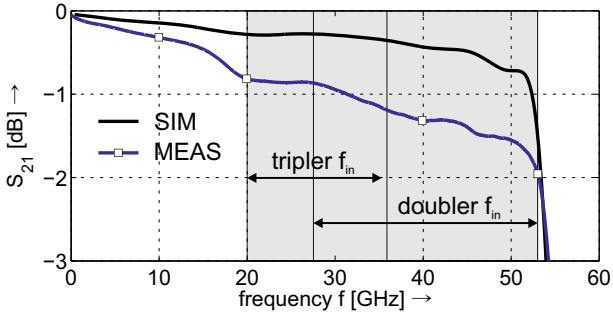

Figure 2.47: Magnitude of transmission coefficient S_{21} of the 11$^{\text{th}}$ order LPF from 3D EM simulation (including transition to 1.85 mm) and on-wafer measurement after eLRRM calibration versus frequency.

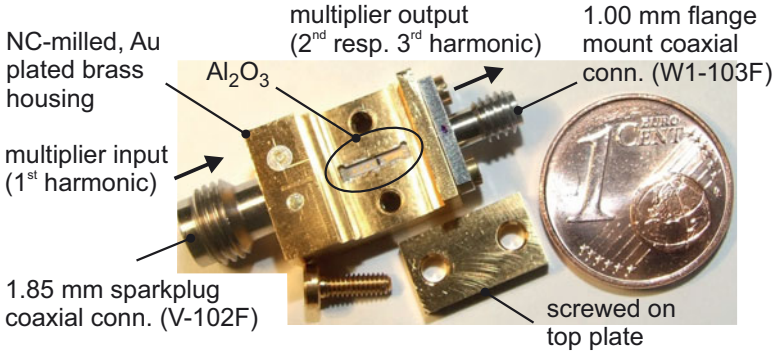

Figure 2.48: Mechanical housing of the proposed frequency multipliers with 1.85 mm / 1.00 mm coaxial connectors (top view).

equipped with Au bumps to allow for thermo-sonic bonding assembly, conventional solder paste (62Sn-36Pb-2Ag, $T_{\text{M}} = 179$ °) with particle size of 20 to 45 µm is used to mount the diode on the Al_2O_3 substrates (0.9 mm × 6.0 mm). As it is shown in Fig. 2.49, while soldering the substrate is fixed with high temperature resistant polyimide tape with silicon adhesive on a hotplate. As a second solder step with the same solder paste, substrate and diode are assembled to the Au-plated brass housing. Finally the stress relief of the 1.85 mm connector

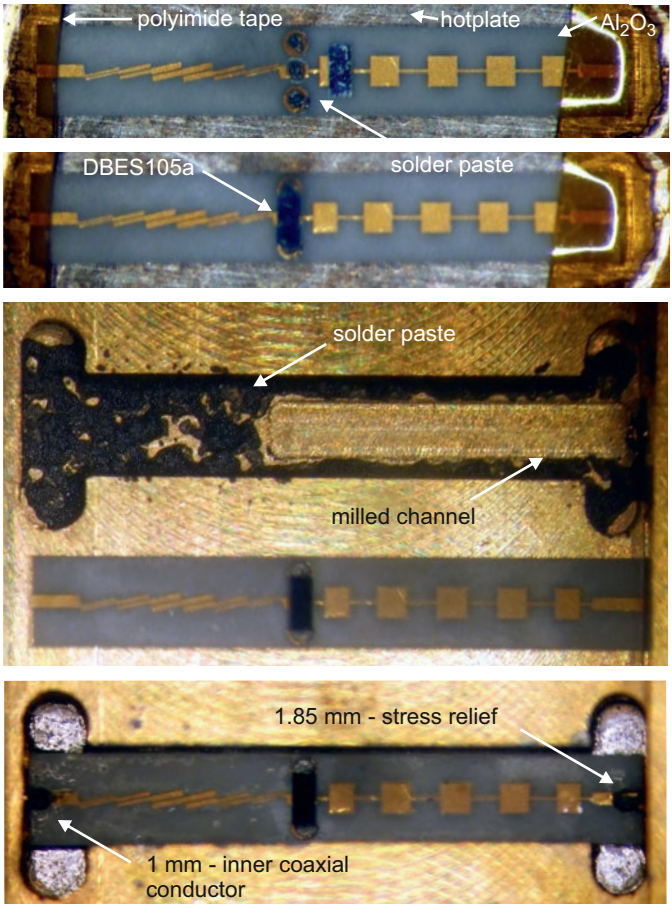

Figure 2.49: Frequency multiplier assembly steps.

(Fig. 2.39) and the inner coaxial conductor of the 1.00 mm connector are soldered to MSL with an indium- (In) ($T_M = 154$ °) or bismuth-based (Bi) ($T_M = 140$ °) solder. Alternatively conductive adhesive is used. Table 2.4 summarizes electrical conductivity properties and melting points of several solders and conductive adhesives.

Table 2.4: Comparison of solder alloys and conductive adhesives for multiplier assembly

solder or conductive adhesive	IACS [%]	el. cond. σ [MS/m]	approx. melt. T_M point [°]
96.5Sn-3Ag-0.5Cu	16	9.3	219
SC126 (62Sn-36Pb-2Ag)	14	8.1	179
Indalloy 2 (80In-15Pb-5Ag)	13	7.5	154
Indalloy 1E (52In-48Sn)	11.7	6.8	118
Indalloy 282 (57Bi-42Sn-1Ag)	4.5	2.6	140
EPO-TEK® H20E	0.69	0.4	-
Panacol Elecolit® 325	0.34	0.2	-

IACS compares conductivity to copper material (Cu), $\kappa_{Cu} = 58$ MS/m and $IACS_{Cu} = 100$ %.

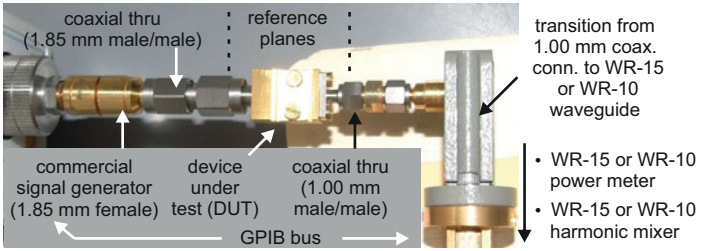

Figure 2.50: Measurement setup of the proposed multipliers with 1.85 mm / 1.00 mm coaxial connectors.

Measurement Setup The fully assembled multipliers with 1.85 mm / 1.00 mm coaxial connectors are driven by a commercial signal generator, 5 dBm $\leq P_{in} \leq$ 18 dBm, within the input frequency range. Fig. 2.50 illustrates the measurement setup. The scalar output power level is measured with commercial V- and W-band power meters. All measurement results are corrected for the additional insertion loss of the measurement setup, a 1.00 mm thru connector and transitions to

WR-15 and WR-10 waveguide, but include the influence of the multiplier's coaxial connectors (reference planes in Fig. 2.50). Power meter measurements constitute the most precise method to capture scalar power levels, but do not allow for distinguishing spectral components of the harmonic content. Spectral measurements with decreased accuracy are performed with calibrated V- and W-band harmonic mixers in front of a spectrum analyzer to verify the power meter measurements consider the envisaged spectral components and to measure the multiplier's rejection of undesired harmonics (subsection 2.7.2).

2.6.1 Frequency Tripler x3_HE_1 (#1)

Top and bottom view of the manufactured x3_HE_1 (#1) frequency tripler [I6] Al_2O_3 substrates are shown in Fig. 2.51.

After the 1.85 mm connector or bondwire transition within integrated modules, the fundamental signal passes the input LPF, which ensures reflection of the multiplied harmonics. The mechanical housing provides a milled channel, required for DGS of the high impedance LPF sections. The Smith chart in Fig. 2.52 depicts the impedances provided to the diode junctions, including the diode mounting structure (Γ_{in} in Fig. 2.51). The 1st harmonic should be matched, which is the case and does unfortunately hold true partly for the 2nd harmonic. The 3rd harmonic frequencies are arranged around the ideal open circuit at 79.5 GHz, which is essential for proper operation. In cascade to the LPF, the two Schottky junctions of DBES105a diode are excited in antiparallel configuration.

Assuming equal Schottky junction behaviour, the antiparallel diode configuration ensures an effective suppression of the 2nd and 4th harmonic (short idlers, [54]). Within this balanced configuration no measures can be adopted to reject the 5th harmonic.

The same waveguide (MSL) is used at the input and output of the diode mounting structure. This is critical, as the electrical length from the diode junctions to the output HPF has to stay below 180 degree at f_{in}. Highpass filtering is established by exciting a HE_1 like mode with 53 GHz cut-off frequency in the area of its electric field

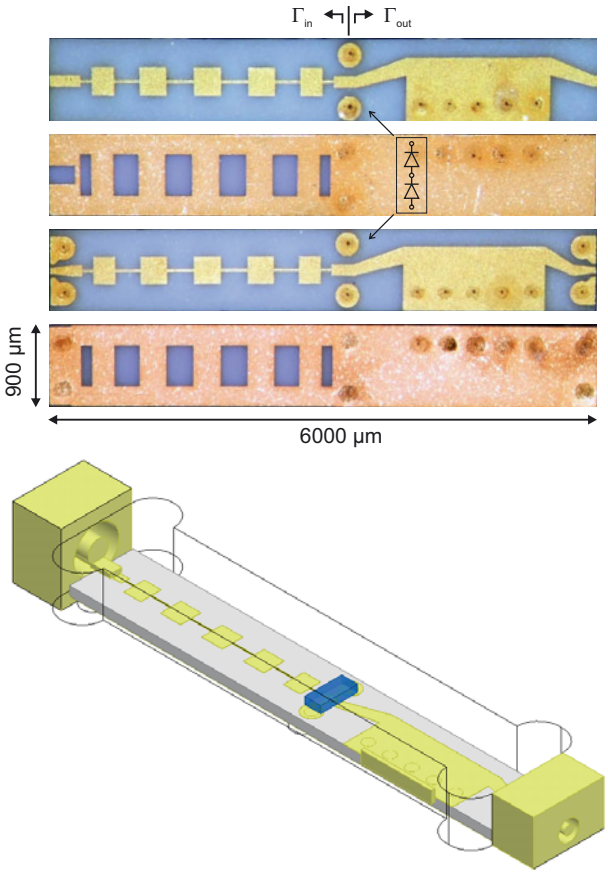

Figure 2.51: Top and bottom view of the manufactured x3_HE_1 frequency tripler Al_2O_3 substrates (0.9 mm × 6.0 mm) and 3D model for coaxial interconnection.

maximum (Fig. 2.53). The HE_1 mode is guided by a slot between the top metallization and the mechanical housing. This class of HPFs has first been suggested by Chramiec in 1981 [59–61] and has also been discussed as a degenerated case of transmission line comb HPFs recently in [62].

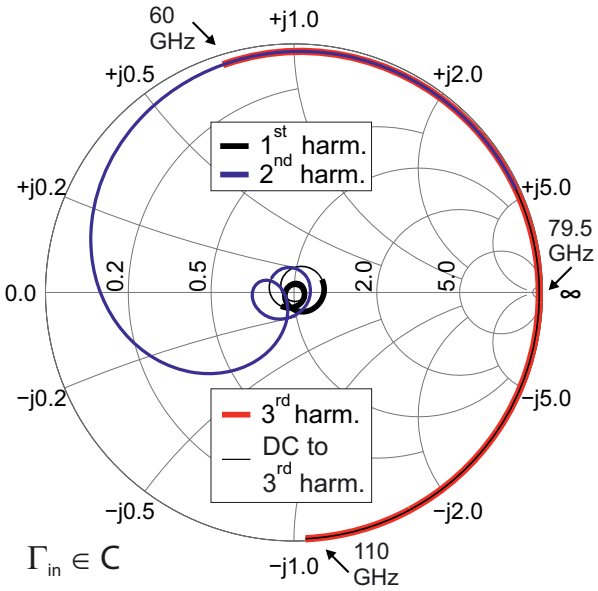

Figure 2.52: 3D EM simulated input impedances of x3_HE$_1$ (including transition to 1.85 mm) provided to the diode junctions visualized in the Smith chart versus frequency. $\Gamma_{in} \in \mathbb{C}$.

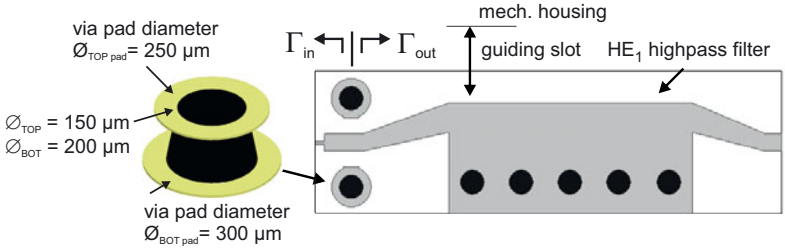

Figure 2.53: Detail view of the transition from x3_HE$_1$ diode mounting structure to HE$_1$ waveguide.

Fig. 2.54 shows a cross-sectional view of the HE$_1$ waveguide with 250 µm gap to the metallic enclosure, the magnitude of the HE$_1$ mode electric field strength at 80 GHz and the real parts of the characteristic

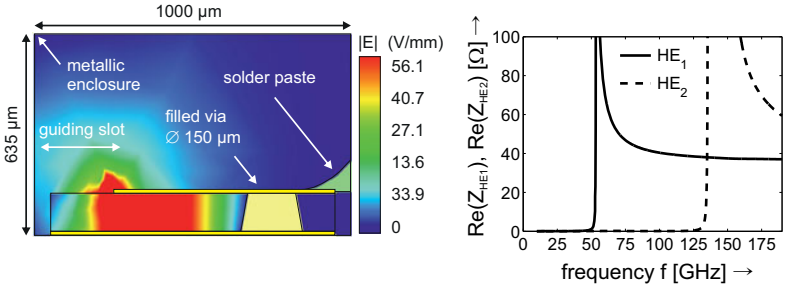

Figure 2.54: Cross-sectional view of the HE_1 waveguide, magnitude of the electric field strengths at 80 GHz and real parts of the characteristic impedances of HE_1 and HE_2 versus frequency.

impedances of HE_1 and HE_2 versus frequency. The HE_1 waveguide is in single mode operation up to $\approx$ 130 GHz and exhibits much lower impedance (power-current definition) values than conventional unilateral finlines (uFIN). Therefore, it can be matched more easily to 50 Ω MSL. Fig. 2.55 shows scattering parameters of the output HPF (including transition to 1.00 mm) from 3D EM simulation with return loss values greater than 15 dB at f_{out}. Selectivity is nearly proportional to the HE_1 waveguide length. The chosen length of 1.55 mm is a compromise between additional loss and 1st harmonic rejection.

The Smith chart in Fig. 2.56 shows the impedances provided to the diodes at the output port, including the diode mounting structure (Γ_{out} in Fig. 2.51).

The HPF is an ideal short circuit at DC. The 1st harmonic is rejected with nearly open circuit idle impedances (ideal open circuit at $f =$ 34 GHz). The 2nd harmonic is idled capacitively. The 3rd harmonic is matched. The feeding MSL length behind the diodes of this HPF could be designed much shorter to stay below 180 degree at f_{in}, but to reduce the coupling between HE_1 and the diode mounting structure a minimum length is required. Otherwise the circuit symmetry is affected and the even order harmonic suppression of the antiparallel diode configuration deteriorates drastically.

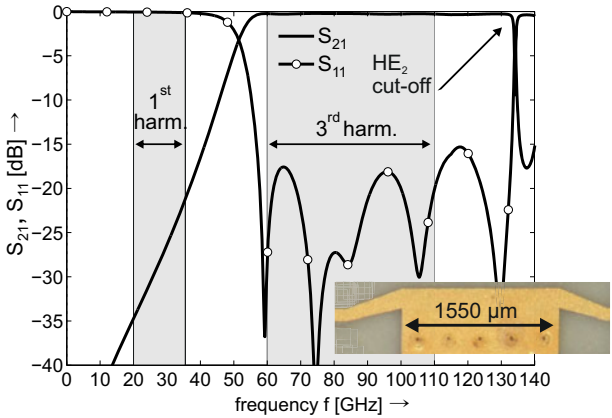

Figure 2.55: 3D EM simulated scattering parameters of the output HPF (including transition to 1.00 mm) versus frequency.

Fig. 2.57 shows the 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 60,\ 66,\ 75,\ 82,\ 95,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data in the frequency range of 60 to 110 GHz are within the gray shaded area.

A minimum input power level of $P_{\text{in}} = 10$ dBm to 14 dBm (at the high end of f_{out}) should be provided. At an input drive level of 18 dBm, the achieved output power levels are within the range of −3 to 1 dBm. A comparison of the measured conversion loss (solid lines) at $P_{\text{in}} = 12,\ 14,\ 16,\ 18$ dBm with results from co-simulation (dashed lines) is given in Fig. 2.58. The conversion loss averages out at 18 dB from 60 to 95 GHz and is below 22 dB up to 110 GHz, which is 2 to 6 dB less output power than simulation results predict. Spectral measurements up to the 5th harmonic have been performed. Fundamental rejection behaves according to Fig. 2.55, which means 20 dB at 40 GHz. At $P_{\text{in}} = 18$ dBm suppression of the 2nd and 4th harmonic is better than 15 dBc. In the frequency range of 100 to 110 GHz rejection of the 5th harmonic is at least 8 dBc (Fig. 2.59).

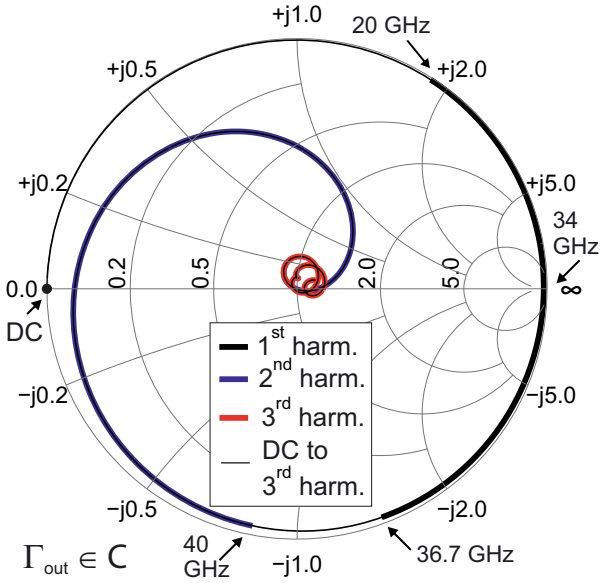

Figure 2.56: 3D EM simulated output impedances of x3_HE$_1$ (including transition to 1.00 mm) provided to the diode junctions visualized in the Smith chart versus frequency. $\Gamma_{\text{out}} \in \mathbb{C}$.

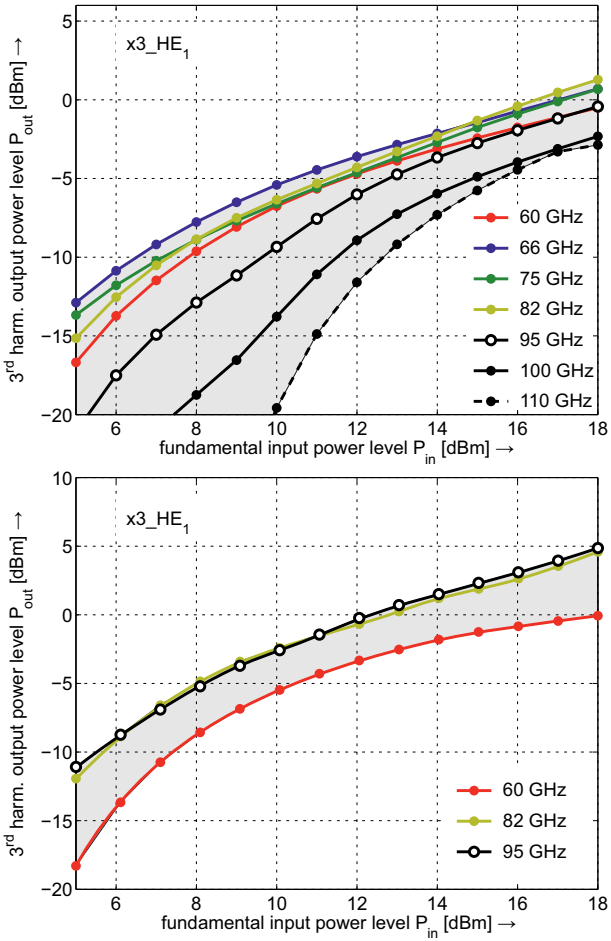

Figure 2.57: 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 60,\ 66,\ 75,\ 82,\ 95,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data (top) and simulation data (bottom) in the frequency range of 60 to 110 GHz are within the gray shaded area.

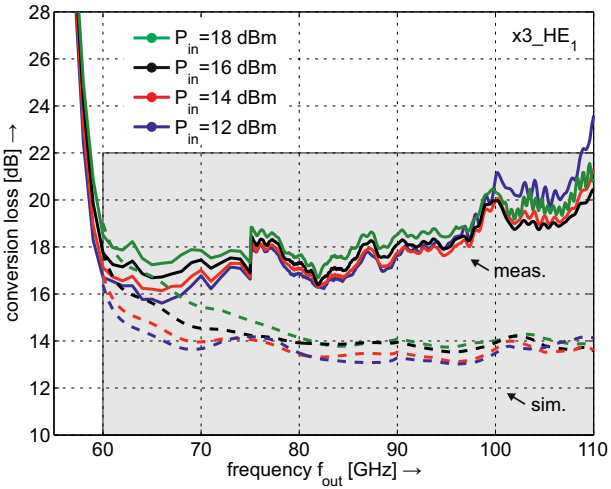

Figure 2.58: Comparison of measured (solid) and simulated (dashed) conversion loss versus output frequency f_{out}. Input power levels $P_{\text{in}} = 12,\ 14,\ 16,\ 18$ dBm.

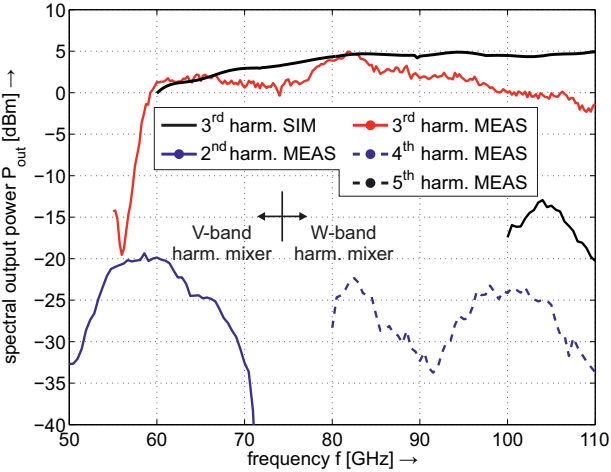

Figure 2.59: Measured spectral output power levels up to the 5^{th} harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 18$ dBm. Compared to simulated 3^{rd} harmonic output power levels with $P_{\text{in}} = 18$ dBm (black, solid).

2.6.2 Frequency Tripler x3_uFIN (#2)

Top and bottom view of the manufactured x3_uFIN (#2) frequency tripler Al_2O_3 substrates are shown in Fig. 2.60. The input circuitry is identical to the configuration of x3_HE_1 from subsection 2.6.1. The fundamental signal drives the Schottky junctions in antiparallel configuration. The cut-off behaviour of a transition from MSL to uFIN allows for highpass filtering and provides open circuit behaviour for the fundamental signal at the output. Cross-sectional view of the uFIN waveguide with 30 µm slot, magnitude of the electric field strengths at 80 GHz and real parts of the characteristic impedances of $uFIN_1$ and $uFIN_2$ versus frequency are shown in Fig. 2.61. With cut-off frequency of $f_c = 39.5$ GHz, the uFIN exhibts 98 Ω characteristic impedance at 50 GHz, 80 Ω at 60 GHz and 63 Ω at 110 GHz. The upper limit of operating frequency range is 129 GHz due to the next higher order mode $uFIN_2$. The generated harmonics propagate from the diode mounting structure to the transition in MSL mode. Fig. 2.62 depicts a detail view. The configuration in Fig. 2.62 was first suggested by Gupta [63] for slotlines and was recently used with finlines [64, 65]. The transition in [G1] achieves an output frequency range of 70 to 110 GHz on a low permittivity substrate. The fundamental TEM mode at MSL is short circuited at the end, which is necessary to also cover the lower frequencies ≥ 60 GHz. Magnetic field coupling excites the hybrid finline mode guided by a 30 µm slot. One end of the finline waveguide is terminated in an open circuit with rectangular shape, similar to quarterwave backshorts in hollow waveguide to MSL transitions. The dimensions of the taper and rectangle are chosen to transform the finline short circuit to an open circuit for an operating frequency range of 60 to 110 GHz. Simulated scattering parameters of the transition in back to back configuration with a total length of $\ell = 2500$ µm are shown in Fig. 2.63 and predict return loss values in the order of 20 dB. Due to the high permittivity substrate, the necessary quarterwave backshort dimensions (450 µm × 50 µm) are quite small compared to similar realizations on SiO_2 or teflon (PTFE). This is advantageous to keep the substrate width small enough for single mode operation

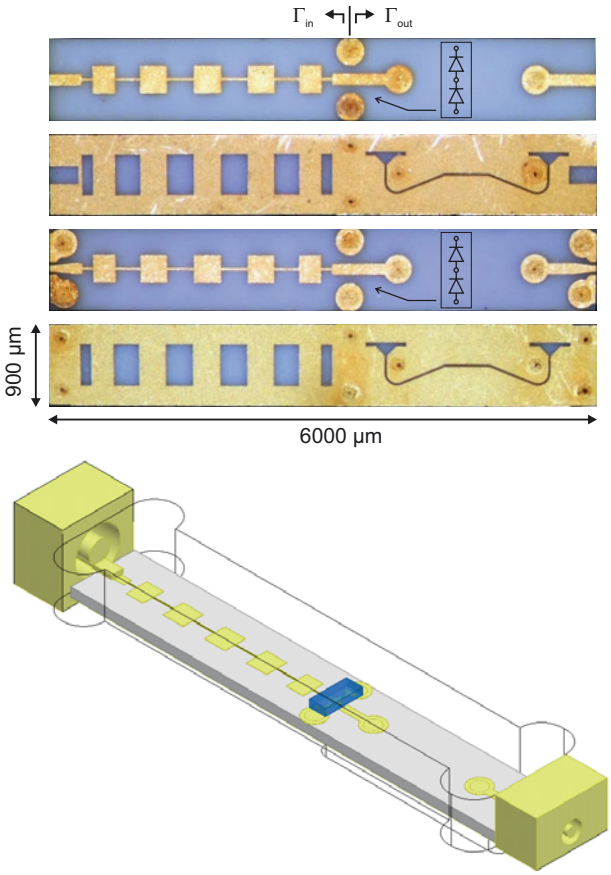

Figure 2.60: Top and bottom view of the manufactured x3_uFIN frequency tripler Al_2O_3 substrates (0.9 mm × 6.0 mm) and 3D model for coaxial interconnection.

up to 110 GHz but leads to more sensitive device performance in presence of tolerances. Contrary to x3_HE$_1$ from subsection 2.6.1, the filled plated-through vias are drilled from top to bottom layer. Consequently the greater via diameter of $\varnothing_{\mathrm{TOP}} = 200$ µm appears at the top layer. This is necessary to allow for a short distance between the position of maximum magnetic field coupling and the

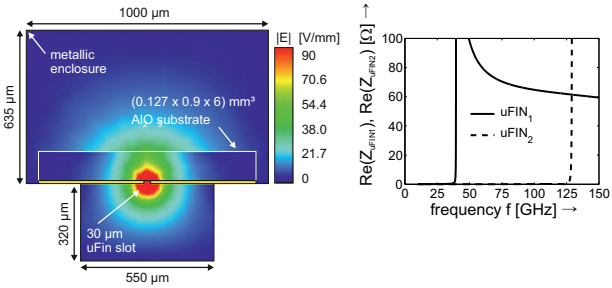

Figure 2.61: Cross-sectional view of the uFIN waveguide, magnitude of the electric field strengths at 80 GHz and real parts of the characteristic impedances of uFIN_1 and uFIN_2 versus frequency.

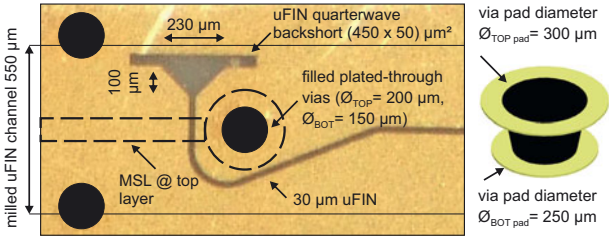

Figure 2.62: Detail view of the transition from x3_uFIN diode mounting structure to uFIN (bottom layer) waveguide.

via barrel, which has to be kept below quarterwave length up to the maximum operating frequency. The Smith chart in Fig. 2.64 shows the impedances provided to the diodes at the output port including the diode mounting structure (Γ_{out} in Fig. 2.60). The HPF is an ideal short circuit at DC. The 1st harmonic frequency range is rejected with inductive behaviour at the lower band limit and nearly open circuit behaviour at the upper band limit. The 2nd harmonic is idled capacitively and partly matched at the frequencies that overlap with the desired output frequency range f_{out}. The 3rd harmonic is matched.

Fig. 2.65 shows the 3rd harmonic output power levels P_{out} at the output frequencies $f_{\mathrm{out}} = 60,\ 65,\ 72,\ 80,\ 95,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data in

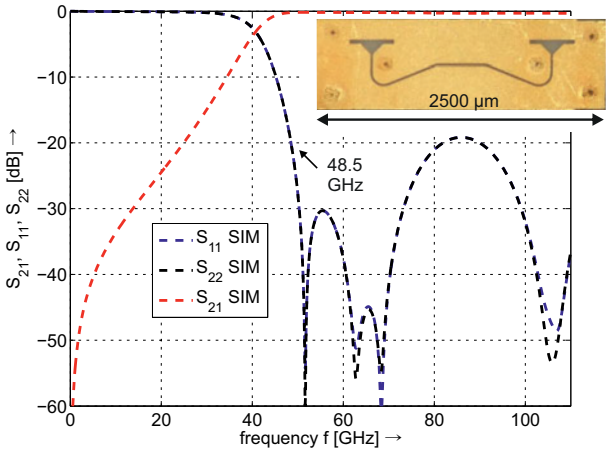

Figure 2.63: Photograph and 3D EM simulated scattering parameters of MSL to uFIN transition in back to back configuration versus frequency (total length $\ell = 2500$ µm).

the frequency range of 60 to 110 GHz are within the gray shaded area. A comparison of the measured conversion loss (solid lines) at $P_{\text{in}} = 12,\ 14,\ 16,\ 18$ dBm with results from co-simulation (dashed lines) is given in Fig. 2.66. With $P_{\text{in}} = 18$ dBm the conversion loss is below 19 dB from 60 to 100 GHz and is below 22 dB up to 103 GHz. There is a sharp increase of conversion loss above 103 GHz. In Fig. 2.62 the milled channel with width of 550 µm is marked. Optical measurements of the assembled multiplier have shown that due to a slightly off-center position of the substrate within the mechanical housing the backshort geometry is partly overlaid by the housing. Therefore, the assembled structure is not capable of operating up to 110 GHz. The problem can be solved by using marginally greater channel width, at least in the area of the backshort geometry. Reliable soldering is still possible with less contact area. Spectral measurements up to the 5^{th} harmonic have been performed. At $P_{\text{in}} = 18$ dBm suppression of the 2^{nd}, 4^{th}, and 5^{th} harmonic is better than 10 dBc from 60 to 110 GHz (Fig. 2.67).

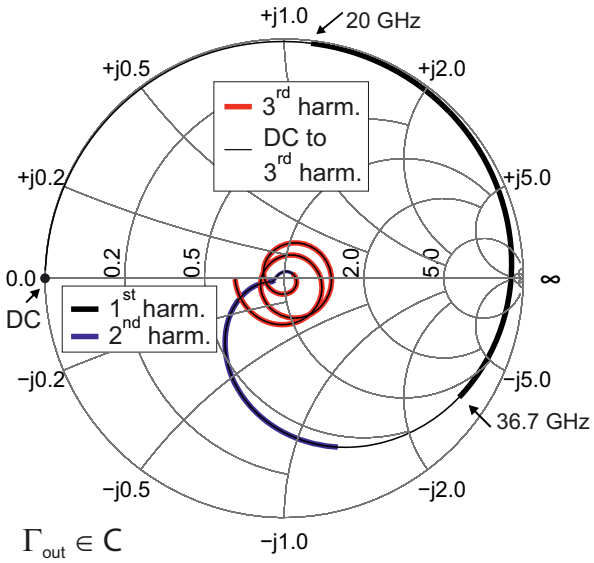

Figure 2.64: 3D EM simulated output impedances of x3_uFIN (including transition to 1.00 mm) provided to the diode junctions visualized in the Smith chart versus frequency. $\Gamma_{\mathrm{out}} \in \mathbb{C}$.

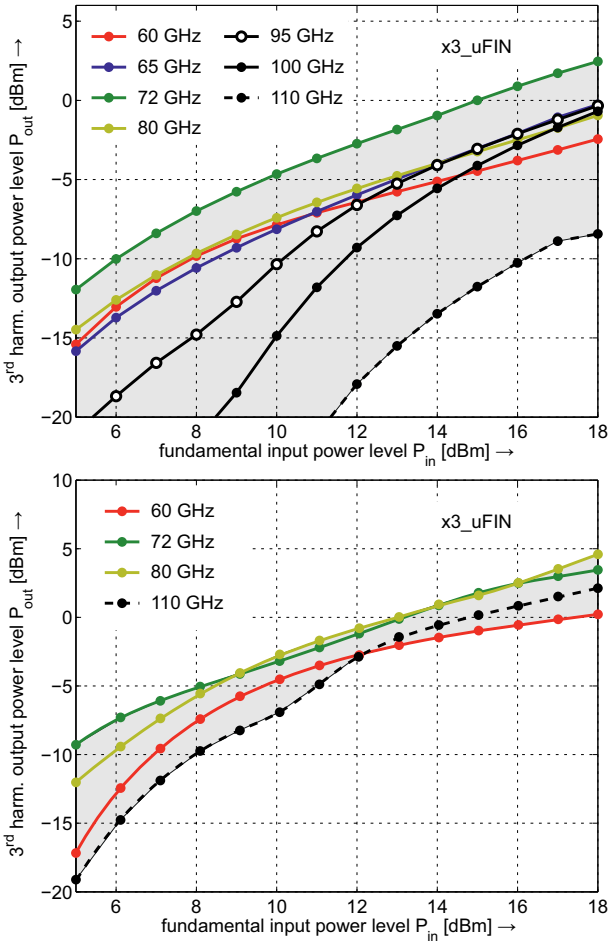

Figure 2.65: 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 60,\ 65,\ 72,\ 80,\ 95,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data (top) and simulation data (bottom) in the frequency range of 60 to 110 GHz are within the gray shaded area.

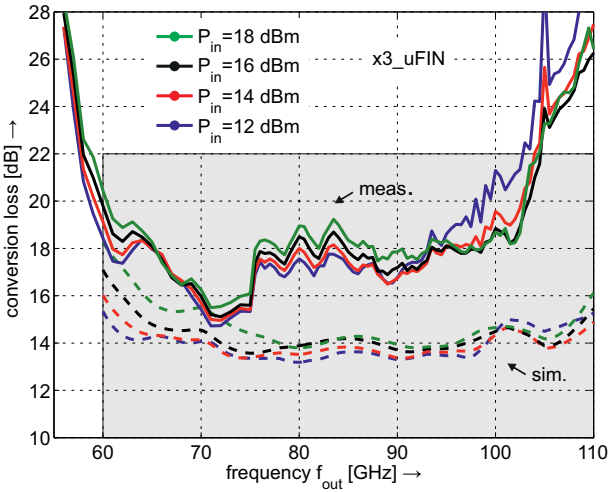

Figure 2.66: Comparison of measured (solid) and simulated (dashed) conversion loss versus output frequency f_{out}. Input power levels $P_{\text{in}} = 12,\ 14,\ 16,\ 18$ dBm.

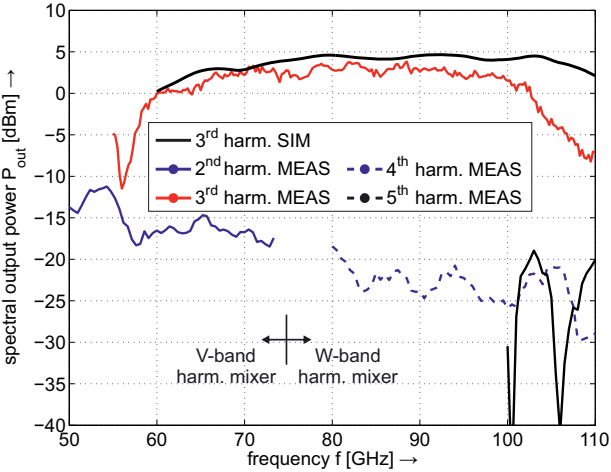

Figure 2.67: Measured spectral output power levels up to the 5^{th} harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 18$ dBm. Compared to simulated 3^{rd} harmonic output power levels with $P_{\text{in}} = 18$ dBm (black, solid).

2.6.3 Frequency Tripler x3_SIDE (#3)

Top and bottom view of the manufactured x3_SIDE (#3) frequency tripler Al_2O_3 substrates are shown in Fig. 2.68. The input circuitry of x3_SIDE is identical to multiplier #1 and #2. The two Schottky junctions are driven in antiparallel configuration by the fundamental signal. Beside the fundamental signal, all harmonics with different power levels exist across the Schottky junctions. An input LPF and output HPF allows for controlling spectral harmonic content at the multiplier's input and output. With ultrawideband frequency multiplier design, it is a key function to avoid destructive interference of the fundamental and desired harmonic $\left(3^{\text{rd}}\right)$ at the Schottky junctions over the input and output frequency ranges. This is achieved with filter structures that show minimum reflection phase $\min\left(\arg S_{11}\right)$. As already mentioned, this normally prohibits the use of many LPFs in cascade. The frequency triplers #1 and #2, as well as #4 and #5 all make use of different modes of propagation at the input and output. Utilizing the cut-off behaviour as HPF is an excellent solution with respect to minimum reflection phase. Literal HPF resp. BPF based on lowpass to highpass transformation with quarterwave or halfwave resonators according to Matthaei [57] are difficult to implement in ultrawideband frequency multipliers. Realizing octave bandwidth BPF is challenging and requires high filter order, which is associated with greater insertion loss and reflection phase. The presented multipliers in this section utilize HE_1 waveguide and several uFIN solutions. In section 2.5 [G2] bilateral finlines are successfully applied to build up a frequency tripler with output frequency range of 20 to 40 GHz, which is another promising concept for E- and W-band frequency multipliers. Nevertheless, utilization of hybrid modes at the output complicates the mechanical housing and to some extent makes device performance conditional to the housing. There are fields of application that benefit from the use of resonator-based output filters in multiplier designs, although the maximum achievable bandwidth is reduced. Therefore, multiplier #3 with halfwave resonator BPF at the output (Fig. 2.69) has been developed. The 5^{th} order BPF is

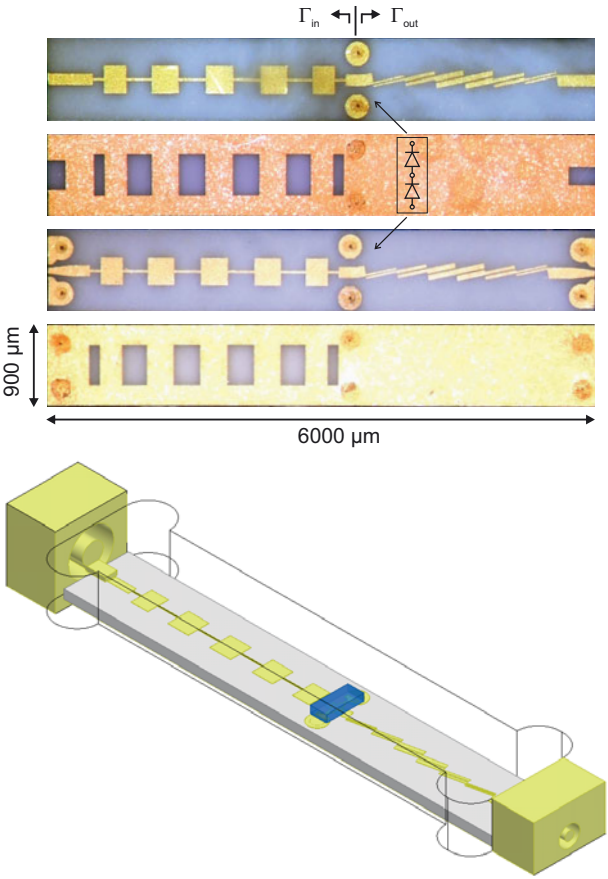

Figure 2.68: Top and bottom view of the manufactured x3_SIDE frequency tripler Al_2O_3 substrates (0.9 mm × 6.0 mm) and 3D model for coaxial interconnection.

based on side-coupled striplines (cMSL), each of them a quarterwave length long, to act as impedance inverters $J_k, k \in \mathbb{N}$ for the MSL halfwave parallel resonators. The center frequency of the design is $f_0 = \sqrt{70 \cdot 110}$ GHz = 87.7 GHz, which means fractional bandwidth of FBW = 46 %. Fig. 2.70 illustrates the cross-sectional view of the first J_1 and last J_6 inverter's cMSL and magnitudes of the electric

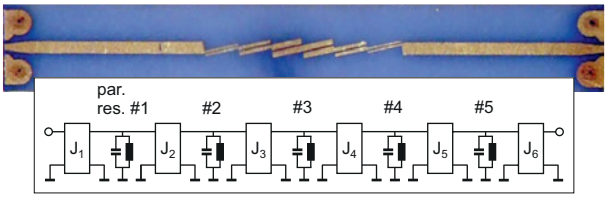

Figure 2.69: Photograph of the 5th order coupled microstrip halfwave resonator BPF with corresponding block diagram.

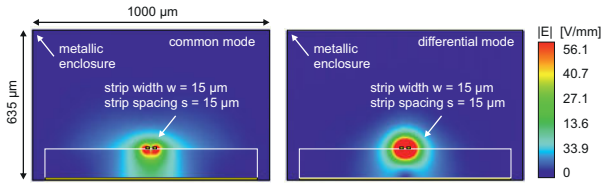

Figure 2.70: Cross-sectional views of the first side-coupled microstrip line (cMSL, first and last J inverter) and magnitudes of the electric field strengths of common and differential modes at 87.7 GHz.

field strengths of common and differential modes at $f_c = 87.7$ GHz. Stepped impedance LPF designs benefit from a large ratio of high and low characteristic impedances of the incorporated filter elements to achieve great bandwidth of stopband. Similarly the BPF requires a high ratio between the even mode characteristic impedance of the outer J inverters compared to the J inverters in the filter center to achieve great passband frequency range. The concepts described in [66] based on DGS technique allow for realization of greater even mode impedances compared to fully backside metallized cMSL. Further on the center frequency of the second parasitic passband is increased if the even and odd mode of each J inverter experience the same electrical length when propagating along the quarterwave cMSL waveguide. This is critical with dispersive cMSL realizations. DGS technique allows for increasing the phase velocity of the even mode to match the odd mode phase velocity. Superior suppression of the second passband could be achieved in [66] for BPF operating from 10 to

Table 2.5: 5^{th} order halfwave resonator bandpass filter

impedance inverters J_k	even and odd mode impedances $Z_{0e}, Z_{0o}[\Omega]$, required / 2D EM sim.	strip widths and spacings [µm]	lengths [mm]
1 and 6	$135,43$ / $137.9,44.6$	$15,15$	343
2 and 5	$111,40$ / $113.3,41.2$	$30,20$	324
3 and 4	$94,35$ / $95.7,36.0$	$50,20$	307

filter order $N = 5$, fractional bandwidth FBW $= 46$ %,
center frequency $f_0 = \sqrt{70 \cdot 110}$ GHz $= 87.7$ GHz.

20 GHz. DGS technique is indispensable for the presented input LPF at f_{in}, but complicates the analytical based design flow of the BPF. It is further difficult to keep cut-off frequency of higher order modes greater than the maximum operating frequency if DGS technique is used for cMSL at W-band frequencies and beyond. The designed BPF for multiplier #3 without DGS technique utilizes minimum strip widths and spacings of 15 µm, which is sufficient to realize pass-band frequency range of 70 GHz to 110 GHz. Filter performance is achieved without via interconnections. The characteristic impedances of each inverter's even and odd mode from analytical synthesis [57], together with corresponding values of the actual realization (2D EM simulation) are summarized in Table 2.5. Contrary to the presented LPF design, the analytical requirements cannot be realized as good with dispersive cMSL. Therefore, deviations from analytically calculated filter performance to 3D EM simulation and measurement have to be tolerated. Scattering parameters from 3D EM simulation and on-wafer measurement after eLRRM calibration are shown in Fig. 2.71. Poor isolation from 20 to 40 GHz is caused by crosstalk between the on-wafer probes and is not a problem within integrated front end modules. Simulation and measurement are in very good agreement, except for underestimation of real losses in 3D EM simulation. The achieved bandwidth and performance constitute almost

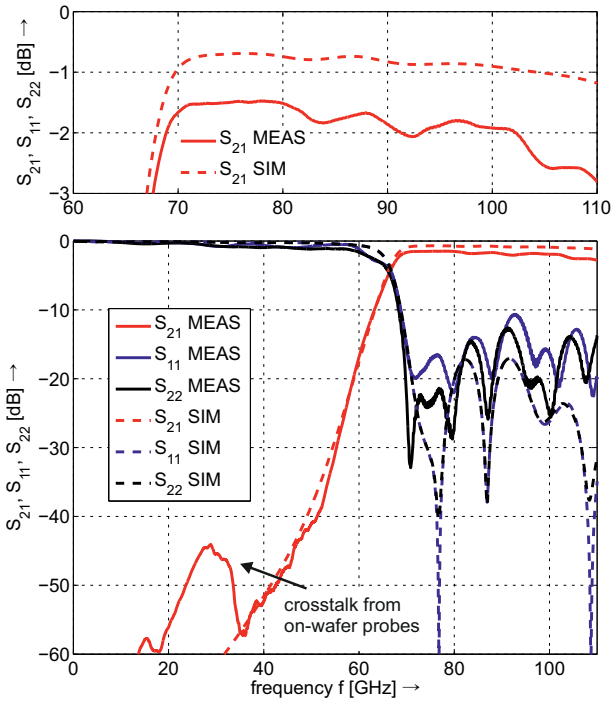

Figure 2.71: Scattering parameters of 5th order coupled microstrip halfwave resonator bandpass filter from 3D EM simulation and on-wafer measurement after eLRRM calibration versus frequency.

the limit for this filter architecture. The analytical synthesis results do not show the roll-off at the lowest and especially at the highest passband frequency, visible in Fig. 2.71, but could be observed by the author in many side-coupled BPF realizations with different center frequencies f_0. Other architectures are required to build filters with sharper edges and greater bandwidth, e.g. [67] based on broad-side coupled quarterwave resonators. The Smith chart in Fig. 2.72 depicts the impedances provided to the diodes at the output port including the diode mounting structure and the transition to 1.00 mm coaxial connector (Γ_{out} in Fig. 2.68). The filter is an ideal open circuit at

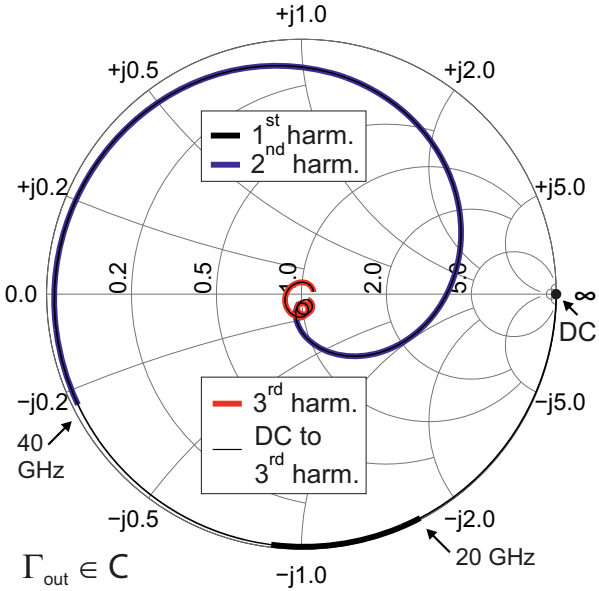

Figure 2.72: 3D EM simulated output impedances of x3_SIDE (including transition to 1.00 mm) provided to the diode junctions visualized in the Smith chart versus frequency. $\Gamma_{\text{out}} \in \mathbb{C}$.

DC. The 1st harmonic is rejected capacitively. The 2nd harmonic is arranged around the ideal short circuit and matched at frequencies > 70 GHz. The 3rd harmonic and part of the 4th harmonic's frequency range are matched. Suppression of the even order harmonics $\left(2^{\text{nd}} \text{ and } 4^{\text{th}}\right)$ is realized by the antiparallel diode configuration (short idlers). Fig. 2.73 shows the 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 67,\ 75,\ 80,\ 85,\ 90,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data in the frequency range of 67 to 110 GHz are within the gray shaded area. At an input power level of $P_{\text{in}} = 18$ dBm, the achieved output power levels are within the range of -5 to 3 dBm. A comparison of the measured conversion loss (solid lines) at $P_{\text{in}} = 14,\ 16,\ 18$ dBm with results from co-simulation (dashed lines) is given in Fig. 2.74.

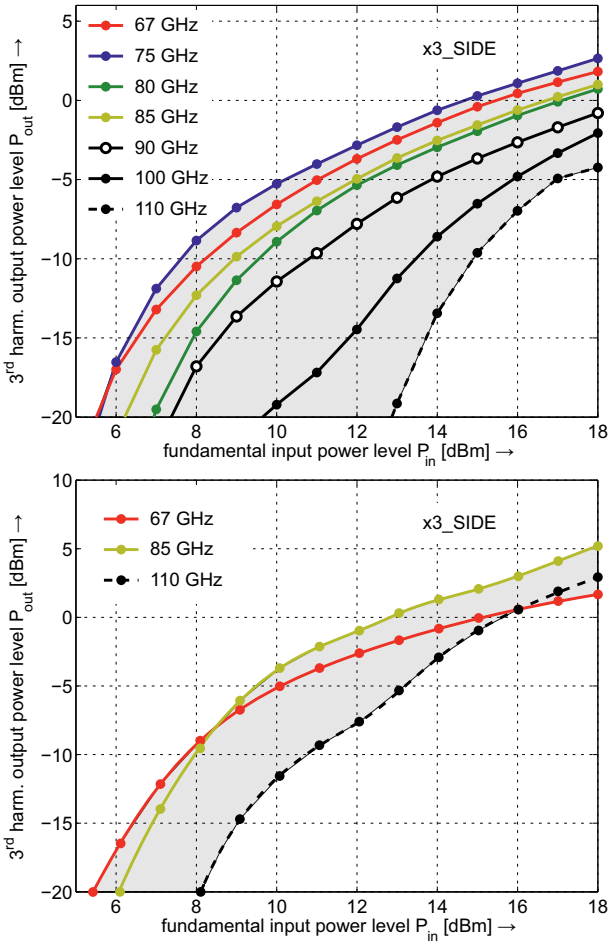

Figure 2.73: 3rd harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 67,\ 75,\ 80,\ 85,\ 90,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data (top) and simulation data (bottom) in the frequency range of 67 to 110 GHz are within the gray shaded area.

The conversion loss values are below 20 dB from 67 to 100 GHz and below 24 dB up to 110 GHz, which is 2 to 8 dB less output power

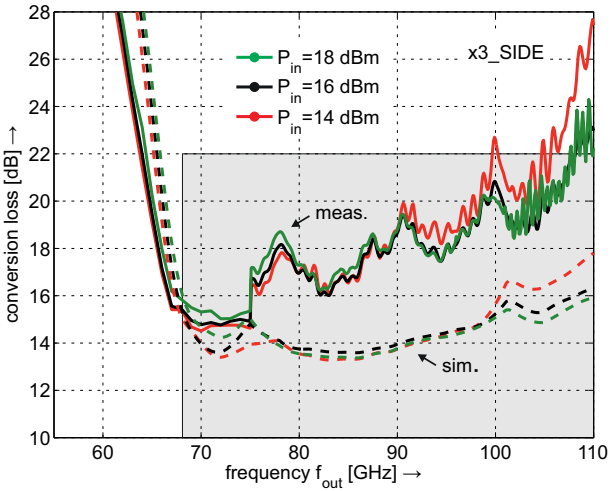

Figure 2.74: Comparison of measured (solid) and simulated (dashed) conversion loss versus output frequency f_{out}. Input power levels $P_{\mathrm{in}} = 14,\ 16,\ 18$ dBm.

than simulation results predict. Spectral measurements up to the 4^{th} harmonic have been performed. At $P_{\mathrm{in}} = 18$ dBm suppression of the 2^{nd} and 4^{th} harmonic is better than 20 dBc from 60 to 110 GHz (Fig. 2.75). The presented longitudinal E-field probe transition from MSL to WR-10 is designed to couple the x3_SIDE output signals to WR-10 waveguides.

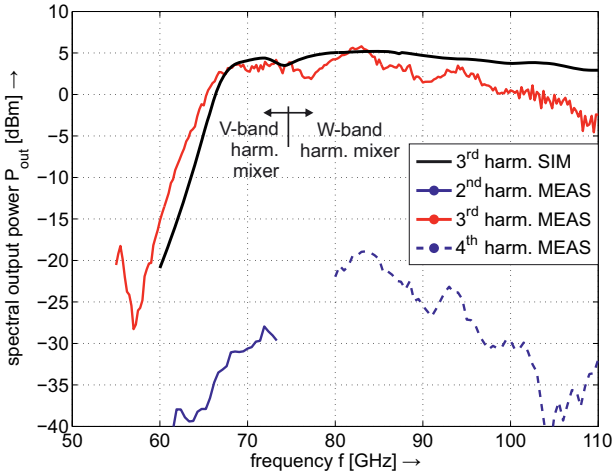

Figure 2.75: Measured spectral output power levels up to the 5^{th} harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 18$ dBm. Compared to simulated 3^{rd} harmonic output power levels with $P_{\text{in}} = 18$ dBm (black, solid).

2.6.4 Frequency Doubler x2_uFIN (#4)

Top and bottom view of the manufactured x2_uFIN (#4) frequency doubler Al_2O_3 substrates are shown in Fig. 2.76.

As already mentioned a minimum filter order of $N = 15$ is required for frequency doublers that cover an output frequency range of 60 to 110 GHz, establishing passband behaviour at the highest input frequency along with sufficient stopband rejection at the lowest output frequency. Within the applied dicing process the maximum substrate length of 6 mm does not allow for higher filter orders than $N = 11$. The achievable input and output frequency ranges are $f_{\text{in}} = [27.5, 53]$ GHz, $f_{\text{out}} = [53/55, 106]$ GHz, when using the presented LPF. The designed LPF will add up to 4 dB loss to a fundamental signal at 55 GHz, therefore efficiency at frequencies greater than 106 GHz is poor. Things are different at the lower end of the output frequency range. Fundamental signals at frequencies below 27.5 GHz pass the

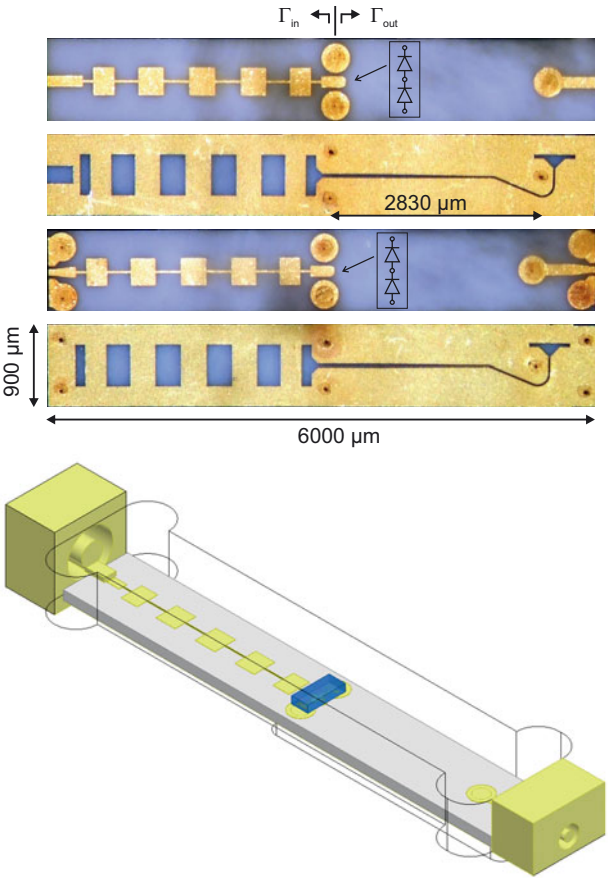

Figure 2.76: Top and bottom view of the manufactured x2_uFIN frequency doubler Al_2O_3 substrates (0.9 mm × 6.0 mm) and 3D model for coaxial interconnection.

LPF and generate harmonics at the Schottky junctions. Although, the amount of 2^{nd} harmonic power that propagates to the matched input port is lost, there is 2^{nd} harmonic power propagating in forward direction to the output load. This power splitting is rarely equal. Actually, it strongly depends on the frequency multiplier architecture

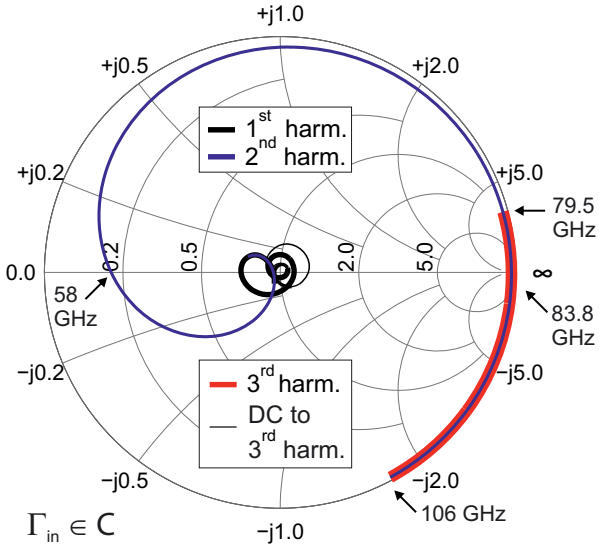

Figure 2.77: 3D EM simulated input impedances of x2_uFIN (including transition to 1.85 mm) provided to the diode junctions visualized in the Smith chart versus frequency. $\Gamma_{\text{in}} \in \mathbb{C}$.

and especially on the output circuitry. Therefore measurement results of x2_uFIN (this subsection) and x2_uFINring (subsection 2.6.5) cover the output frequency range of 50 to 110 GHz. The Smith chart in Fig. 2.77 shows the impedances provided by the LPF to the diode junctions including the diode mounting structure at the input, in case of frequency doubling (Γ_{in} in Fig. 2.76). The 1st harmonic is matched. Due to insufficient filter order the 2nd harmonic is not entirely reflected at the lower end of the output frequency range, but it is arranged around the ideal open circuit at 83.8 GHz at the higher output frequencies. The 3rd harmonic frequencies overlap with f_{out} and are rejected with open / inductive behaviour. The proposed frequency doubler x2_uFIN utilizes the cut-off behaviour of an uFIN with 30 µm slot as HPF. The same uFIN is used for frequency tripler x3_uFIN from subsection 2.6.2. It shows 98 Ω characteristic impedance at 50 GHz (Fig. 2.61). The two Schottky junctions are

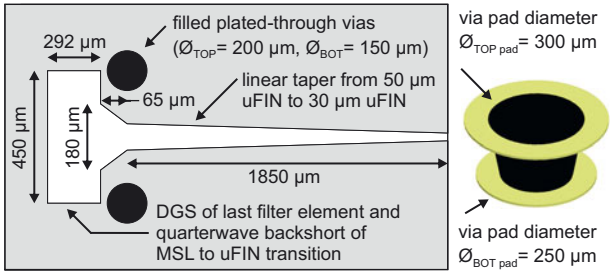

Figure 2.78: Detail view of the transition from x2_uFIN diode mounting structure to uFIN (bottom layer) waveguide.

driven in antiparallel configuration at the input and excite the hybrid finline mode at the output in phase. Both Schottky junctions are in series with the uFIN, which allows for propagation of generated even harmonics along the uFIN waveguide. A detail view of the transition from the diode mounting structure to uFIN is shown in Fig. 2.78. The DGS structure of the last LPF element is used as quarterwave backshort of the uFIN transition. The dimensions of the DGS are fixed, two linear tapers allow for adjusting the operating frequency of the backshort. The author successfully applied a similar approach to build D-band frequency doublers (section 2.7, [I7]) on PTFE with 50 µm thickness and WR-12 input and WR-6 output waveguide. The length of the finline (ℓ = 1850 µm) is chosen to achieve sufficient fundamental rejection (43 dB at 35 GHz) and to reduce reflections of the finline taper from 180 to 30 µm. At the output the uFIN to MSL transition from x3_uFIN (subsection 2.6.2) is used. As it is shown in Fig. 2.63 the transition has an operating frequency range from 48.5 to 110 GHz. Therefore the output circuitry is capable of covering the frequency range from 50 to 110 GHz, but the input LPF adds 3 dB to 4 dB additional loss at the maximum input frequency of 55 GHz (compare Fig. 2.47). With respect to the explanations about the applied co-simulation procedure in this section and subsection 2.6, multiplier x2_uFIN (#4) constitutes a multiplier architecture, which does not allow for extensive partitioning within the design process.

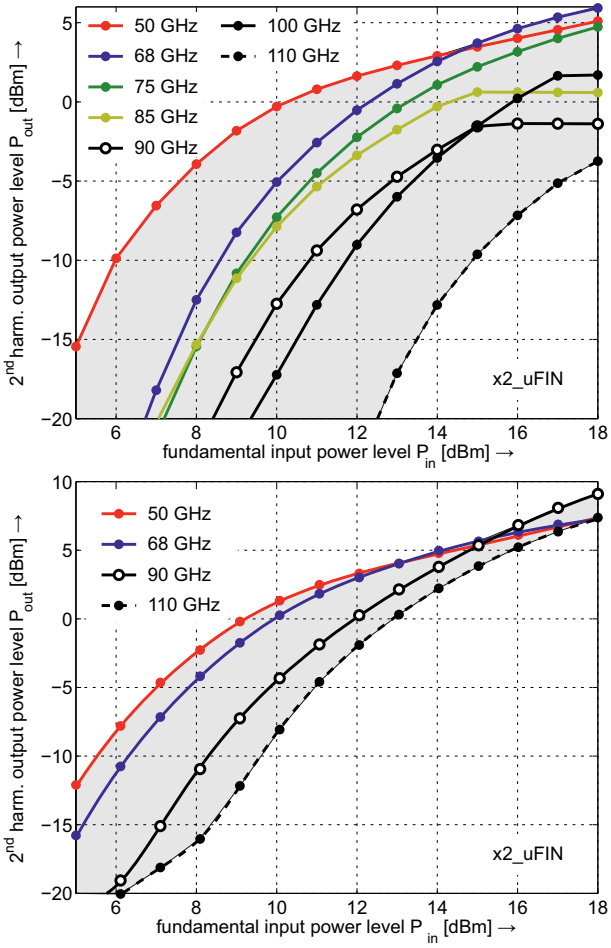

Figure 2.79: 2^{nd} harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 50,\ 68,\ 75,\ 85,\ 90,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data (top) and simulation data (bottom) in the frequency range of 50 to 110 GHz are within the gray shaded area.

The diode mounting structure in Fig. 2.78 strongly interacts with the last LPF elements and the tapered uFIN parts at the output.

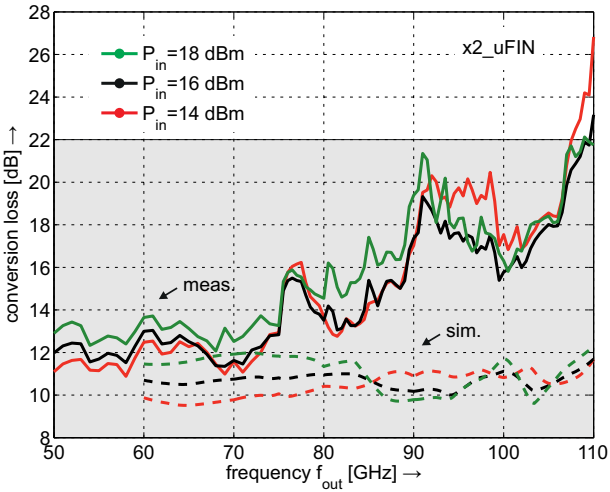

Figure 2.80: Comparison of measured (solid) and simulated (dashed) conversion loss versus output frequency f_{out}. Input power levels $P_{\mathrm{in}} = 14,\ 16,\ 18$ dBm.

Hence, individual optimization of these single parts is not possible. Fig. 2.79 shows the 2nd harmonic output power levels P_{out} at the output frequencies $f_{\mathrm{out}} = 50,\ 68,\ 75,\ 85,\ 90,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data in the frequency range of 50 to 110 GHz are within the gray shaded area. At an input power level of $P_{\mathrm{in}} = 18$ dBm, the achieved output power levels are within the range of -5 to 6 dBm. A comparison of the measured conversion loss (solid lines) at $P_{\mathrm{in}} = 14,\ 16,\ 18$ dBm with results from co-simulation (dashed lines) is given in Fig. 2.80. The conversion loss values are below 14 dB from 50 to 75 GHz (entire V-band) and below 23 dB up to 110 GHz, which is 2 to 10 dB less output power than simulation results predict. Spectral measurements up to the 3rd harmonic have been performed. In case of frequency doublers for the output frequency range of 50 to 110 GHz, the 3rd harmonic is the only harmonic overlapping with the desired output

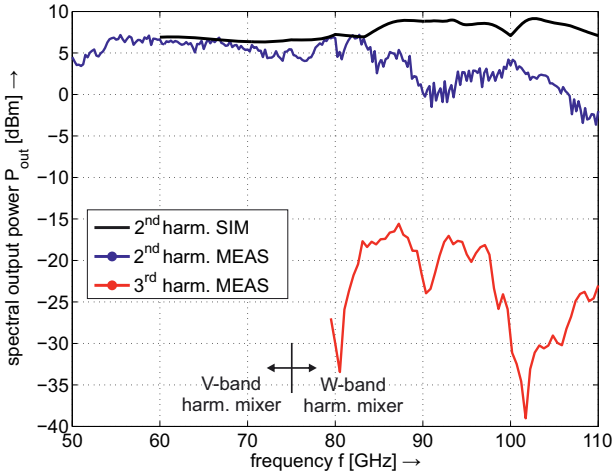

Figure 2.81: Measured spectral output power levels up to the 4th harmonic versus output frequency f_{out} at input power level $P_{in} = 18$ dBm. Compared to simulated 3rd harmonic output power levels with $P_{in} = 18$ dBm (black, solid).

signal. At $P_{in} = 18$ dBm suppression of the 3rd harmonic is better than 15 dBc (Fig. 2.81).

2.6.5 Frequency Doubler x2_uFINring (#5)

Top and bottom view of the manufactured x2_uFINring (#5) frequency doubler Al_2O_3 substrates are shown in Fig. 2.82. The explanations regarding the utilized LPF for frequency doublers from subsection 2.6.4 hold true for x2_uFINring. The fundamental signal exits the LPF in MSL mode. Through a filled plated-through via ($\varnothing_{TOP} = 200$ µm), the signal enters a coplanar waveguide (CPW) at the bottom layer. In CPW mode the two Schottky junctions are driven in antiparallel configuration. A detail view of the transition is shown in Fig. 2.83. The 2nd harmonic at each Schottky junction excites uFIN modes (slot width 30 µm) in forward and backward direction. In backward direction, the two uFIN waves with opposite

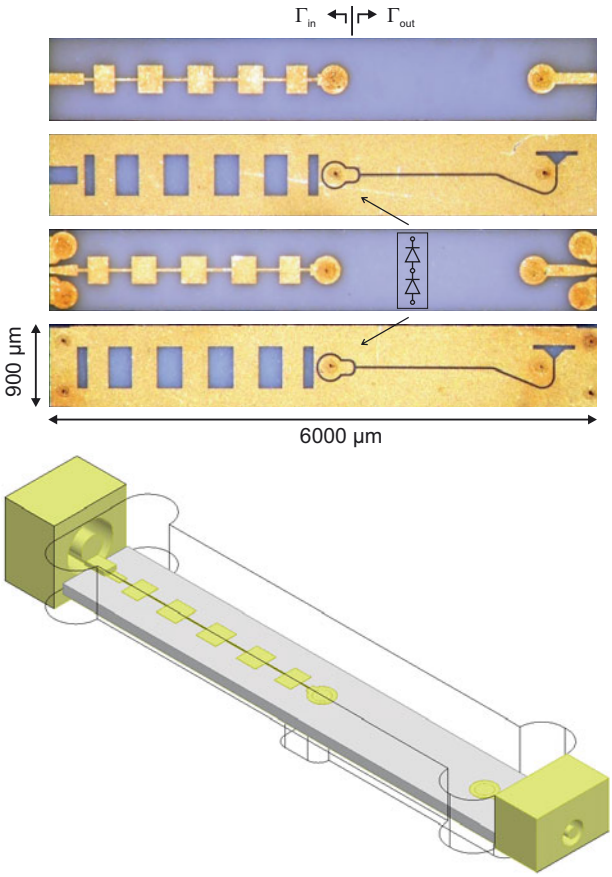

Figure 2.82: Top and bottom view of the manufactured x2_uFINring frequency doubler Al_2O_3 substrates (0.9 mm × 6.0 mm) and 3D model for coaxial interconnection.

phases propagate along the ring structure of Fig. 2.83, building a virtual ground behind the signal via. The distance from the diode junctions to the virtual ground is approximately a quarterwave length long to establish open circuit behaviour at the diode junctions. This ring structure was first introduced in [68] and modified in [69] to build single balanced mixers with RF frequency range of 40 to 70 GHz.

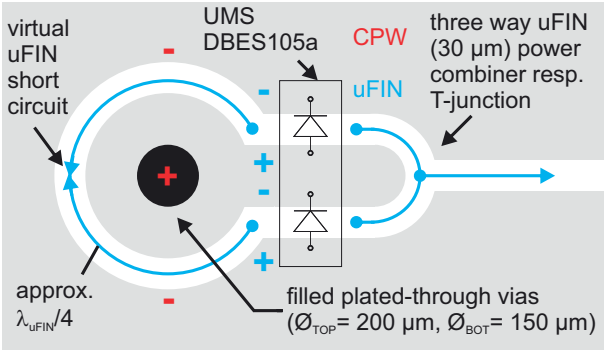

Figure 2.83: Detail view of the transition from x2_uFINring diode mounting structure to uFIN (bottom layer) waveguide.

The virtual ground already provides isolation between the input and output port, but the LPF is still needed to establish well-defined back reflection of the parasitic 2nd and 4th harmonic propagating in CPW mode. An uFIN three way power combiner allows for combination of both uFIN waves in forward direction. At the output the transition from uFIN to MSL of multiplier #2 from subsection 2.6.2 is used. The multiplier assembly procedure described in the beginning of this section has been used to assemble multiplier #1 to #4. In case of x2_uFINring the DBES105a diode is located at the bottom layer. Hence, if conventional solder paste (62Sn-36Pb-2Ag) is used for diode assembly to the substrate, conductive adhesive or low-melting solder based on In or Bi has to be used for assembly of substrate with diode to the Au-plated brass housing. Otherwise the diode solder connection would become affected. The low-melting solder pastes come with improved wettability, but lower electrical conductivity (compare Table 2.4). The author experienced problems with several assemblies, if low-melting solder paste interacts with conventional tin-based solder or soldering flux residues. Optical inspections of the soldered connections show discontinuous points and the joints are prone to cracking. As the contact area between Al_2O_3 substrate and mechanical housing is quite small, sufficient cleaning can hardly be done. The utilized

uFIN is a single conductor waveguide and very sensitive to failures of solder connections between substrate metallization and housing. As a result, conversion loss peaks occur at some output frequencies. As already outlined the diode pads of DBES105a are equipped with Au bumps, that allow for thermo-sonic bonding assembly, to overcome the aforementioned problems with low-melting solder paste. Therefore, the author decided to use thermo-sonic diode bonding and conventional solder paste to mount the substrate with diode to the housing. Fig. 2.84 shows the 2^{nd} harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 50,\ 60,\ 70,\ 80,\ 95,\ 105,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data in the frequency range of 50 to 110 GHz are within the gray shaded area. At an input power level of $P_{\text{in}} = 18$ dBm, the achieved output power levels are within the range of -3.4 to 6.8 dBm. A comparison of the measured conversion loss (solid lines) at $P_{\text{in}} = 14,\ 16,\ 18$ dBm with results from co-simulation (dashed lines) is given in Fig. 2.85. The conversion loss values are below 15 dB from 50 to 89 GHz and below 22 dB from 50 to 110 GHz. Spectral measurements up to the 3^{rd} harmonic have been performed. At $P_{\text{in}} = 18$ dBm suppression of the 3^{rd} harmonic is better than 15 dBc (Fig. 2.86).

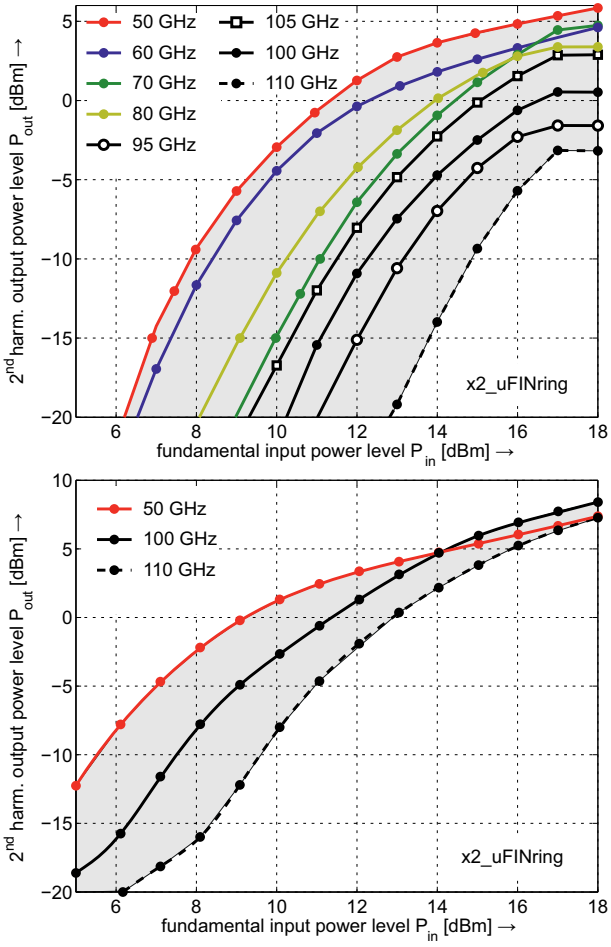

Figure 2.84: 2^{nd} harmonic output power levels P_{out} at the output frequencies $f_{\text{out}} = 50,\ 60,\ 70,\ 80,\ 95,\ 105,\ 100,\ 110$ GHz versus the fundamental input power level P_{in}. Measurement data (top) and simulation data (bottom) in the frequency range of 50 to 110 GHz are within the gray shaded area.

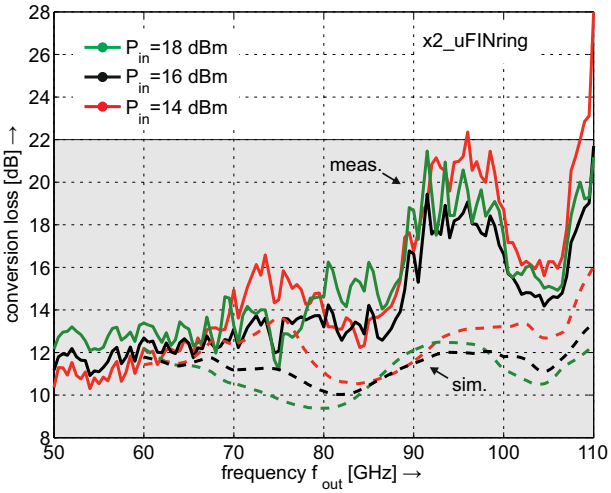

Figure 2.85: Comparison of measured (solid) and simulated (dashed) conversion loss versus output frequency f_{out}. Input power levels $P_{\text{in}} = 14,\ 16,\ 18$ dBm.

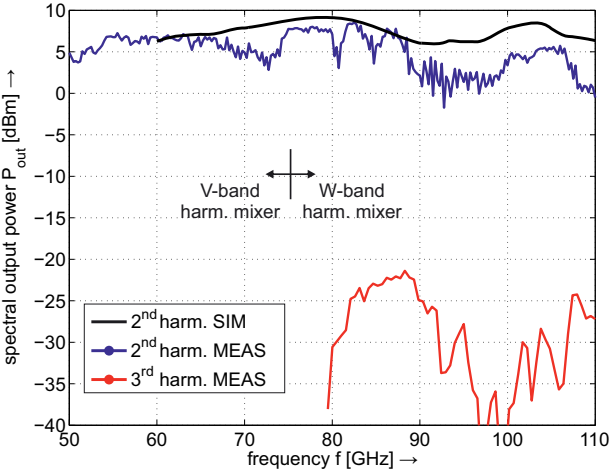

Figure 2.86: Measured spectral output power levels up to the 4^{th} harmonic versus output frequency f_{out} at input power level $P_{\text{in}} = 18$ dBm. Compared to simulated 3^{rd} harmonic output power levels with $P_{\text{in}} = 18$ dBm (black, solid).

Comparison and Conclusion Fig. 2.87 compares the measured output power levels P_{out} versus output frequency f_{out} at an input drive level of 18 dBm of the proposed multipliers (#1 to #5). Obviously, the frequency tripler x3_HE$_1$, frequency doublers x2_uFIN and x2_uFINring cover the largest bandwidth with the best efficiency. Conversion loss values around 18 dB from 60 to 95 GHz and below 22 dB from 60 to 110 GHz are achieved with frequency tripler #1. Frequency doubler #4 achieves conversion loss values below 16 dB from 50 to 88 GHz and below 23 dB from 50 to 110 GHz. Frequency doubler #5 operates with conversion loss values below 15 dB from 50 to 89 GHz and below 22 dB from 50 to 110 GHz. The signal generators, available for characterization, restrict the input power level to a maximum of $P_{\text{in}} = 18$ dBm[43]. As it can be seen from Fig. 2.57, Fig. 2.65, Fig. 2.73, Fig. 2.79, and Fig. 2.84 the multipliers are not entirely saturated at $P_{\text{in}} = 18$ dBm. Hence, for applications where maximum output power instead of best efficiency is preferred, the reported maximum output power levels can be increased with $P_{\text{in}} > 18$ dBm.

The presented measurement data in subsection 2.6.1 to subsection 2.6.5 deviate from the predicted co-simulation results. The main reasons for deviations are the applied Schottky junction modelling and underestimation of dielectric and conductor loss. Furthermore, the influence of the coaxial connectors is not entirely included within simulations. More sophisticated Schottky junction modelling approaches have been reported [53], but can hardly be utilized with commercial diodes due to insufficient information about material and geometry parameters of the diode.

A comprehensive comparison of the proposed frequency multipliers with reported work is given in Table 2.6. There are only a few reported multipliers [44, 70] that operate over comparable fractional bandwidths as the proposed multipliers (column four of Table 2.6). The reader should keep in mind the results of MIC multipliers are

[43] In fact, the actual generator output power level of the driving signal generator is lower than assumed (18 dBm). Hence, the measured conversion loss values of the proposed multipliers are slightly better than it is shown.

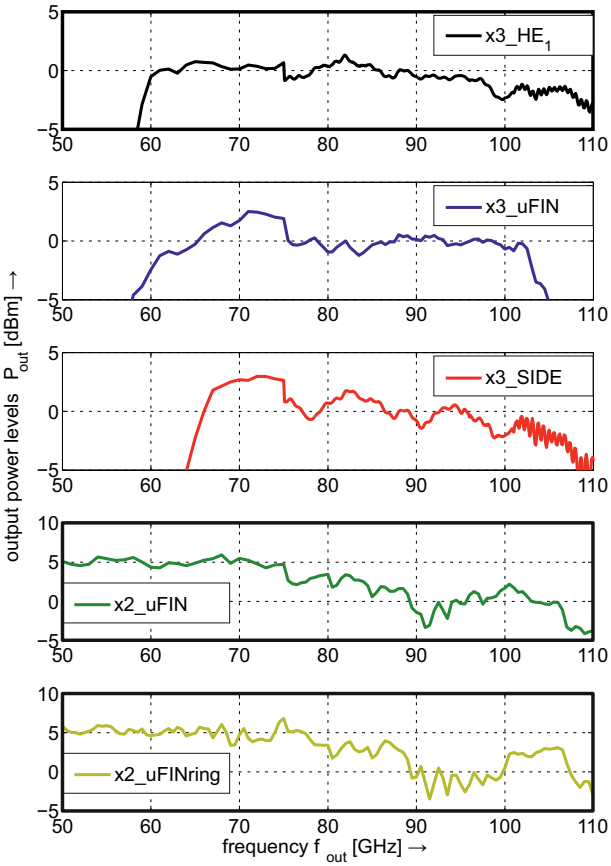

Figure 2.87: Comparison of the measured output power levels versus output frequency of the proposed multipliers (#1 to #5) with an input drive level of 18 dBm.

from on-wafer measurements of the bare die and not from a fully connectorized module, as it is with the proposed multipliers. The necessary interconnect solutions add loss at the in- and output. Considering this fact, the proposed multipliers achieve similar conversion loss values compared to MIC multipliers, but operate over greater bandwidth. Consequently, the actually necessary input power level

P_{in} of an MIC multiplier within front end modules is higher than indicated in Table 2.6.

In this section, innovative planar frequency multiplier designs dedicated to system design of VNA and signal generator frequency extension modules, as well as front end modules of ATS are presented. For cost reasons, it is preferred to manufacture the planar devices required for these modules on a single ceramic wafer with a certain set of design rules. Furthermore, restrictions from the mechanical housing and the intended level of integration make it necessary to individually choose the right multiplier architecture for a certain module. For example, multiplier #2, #4, and #5 can be directly connected to other uFIN components, if manufactured without the transition to MSL at the output, whereas multiplier #1 and #3 are best used with other MSL components.

The proposed frequency multipliers are based on cost effective commercially available GaAs Schottky diodes and conventional thin-film technology for high permittivity 5 mil Al_2O_3 instead of expensive, fragile SiO_2. The balanced multipliers do not require DC biasing or ferrite absorber material. Adequate operation is fully defined by the planar structure. Requirements on the mechanical housing are moderate, and the frequency responses are flat enough to be handled by automatic level control loops. In conjunction with commercial gallium nitride (GaN), indium phosphide (InP) or GaAs power amplifiers the achieved broadband operation and efficiency of the proposed hybrid frequency multipliers are highly suitable for the aforementioned fields of application. The presented planar architectures are not restricted to the focussed frequency ranges and substrate material Al_2O_3. In combination with appropriate THz diodes and reduced substrate dimensions, the designs are promising candidates for higher operating frequencies.

Table 2.6: Comprehensive Comparison of Reported Frequency Multipliers

references		output freq. range [GHz]	FBW [%]	diode process	mult. fact.	recom. P_{in} [dBm]	conv. loss min/max [dB]	P_{outmax} [dBm]	bias	size [mm]
[71]	m	87 to 102	16	TRW 0.15 µm GaAs pHEMT*	3	10 to 16	18/20	< -3	no	1.5/1
[43]	m	75 to 110	38	UMS BES GaAs Schottky diode*	3	10 to 18	17.2/20.6	< 3	yes	2/0.74/0.1
[44]	m	60 to 110	**59**	WIN 0.15 µm GaAs mHEMT*	3	15	13.2/20	< 5	no	1/1
[72]	h	93 to 99	6	WIN 0.15 µm GaAs pHEMT*	3	5	19/23	< -10	yes	2.5/1.5
[73]	m	94 to 100	6	0.25 µm GaAs pHEMT	3	–	–	5.5	yes	1.5/1.5
[74]	m	90 to 100	11	InAlGaAs/InP HBV$^\diamond$	3	20 to 26	7.4/17	19.3	no	n/a
[75]	m	67.5 to 84	22	0.15 µm GaAs pHEMT	3	10	4.3/7	7.5	yes	1/1.5
[45]	m	72 to 90	22	GaAs Schottky diode*	3	13	18.5/21.2	< -5	no	1.1/1.4/0.1
[76]	h	75 to 110	38	n/a*	3	16	24$^\bullet$	n/a	no	19.1/19.1/25.4
[77]	h	70 to 110	44	n/a*	3	18 to 25	13/15	n/a	no	25.4/25.4/20.3
[50–52]	m	75 to 100	29	0.13 µm GaAs pHEMT*	2	13	$-3/2$	15	yes	2.25/3
[46–49]	m	70 to 78	11	GaAs Schottky diode$^\diamond$	2	10 to 27	5.3/8.6	> 15	yes	$1.97^\circ/2.6^\circ$
[46–49]	m	70 to 79	12	GaAs Schottky diode$^\diamond$	2	10 to 27	4.4/7.3	> 15	yes	$1.97^\circ/2.6^\circ$
[70]	m	50 to 128	**88**	WIN 0.15 µm GaAs pHEMT*	2	12.5	12.5/15	-2.5	no	0.56/0.42
[75]	m	67 to 84	23	0.15 µm GaAs pHEMT	2	16	4/13	10	yes	n/a
[78]	h	94 to 116	21	GaAs Schottky diode*	2	7 to 13	15.2/23	-2.2	no	n/a
[79]	h	64 to 78	20	JPL GaAs Schottky diode$^\diamond$	2	23 to 27	8.4/12	> 18.5	yes	n/a
[80]	h	75 to 110	38	n/a*	2	16	22$^\bullet$	n/a	no	28.6/28.6/15.2
[81]	h	75 to 110	38	n/a*	2	24 to 27	9.6/11.6	n/a	yes	30.5/30.5/20.3
Fig. 2.58 (#1)	h	60 to 110	**59**	UMS BES GaAs Schottky diode*	3	≥ 12	16/22	< 1	no	0.9/6/0.14
Fig. 2.66 (#2)	h	60 to 110	**59**	UMS BES GaAs Schottky diode*	3	≥ 12	15/27	< 2	no	0.9/6/0.14
Fig. 2.74 (#3)	h	67 to 110	**49**	UMS BES GaAs Schottky diode*	3	≥ 14	15/24	< 2	no	0.9/6/0.14
Fig. 2.80 (#4)	h	50 to 110	**75**	UMS BES GaAs Schottky diode*	2	≥ 14	11/23	< 5	no	0.9/6/0.14
Fig. 2.85 (#5)	h	50 to 110	**75**	UMS BES GaAs Schottky diode*	2	≥ 14	11/22	< 6.8	no	0.9/6/0.14

Min. and max. conversion loss values do not necessarily correspond to the same input power level as in the case of the max. output power level P_{outmax}. $\star$ / $\diamond$ = Varistor / Varactor mode. m / h = monolithic / hybrid realization. $\circ$ Estimated from die photography in [46]. $\bullet$ Typical values from datasheet.

2.7 D-Band Frequency Doubler and Y-Band Frequency Tripler

The presented frequency multipliers for 50 / 60 to 110 GHz of the preceding section are based on the UMS DBES105a diode. The physical dimensions of this discrete diode, especially the distance of both Schottky junctions, do not suggest operation at frequencies above 110 GHz[44]. Anyway, frequency multipliers for D-band and Y-band frequency ranges based on the DBES105a diode are valuable for extending the frequency range of cost driven industrial radar modules. At the expense of conversion loss performance, these millimeter-wave components are built up at very low cost utilizing PCB processing.

This section describes a zero bias D-band frequency doubler and Y-band frequency tripler based on pure PTFE material, split block construction and the DBES105a diode. At an input drive level range of 16 to 18 dBm the multipliers [I7] deliver output power levels $P_{\text{out}} \in [-5, 5]$ dBm from 100 to 160 GHz and $P_{\text{out}} \in [-20, -11]$ dBm from 180 to 230 GHz. As an outlook, further innovative multiplier designs are shown. Several transitions from planar waveguide to rectangular waveguides and the analytical design procedure of Dolph-Chebyshev tapers (subsection 2.7.1) are presented. A brief uncertainty analysis of spectral measurements with harmonic mixers in front of spectrum analyzers is given in subsection 2.7.2.

Introduction, Manufacturing and Assembly Successful planar Schottky diode frequency multipliers for D-band (110 to 170 GHz) and Y-band (170 to 260 GHz) output frequency ranges have been reported. These are hybrid circuits using thin SiO_2 substrates with proprietary discrete diodes or monolithic millimeter-wave integrated circuits (MMICs). Industrial short-range radar modules for various applications like distance or liquid level measurements and material

[44] The single Schottky junction of UMS DBES105a performs well up to 300 GHz and beyond. In [38], page 104, a single junction of the discrete diode is singularized in a further dicing step and used for a power detector design. In [82], a 150 to 151 GHz frequency doubler utilizing DBES105a diodes is presented.

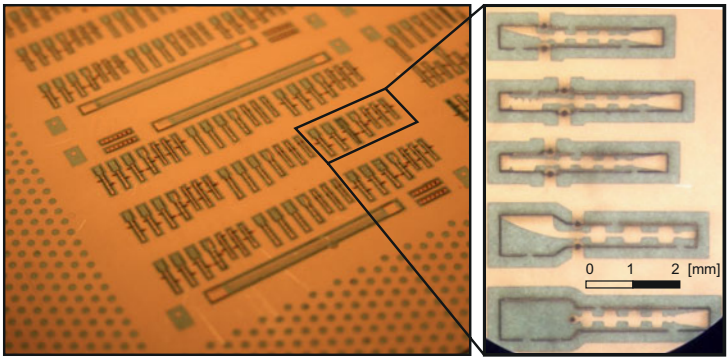

Figure 2.88: Photograph of manufactured Fastfilm 27 laminate with close up view of the proposed frequency multipliers.

parameter monitoring are narrow band, highly integrated and therefore bound to a certain technology. Frequency extension of existing modules utilizing cost effective PCB technology requires millimeter-wave frequency multipliers based on the same technology. Although the aforementioned radar modules operate at fractional bandwidths below 10 %, it is desirable to develop broadband multipliers that can be used within many different modules. Broadband cost effective D- and Y-band multipliers are further interesting for several imaging applications, where many multipliers arranged in an array are required.

The proposed multipliers are built on pure PTFE material (Fastfilm 27 from Taconic Farms, Inc.) with thickness of 50 µm and 17 µm copper cladding, processed by commercially available PCB technology. To improve lateral displacement between top and bottom layer etching, the entire PCB panel (430 × 260) mm^2 is partitioned into smaller regions (60 × 60) mm^2 that are equipped with individual alignment marks. Fig. 2.88 illustrates such a partition and close up view of the proposed multipliers.

D-Band Frequency Doubler In compliance with these design rules, an input lowpass filter (LPF) of 9^{th} order with cut-off frequency

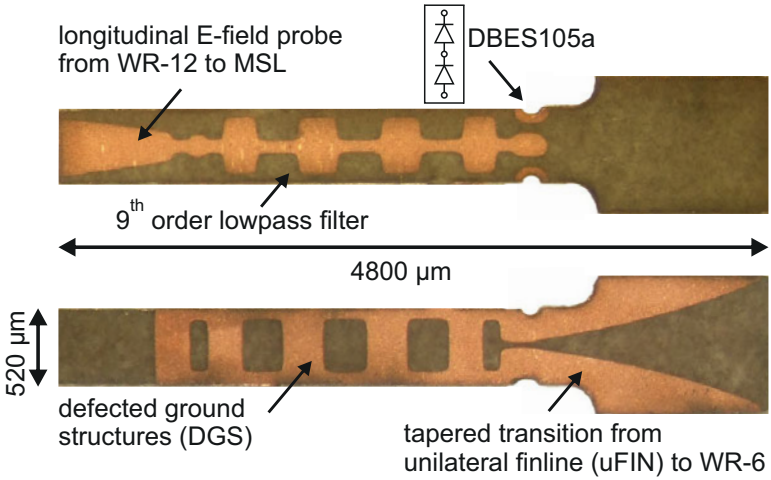

Figure 2.89: Photographs of top and bottom layer of the proposed D-band (WR-6) frequency doubler.

Table 2.7: 9^{th} order stepped impedance MSL lowpass filter

filter elements	strip widths [µm]	lengths [µm]	inductance and capacitance values at f_c
1 and 9	75	128	5.75 pH
2 and 8	370	216	42.26 fF
3 and 7	75	283	12.72 pH
4 and 6	370	259	50.67 fF
5	75	299	13.44 pH

filter order $N = 9$, cut-off frequency $f_{c\,1\,dB} = 90.7$ GHz,
$f_{c\,3\,dB} = 94$ GHz, passband ripple $r_{dB} = 0.01$ dB,
stopband rejection of 25 dB at $1.2 \times f_{c\,3\,dB}$.

$f_{c\,1\,dB} = 91$ GHz and passband ripple of 0.01 dB has been designed. Table 2.7 summarizes the filter parameters.

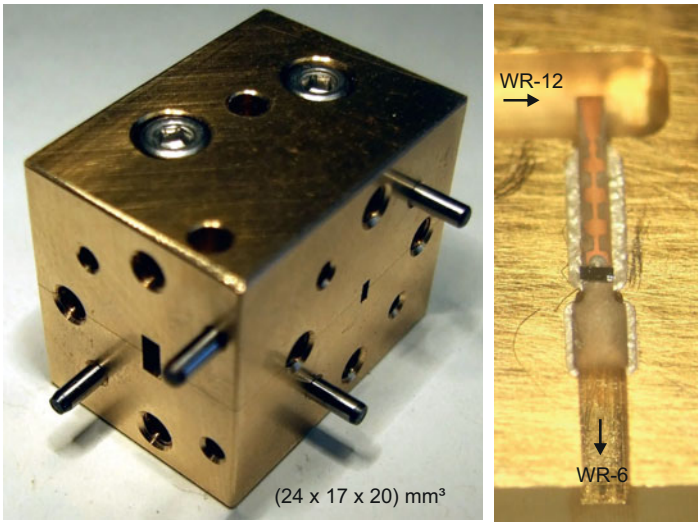

Figure 2.90: Photographs of mechanical housing and laminate assembly of the proposed D-band (WR-6) frequency doubler.

To achieve the required inductance values, the high impedance LPF sections are equipped with defected ground structures (DGS). The first and last filter elements are inductive to ensure open circuit stopband behavior for the 2nd harmonic output signal at the input. Cross-sectional views of the low (C) and high (L) impedance MSL, magnitude of the electric field strengths at 95 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{MSL}})$ of 50 Ω MSL, high and low MSL are given in Fig. 2.91. Simulation results of Fig. 2.92 predict 20 dB rejection at 110 GHz.

In cascade to the LPF, the DBES105a diode with two Schottky junctions in series tee configuration is soldered to PTFE laminate at the position indicated in Fig. 2.89. The generated 2nd harmonic signal excites an unilateral finline (uFIN) mode (bottom layer) that exits the planar circuit by a tapered transition to WR-6 waveguide. The last filter DGS structure serves as quarterwave backshort of the MSL to uFIN transition.

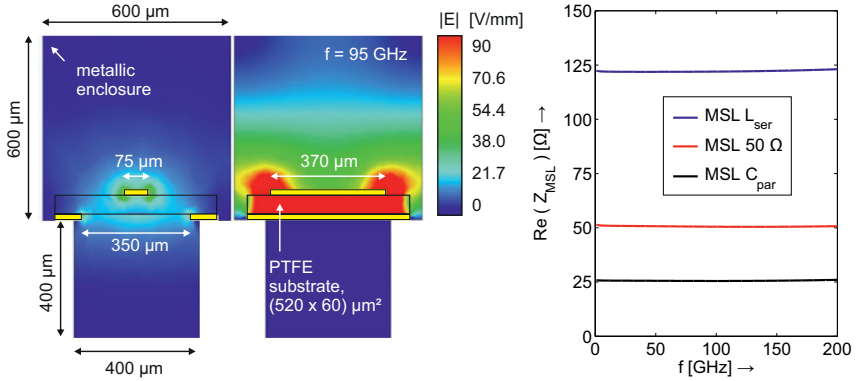

Figure 2.91: Cross-sectional views of the low (C) and high (L) impedance MSL, magnitude of the electric field strengths at 95 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{MSL}})$ of 50 Ω MSL, high and low MSL versus frequency. $\mathrm{Re}\,(Z_{\mathrm{MSL-L}}) = 121.98\ \Omega, \mathrm{Re}\,(Z_{\mathrm{MSL-C}}) = 25.5\ \Omega$ and the corresponding effective permittivities are $\epsilon_{\mathrm{reff-L}} = 1.49, \epsilon_{\mathrm{reff-C}} = 2.24$ at $f = 95$ GHz.

A cross-sectional view of the uFIN, magnitude of the electric field strengths at 170 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{uFIN}})$ of the first three hybrid modes are shown in Fig. 2.93. The taper contour of the transition from uFIN to WR-6 waveguide follows the Dolph-Chebyshev function, as it is outlined in subsection 2.7.1. Fig. 2.94 includes simulated scattering parameters, which also show propagation of the next higher order TE_{20} like mode. The higher order unilateral finline modes, which have even lower cut-off frequencies according to Fig. 2.93 are not excited by the transition. The milled channel of the MSL part ensure mono mode operation across the full D-band.

Fig. 2.95 shows the measured input P_{in} (red) and output power levels P_{out} versus input f_{in} (red) and output frequencies f_{out}. Precise scalar P_{out} measurements have been performed with VDI Erickson PM4 calorimeter (black) according to the procedure outlined in [83]. Scalar power measurements do not allow for distinguishing spectral components of the harmonic content.

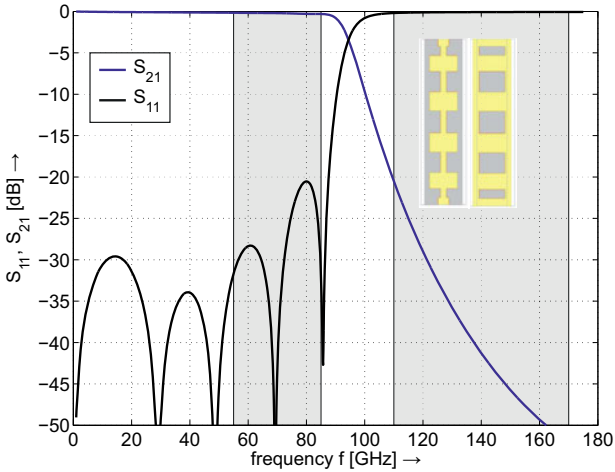

Figure 2.92: Simulated transmission (blue) and reflection coefficient (black) of the 9th order stepped impedance MSL lowpass filter versus frequency.

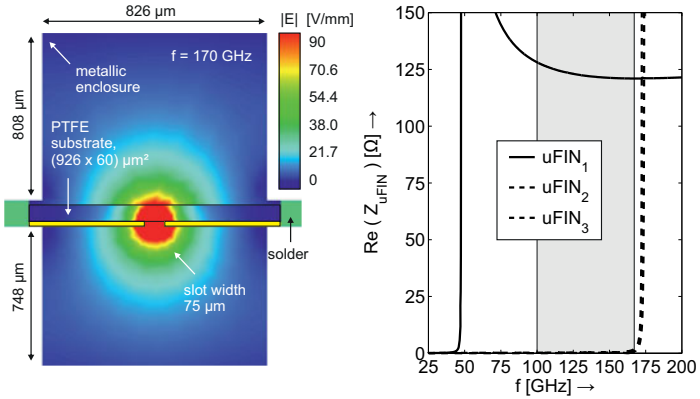

Figure 2.93: Cross-sectional view of the unilateral finline, magnitude of the electric field strengths at 170 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{uFIN}})$ of the first three hybrid modes versus frequency.

Harmonic mixer measurements (blue) with rather poor accuracy[45] (at least 6 dBm, subsection 2.7.2) have been applied to verify the

[45] The accuracy of harmonic mixer measurements is drastically decreased if the device under test is poorly matched, which is the case with the proposed multi-

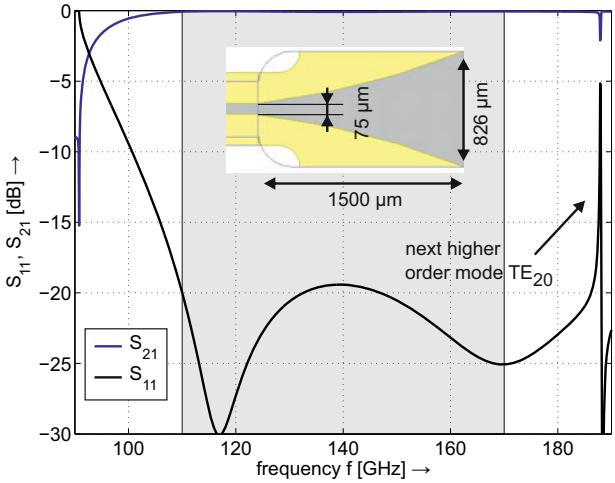

Figure 2.94: Simulated transmission (blue) and reflection coefficients (black) of the tapered (Dolph-Chebyshev) transition from unilateral finline (uFIN) to WR-6 versus frequency.

calorimetric measurements consider the envisaged spectral component (2^{nd} harmonic).

The gray shaded area in Fig. 2.95 indicates the frequency range with sufficient input power level. An input power level of 16 dBm could be provided up to 65 GHz by commercial signal generator. From 65 to 81 GHz an amplified[46] E-band source with power levels from 16 to 19 dBm has been used in the test setup. The black curve in Fig. 2.95 without dots show P_{out} results from the synthesis procedure, that correspond to a constant input power level of 18 dBm. The measurement results are not corrected for insertion loss of interconnecting waveguides at the output port. The calorimetric P_{out} measurements of the D-Band doubler illustrate multiplier operation with 15 to 20 dB conversion loss from 100 to 160 GHz, which means output power levels in the range of -5 to 5 dBm. Considering the already mentioned

pliers. Coarse conversion loss versus frequency look-up tables and deviations from the required LO power level are further sources of errors.

[46] Amplifier RPG E-MPA-65-85-24-20 from Radiometer Physics GmbH.

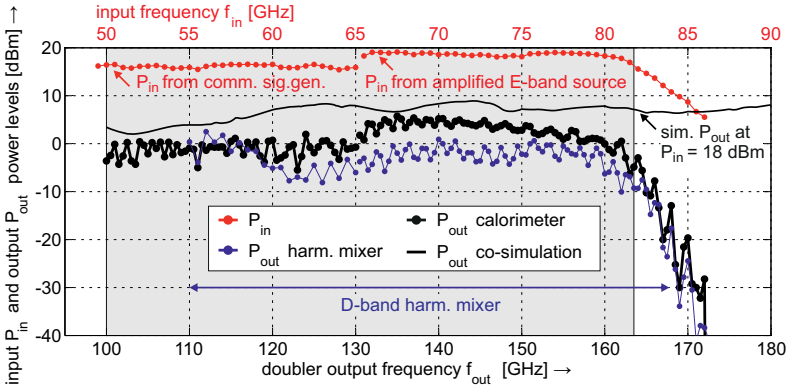

Figure 2.95: Measured input P_{in} (red) and output power levels P_{out} (black, blue) versus input f_{in} (red) and output frequencies f_{out} (black) of the proposed D-band (WR-6) frequency doubler.

problems with PCB manufacturing technology, this is in reasonable agreement to the predicted conversion loss of 10 to 15 dB. Due to insufficient input power levels no statement can be made about the doubler's performance above 160 GHz.

Y-Band Frequency Tripler The input signal of the Y-band frequency tripler of Fig. 2.96 and Fig. 2.97 enters a 7^{th} order lowpass filter (LPF) with cut-off frequency $f_{\text{c}\,1\,\text{dB}} = 109$ GHz and passband ripple of 0.01 dB. Table 2.8 summarizes the filter parameters.

The first and last filter elements are inductive to ensure open circuit stopband behavior for the 3^{rd} harmonic output signal at the input. Cross-sectional views of the low (C) and high (L) impedance MSL, magnitude of the electric field strengths at 116 GHz and real parts of the characteristic impedances $\text{Re}\,(Z_{\text{MSL}})$ of 50 Ω MSL, high and low MSL are given in Fig. 2.98.

To achieve the required inductance values and bandwidth of stopband, the high impedance LPF sections are equipped with defected ground structures (DGS). Simulated scattering parameters of the filter are shown in Fig. 2.99. Greater than 25 dB rejection is predicted at

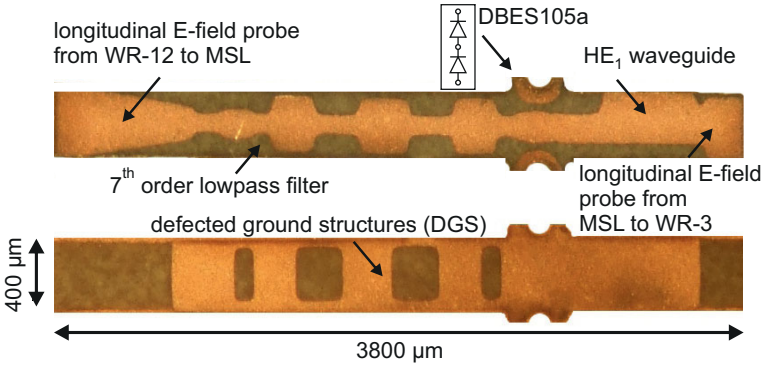

Figure 2.96: Photographs of top and bottom layer of the proposed Y-band frequency tripler with WR-3 interface.

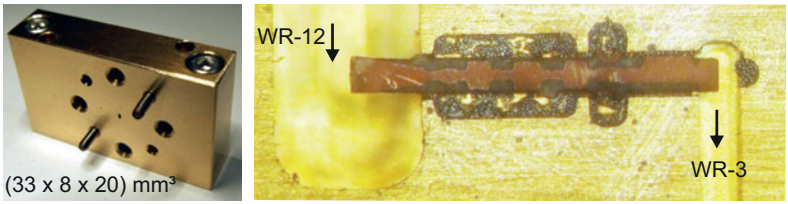

Figure 2.97: Photographs of mechanical housing and laminate assembly of the proposed Y-band frequency tripler with WR-3 interface.

170 GHz. The dashed curve corresponds to the filter's transmission coefficient without utilization of DGS technique. Less bandwidth of stopband and a second passband at 250 GHz are visible.

In cascade to the LPF, the DBES105a diode with two Schottky junctions in series tee configuration is soldered to PTFE laminate at the position indicated in Fig. 2.96. The generated 3rd harmonic signal of the Y-band multiplier propagates along a HE_1 waveguide [60], which acts as a highpass filter (HPF). Fig. 2.100 illustrates a cross-sectional view of the HE_1 waveguide, magnitude of the electric field strengths at 240 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{HE}})$ of the first two hybrid modes. Mono mode operation across Y-band (170 to 260 GHz) is achieved. A compromise between fundamental signal

Table 2.8: 7^{th} order stepped impedance MSL lowpass filter

filter elements	strip widths [µm]	lengths [µm]	inductance and capacitance values at f_c
1 and 7	75	120	5.02 pH
2 and 6	280	220	35.71 fF
3 and 5	75	263	11.01 pH
4	280	258	41.88 fF

filter order $N = 7$, cut-off frequency $f_{c\,1\,\text{dB}} = 109$ GHz,
$f_{c\,3\,\text{dB}} = 116$ GHz, passband ripple $r_{\text{dB}} = 0.01$ dB,
stopband rejection of 15 dB at $1.2 \times f_{c\,3\,\text{dB}}$.

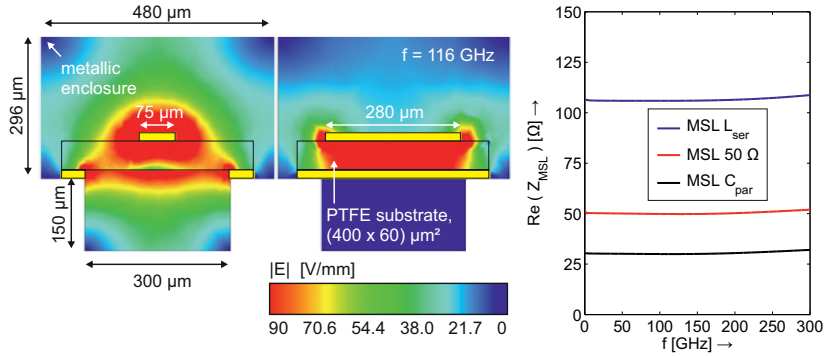

Figure 2.98: Cross-sectional views of the low (C) and high (L) impedance MSL, magnitude of the electric field strengths at 116 GHz and real parts of the characteristic impedances $\text{Re}\,(Z_{\text{MSL}})$ of 50 Ω MSL, high and low MSL versus frequency. $\text{Re}\,(Z_{\text{MSL}-\text{L}}) = 105.91\ \Omega, \text{Re}\,(Z_{\text{MSL}-\text{C}}) = 29.97\ \Omega$ and the corresponding effective permittivities are $\epsilon_{\text{reff}-\text{L}} = 1.49, \epsilon_{\text{reff}-\text{C}} = 2.13$ at $f = 116$ GHz.

rejection and additional insertion loss caused by HE_1 propagation is found by an HE_1 waveguide length of 0.5 mm. The solid curves in Fig. 2.101 correspond to simulation results of the highpass filter. Using the design procedure for distributed LPF based on quarterwave

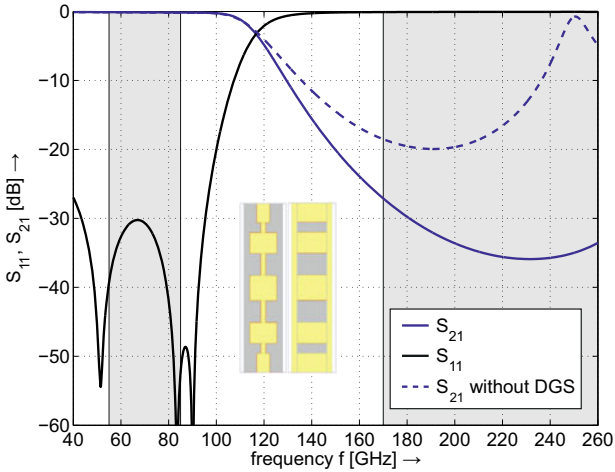

Figure 2.99: Simulated transmission (blue) and reflection coefficient (black) of the 7th order stepped impedance MSL lowpass filter versus frequency. The dashed curve corresponds to a filter design without defected ground structures.

prototypes from the appendix A, a notch LPF is developed. It is based on uFIN notches placed in quarterwave distance [84, 85] and constitutes an idler circuit for the 5th harmonic. The filter integration leads to an unintended altering of the HE_1 waveguide, which shifts the cut-off frequency to higher frequencies and therefore limits the operational bandwidth of the tripler (dashed curves in Fig. 2.101). A manufactured tripler using the integrated notch LPF is illustrated in the outlook of this section (Fig. 2.108).

The HE_1 waveguide is coupled to a WR-3 longitudinal E-field probe by a short section of 50 Ω MSL. Simulation results of the E-field probe are shown in Fig. 2.102. The milled channel of the Y-band MSL ensures mono mode operation up to 250 GHz (part of Y-band) only. Hence, the next higher order mode of the MSL channel restricts the output bandwidth of the tripler (180 to 270 GHz) and not the next higher order mode TE_{20} of the waveguide, which is also visible in Fig. 2.102 at about 345 GHz. Although Y-band frequency range

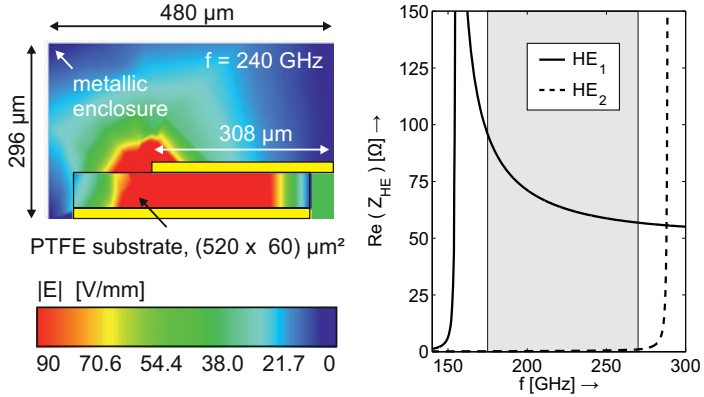

Figure 2.100: Cross-sectional view of the HE_1 waveguide, magnitude of the electric field strengths at 240 GHz and real parts of the characteristic impedances $\mathrm{Re}\,(Z_{\mathrm{HE}})$ of the first two hybrid modes versus frequency.

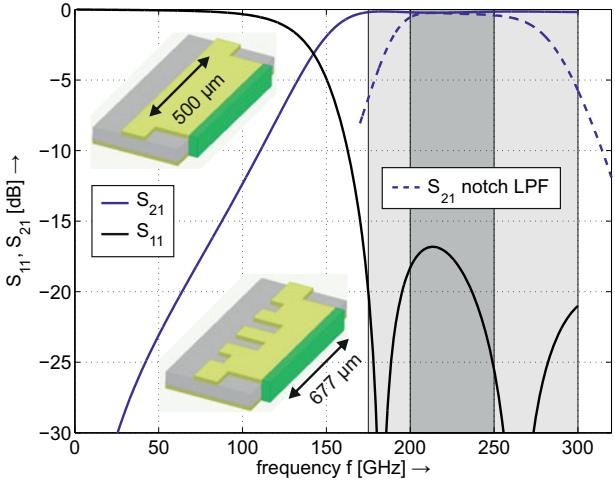

Figure 2.101: Simulated transmission (blue) and reflection coefficients (black) of the HE_1 waveguide as HPF with (dashed) and without (solid) integrated notch LPF.

(WR-4) is envisaged, a WR-3 waveguide is manufactured and used at Y-band frequencies (lower end of WR-3 frequency range).

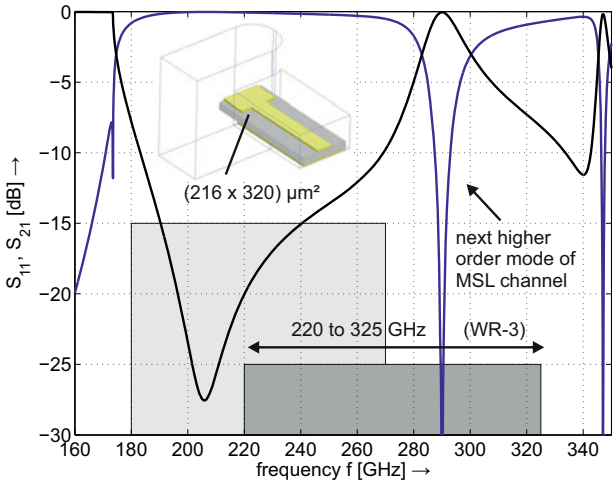

Figure 2.102: Simulated transmission (blue) and reflection coefficient (red) of a longitudinal E-field probe transition from MSL to WR-3.

Fig. 2.103 shows the measured input P_{in} (red) and output power levels P_{out} versus input f_{in} (red) and output frequencies f_{out}. The measurement setup is the same as it is with the D-band frequency doubler of the preceding paragraph.

Precise scalar P_{out} measurements have been performed with VDI Erickson PM4 calorimeter (black) according to the procedure outlined in [83]. Scalar power measurements do not allow for distinguishing spectral components of the harmonic content. Harmonic mixer measurements (blue) with rather poor accuracy (at least 6 dBm, subsection 2.7.2) have been applied to verify the calorimetric measurements consider the envisaged spectral component (3^{rd} harmonic).

The gray shaded area in Fig. 2.103 indicates the frequency range with sufficient input power level. An input power level of 16 dBm could be provided up to 65 GHz by commercial signal generator. From 65 to 81 GHz an amplified[47] E-band source with power levels from 16 to 19 dBm has been used in the test setup. The black curve in

[47] Amplifier RPG E-MPA-65-85-24-20 from Radiometer Physics GmbH.

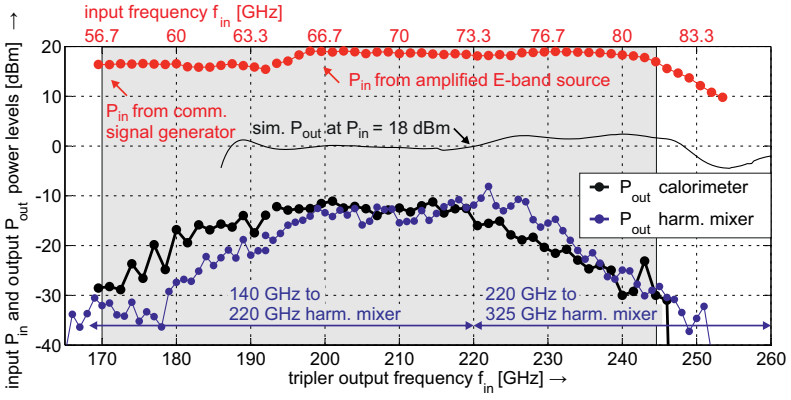

Figure 2.103: Measured input P_{in} (red) and output power levels P_{out} (black, blue) versus input f_{in} (red) and output frequencies f_{out} (black) of the proposed Y-band frequency tripler with WR-3 interface.

Fig. 2.103 without dots show P_{out} results from the synthesis procedure, that correspond to a constant input power level of 18 dBm. The measurement results are not corrected for insertion loss of interconnecting waveguides at the output ports.

The applied synthesis procedure for the Y-band tripler predicts output power levels in the range of -5 to 2 dBm from 186 to 249 GHz at 18 dBm input drivel level. The measurement results of Fig. 2.103 show output power levels $P_{\text{out}} \in [-11, -20]$ dBm from 180 to 230 GHz, which is a lot less output power than predicted. Assembly problems can be almost excluded as these results have been verified with two separate structures. Decreased output power levels at Y-band frequencies are believed to belong to the diode package and the electrically large distance of the two Schottky junctions. The frequency shift of the maximum output power level to lower frequencies, visible in Fig. 2.103, might be best explained by deteriorated performance of the longitudinal E-field probe to WR-3 waveguide. Careful inspection of Fig. 2.96 shows the separation of HE_1 waveguide and WR-3 probe is affected by the PCB manufacturing technology.

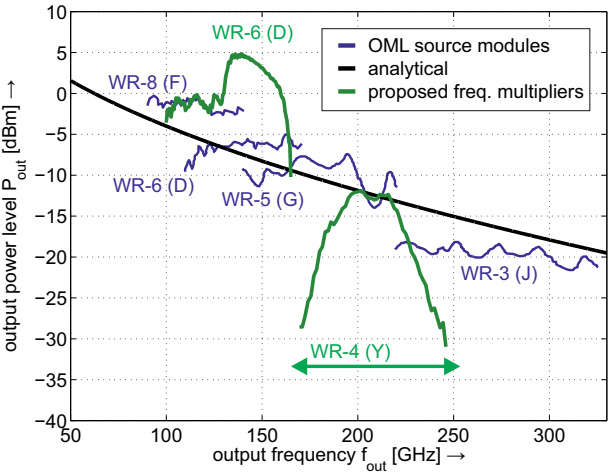

Figure 2.104: Comparison of measured output power levels P_{out} (green) of the D-band doubler and Y-band tripler with output power levels (blue) of the commercial signal generator series of OML Inc. versus frequency.

However, the reader should keep in mind that commercially available signal sources at Y-band frequencies deliver only -20 dBm of unleveled output power. Fig. 2.104 compares the measured output power levels of the proposed frequency multipliers with OML's signal generator frequency extension modules.

Efficient gallium arsenide (GaAs), gallium nitride (GaN) and indium phosphide (InP) E- and W-band MMIC power amplifiers recently became commercially available, therefore establishing 18 to 20 dBm input drive levels for the rather narrowband (10 %) radar modules can easily be realized. Whereas 15 dBm is the minimum necessary input power level. If MMIC driver amplifiers are used, bondwires to MSL instead of a WR-12 input waveguide can be utilized.

Conclusion and Outlook The developed D- and Y-band multipliers are capable for extending the frequency range of existing industrial short-range radar modules and might also be interesting for several imaging applications, where many cost effective multipliers arranged

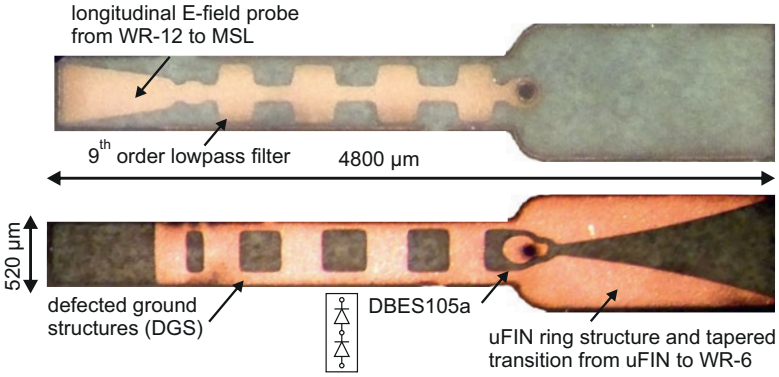

Figure 2.105: Photographs of top and bottom layer of a D-band (WR-6) frequency doubler.

in an array are required. Targeted improvements of the PCB manufacturing process, especially the realization of plated-through via holes, could further enhance the multipliers' performance.

Within the scope of this study, four more frequency multipliers are designed. Measurement results are not available, but the basic design idea is explained in the following.

The frequency doubler of Fig. 2.105 is similar to the doubler of subsection 2.6.5, which includes an explanation of the uFIN ring structure. The doubler utilizes the input LPF from Fig. 2.92. At the output the tapered transition from uFIN to WR-6 waveguide of Fig. 2.94 is used.

A D-band frequency tripler is depicted in Fig. 2.106. It utilizes the LPF of Fig. 2.99 in conjunction with the tapered (Dolph-Chebyshev) antipodal transition from MSL to WR-6 from Fig. 2.107. A transition from MSL to 1.85 mm coaxial connector is sufficient to cover the input frequency range.

Fig. 2.108 illustrates a Y-band frequency tripler, which is identical to the tripler of the preceding paragraph, but utilizes an integrated notch lowpass filter [84, 85]. The pitch of the notches is 159 µm and the individual lengths of the notches are $\ell_1 = \ell_4 = 63$ µm,

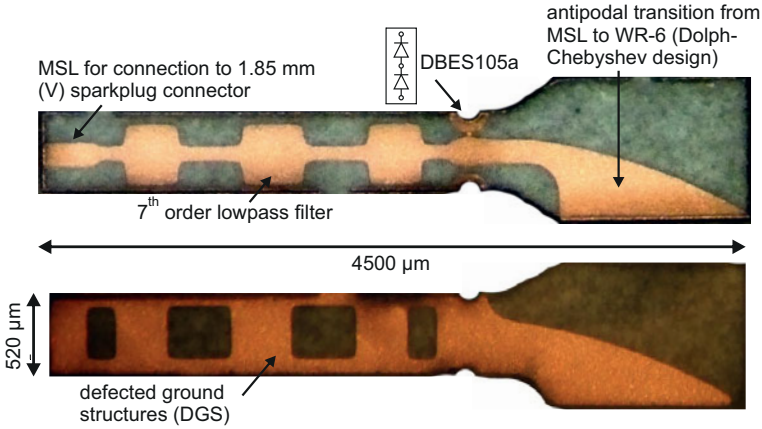

Figure 2.106: Photographs of top and bottom layer of a D-band (WR-6) frequency tripler.

$\ell_2 = \ell_3 = 139$ µm. The design procedure of distributed LPF based on quarterwave prototypes is given in the appendix A. The LPF constitutes an idler circuit for the 5^{th} harmonic. Simulated scattering parameters are shown in Fig. 2.101. The filter integration leads to an unintended altering of the HE_1 waveguide, which shifts the cut-off frequency to higher frequencies and therefore limits the operational bandwidth of the tripler.

A Y-band frequency tripler is depicted in Fig. 2.109. It utilizes the LPF of Fig. 2.99 in conjunction with a modified version of the tapered (linear) antipodal transition from MSL to WR-3 from Fig. 2.110.

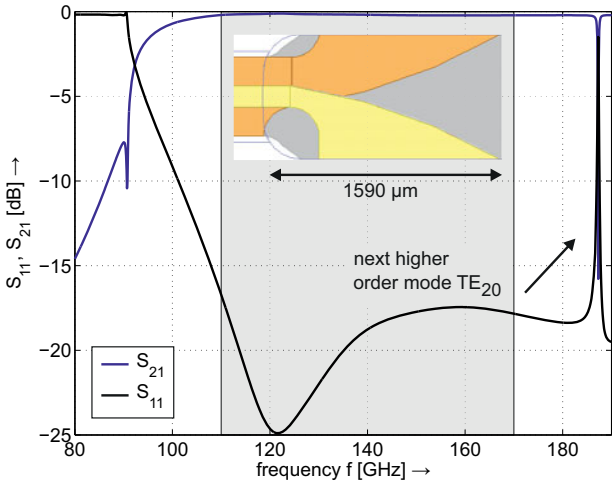

Figure 2.107: Simulated transmission (blue) and reflection coefficients (black) of the tapered (Dolph-Chebyshev) antipodal transition from MSL to WR-6 versus frequency.

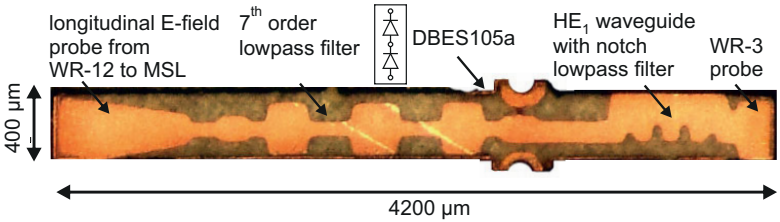

Figure 2.108: Photographs of top and bottom layer of the a Y-band (WR-3!) frequency tripler with integrated notch LPF.

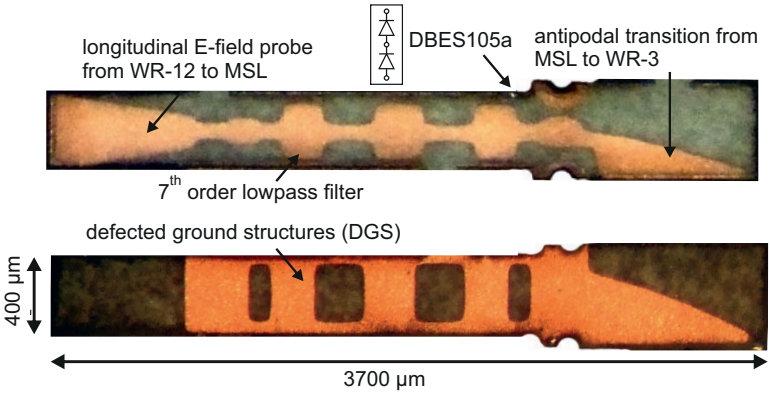

Figure 2.109: Photographs of top and bottom layer of a Y-band (WR-3!) frequency tripler.

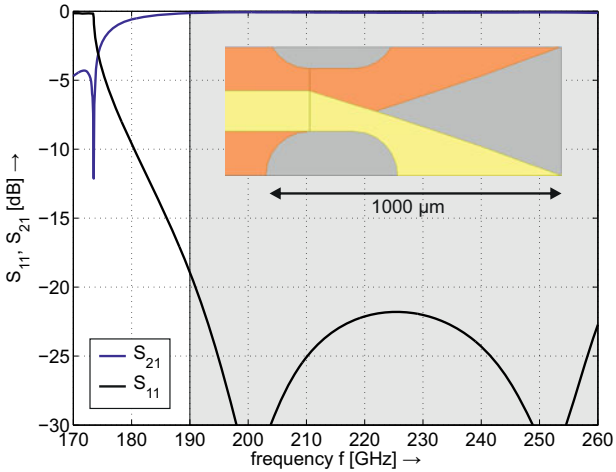

Figure 2.110: Simulated transmission (blue) and reflection coefficients (black) of the tapered (linear) antipodal transition from MSL to WR-3 versus frequency.

2.7.1 Dolph-Chebyshev Taper

Continuous tapers from waveguides with characteristic impedance Z_1 and Z_2, respectively, are considered. The Dolph-Chebyshev or Klopfenstein taper [86–88] provides a specified passband reflection coefficient $\Gamma_{\max}$ at minimum taper length ℓ or achieves minimum reflection coefficients for a given length ℓ. Hence, it is the preferred design solution for the required waveguide transitions within the proposed circuits of this thesis, especially hollow waveguide to finline and microstrip line transitions (Fig. 2.94, Fig. 2.107). Reflection behaviour is improved compared to exponential, triangular tapers and discrete multisection quarterwave transformers[48].

Derivation of the required characteristic impedance contour $Z(z)$ is given in the following. The overall reflection coefficient $\Gamma(z)$ of a nonuniform transmission line (NTL) with length $-\ell/2, \ldots, z = 0, \ldots, \ell/2$, which is terminated in $Z(z = -\ell/2)$ at the input and $Z(z = \ell/2)$ at the output, is described by the first order nonlinear differential equation from Walker and Wax (see derivation of Eq. (3.51) in subsection 3.2.1).

$$\begin{aligned} &\frac{\mathrm{d}\Gamma(z)}{\mathrm{d}z} - 2\gamma(z)\Gamma(z) + \left[1 - \Gamma(z)^2\right] p(z) = 0 \\ &p(z) = \frac{1}{2}\frac{\mathrm{d}}{\mathrm{d}z} \ln Z(z) \end{aligned} \tag{2.91}$$

In case of $\Gamma^2 \ll 1$, which is known as small signal reflection theory (page 193 et seqq.), it simplifies to the following equation.

$$\frac{\mathrm{d}\Gamma(z)}{\mathrm{d}z} - 2\gamma(z)\Gamma(z) + p(z) = 0 \tag{2.92}$$

Applying the boundary condition $\Gamma(\ell/2) = 0$ and assuming lossless transversal electromagnetic wave (TEM) propagation $\gamma = j\beta$, $\Gamma(z)$ is given by Eq. (2.93).

[48] In fact, Dolph-Chebyshev tapers are degenerated multisection quarterwave transformers with Chebyshev passband characteristics, infinite order and fixed length.

$$\begin{aligned}\Gamma(z) &= \int_{-\ell/2}^{\ell/2} p(\zeta) \exp\left(-2 \int_{-\ell/2}^{\zeta} \gamma(\xi) \mathrm{d}\xi\right) \mathrm{d}\zeta \\ \Gamma \exp(j\beta\ell) &= \int_{-\ell/2}^{\ell/2} p(\zeta) \exp(-2j\beta\zeta)\, \mathrm{d}\zeta\end{aligned} \tag{2.93}$$

Inspecting Eq. (2.93), $p(z)$ and $\Gamma e^{j\beta\ell}$ are recognized as a pair of Fourier transform. This allows for calculation of $p(z)$ from the taper's specification.

$$p(z) = \frac{1}{\pi} \int_{-\infty}^{\infty} [\Gamma \exp(j\beta\ell)] \exp(j2\beta z)\, \mathrm{d}\beta \tag{2.94}$$

In case of a Chebyshev taper with infinite order and fixed length ℓ, Γ is given by Eq. (2.95) [86].

$$\Gamma \exp(j\beta\ell) = \Gamma_0 \frac{\cos\left((\beta\ell)^2 - A^2\right)}{\cosh(A)} \tag{2.95}$$

Whereas Γ_0 is the reflection coefficient without taper or taper length equal to zero $\Gamma_0 = \frac{Z_2 - Z_1}{Z_2 + Z_1}$. In [86] it is suggested to use $\Gamma_0 = \frac{1}{2} \ln\left(\frac{Z_2}{Z_1}\right)$ as an initial value for numerical calculation. To determine the constant value of A, the specified $\Gamma_{\max}$ and ℓ/λ are inserted into Eq. (2.95). A is known from Eq. (2.96).

$$0 = \Gamma_0 \frac{\cos\left((\beta\ell)^2 - A^2\right)}{\cosh(A)} - \Gamma_{\max} \tag{2.96}$$

Inserting Eq. (2.95) into Eq. (2.94) and solving the integral leads to Eq. (2.97) with the modified Bessel function I_1 of the first kind with order one, and the unit impulse function δ.

$$p(z) = \frac{\Gamma_0}{\cosh(A)} \left(\frac{A^2}{\ell} \frac{I_1\left(A\sqrt{1-(2z/\ell)^2}\right)}{A\sqrt{1-(2z/\ell)^2}} + \frac{\delta(z-\ell/2)+\delta(z+\ell/2)}{2} \right)$$
$$p(z) = 0 \qquad |z| \leq \ell/2 \ \wedge |z| > \ell/2 \tag{2.97}$$

From direct integration of $p(z)$ (Eq. (2.91)), the Dolph-Chebyshev impedance contour $Z(z)$ is given by Eq. (2.98).

$$\begin{aligned} Z(z) = &\exp\Big(\frac{1}{2}\ln(Z_1 Z_2) + \frac{\Gamma_0}{\cosh(A)}(A^2\phi(2z/\ell, A)+ \\ &H\left(z-\ell/2\right) + H\left(z+\ell/2\right)\big)\Big) \qquad -\ell/2 \geq z \leq \ell/2 \end{aligned} \tag{2.98}$$

The taper starts and ends with a uniform transmission line.

$$Z(z) = Z_2 \quad z > \ell/2 \qquad\qquad Z(z) = Z_1 \quad z < -\ell/2 \tag{2.99}$$

H denotes the Heaviside[49] or unit step function (Eq. (2.100)).

$$H(m) = \begin{cases} 0 & m < 0 \\ 1 & m \geq 0 \end{cases} \tag{2.100}$$

ϕ is numerically calculated from Eq. (2.101).

$$\phi(k, A) = -\phi(-k, A) = \int_0^k \frac{I_1\left(A\sqrt{1-y^2}\right)}{A\sqrt{1-y^2}} \mathrm{d}y \qquad |k| \leq 1 \tag{2.101}$$

2.7.2 Uncertainty Analysis of Spectral Power Measurements above 50 GHz

Measurements with thermocouple or diode power meters constitute the most precise method to capture scalar power levels, but do not allow for distinguishing spectral components of the harmonic content.

[49] Oliver Heaviside (1850−1925), English engineer.

At the time of writing spectrum analyzers are commercially available up to 43 / 50 / 67 GHz. The maximum input frequency is limited by the utilized magnetically tunable preselection bandpass filters (Fig. 1.3), primarily based on yttrium iron garnet (YIG). More sophisticated approaches are required to further increase the base instrument's frequency, which are subject of current research [G1], [64, 65]. Spectral measurements above 43 / 50 / 67 GHz with decreased accuracy are performed with calibrated hollow waveguide harmonic mixers (V-, E-, W-, D-, G-, J-band) in front of a spectrum analyzer to verify the power meter measurements consider the envisaged spectral components (2^{nd} resp. 3^{rd} harmonic) and to measure the multipliers rejection of undesired harmonics.

A brief uncertainty analysis of harmonic mixer measurements is presented in the following. Detailed information about considering several unknown systematic and random error contributions to the overall measurement error of spectrum analyzers can be found in [89–91]. These different errors, contributing to the overall measurement uncertainty of the spectrum analyzer are

- the absolute level error,
- frequency response error,
- attenuator error,
- IF gain error and
- linearity error.

To simplify the uncertainty analysis we neglect all inherent error sources of the spectrum analyzer base instrument and focus on errors due to conversion loss look-up table inaccuracies of the harmonic mixers and errors from mismatch of the harmonic mixers Γ_{MIXER} and the device under test (DUT) Γ_{DUT}.

Nonlinear devices, likewise the proposed frequency multipliers, are poorly matched to the measurement system impedance (50 Ω or characteristic impedance of the corresponding hollow waveguide).

Neglecting the errors during the calibration measurement of the harmonic mixers, performed by the manufacturer, the main source of

errors is deviation from the harmonic mixer's specified local oscillator power level and temperature drift[50]. The manufacturer specifies a maximum level error of 3 dB at 25° and 4.5 dB at 5° to 40° with confidence level of 95 %. Assuming Gaussian distribution this corresponds to the variance value in Eq. (2.102), with 1.96 being the coverage factor of 95 % confidence level.

$$\sigma^2 = (3\ \mathrm{dB}/1.96)^2 = 2.34\ \mathrm{dB}^2 \tag{2.102}$$

Considering the interconnection of mismatched DUT and mismatched harmonic mixer, we build the ratio Eq. (2.103) between the measured power $P_{\max}$ in case of matched conditions $\Gamma_{\mathrm{MIXER}} = \Gamma_{\mathrm{DUT}} = 0$ and P_{meas} in the arbitrary case $\Gamma_{\mathrm{MIXER}} = \Gamma_{\mathrm{DUT}} \neq 0$.

$$\frac{P_{\max}}{P_{\mathrm{meas}}} = \frac{|1 - \Gamma_{\mathrm{DUT}}\Gamma_{\mathrm{MIXER}}|^2}{1 - |\Gamma_{\mathrm{MIXER}}|^2} \tag{2.103}$$

In Eq. (2.104) the power ratio $P_{\max}/P_{\mathrm{meas}}$ is expressed in decibel (dB) units.

$$\begin{aligned}\left(\frac{P_{\max}}{P_{\mathrm{meas}}}\right)_{\mathrm{dB}} &= 10\log_{10}\left(|1 - \Gamma_{\mathrm{DUT}}\Gamma_{\mathrm{MIXER}}|^2\right) \\ &\quad - 10\log_{10}\left(1 - |\Gamma_{\mathrm{MIXER}}|^2\right)\end{aligned} \tag{2.104}$$

The denominator in Eq. (2.103) resp. the second term in Eq. (2.104) does only depend on the magnitude of the mixer's reflection coefficient $|\Gamma_{\mathrm{MIXER}}|$ and is therefore already considered in the conversion loss look-up table. Eq. (2.105) shows maximum and minimum values of the remaining term.

[50] The spurious tone output of these harmonic mixers is another source of error. General methods for identification of spurious signals are given in [92], chapter 6. In [93] a commercially implemented procedure is described, which is based on comparing screenshots (bitmap files) of spectral measurements with different local oscillator frequencies.

$$20\log_{10}\left(\left|1-\Gamma_{\mathrm{DUT}}\Gamma_{\mathrm{MIXER}}\right|\right) = \begin{cases}\text{max.} & 20\cdot\log_{10}\left(1-\left|\Gamma_{\mathrm{DUT}}\right|\left|\Gamma_{\mathrm{LOAD}}\right|\right)\\ \text{min.} & 20\cdot\log_{10}\left(1+\left|\Gamma_{\mathrm{DUT}}\right|\left|\Gamma_{\mathrm{LOAD}}\right|\right)\end{cases} \tag{2.105}$$

The magnitude of the minimum limit in Eq. (2.105) will always be greater than the magnitude of the maximum limit in Eq. (2.105) and is therefore used as mismatch uncertainty [94]. Assuming U distribution [95–97] for errors due to mismatch, this corresponds to the variance expression in Eq. (2.106).

$$\sigma^2 = 1/2\cdot\left[20\cdot\log_{10}\left(1-\left|\Gamma_{\mathrm{DUT}}\right|\left|\Gamma_{\mathrm{LOAD}}\right|\right)\right]^2 \tag{2.106}$$

Although the individual errors have different error distributions, the total error distribution is assumed to be Gaussian. Strictly speaking this holds true only if there are many individual contributions that all have comparable magnitudes (central limit theorem). For Gaussian distribution the individual standard deviations are summed up in Pythagorean way to the total combined standard deviation σ_{total}, that is scaled to total error levels with certain confidence levels using the appropriate coverage factors.

$$\sigma_{\mathrm{total}} = \sqrt{\sum\sigma_k^2} \quad k\in\mathbb{N} \tag{2.107}$$

In case of 95 % confidence level the total measurement uncertainty is $\sigma_{\mathrm{total}}\cdot 1.96$. Table 2.9 summarizes the calculated total measurement errors under certain DUT and harmonic mixer matching conditions and confidence levels. In case of $|\Gamma_{\mathrm{DUT}}| = -4$ dB and $|\Gamma_{\mathrm{MIXER}}| = -5.11$ dB the total measurement error is ±3.1 dB at 68 % confidence level. The error is reduced to ±1.7 dB when using mixers with $|\Gamma_{\mathrm{MIXER}}| = -13.99$ dB. Within the scope of this work, harmonic mixers with both return loss values have been used.

The presented uncertainty analysis makes clear, well-matched harmonic mixers, utilizing isolators at the input [98, 99], can significantly improve measurement accuracy. The probability of the calculated er-

Table 2.9: Calculations of Total Measurement Error with Harmonic Mixers for Different DUT Reflection Coefficients

Γ_{DUT} [dB]	$\Gamma_{\mathrm{LOAD}} = \Gamma_{\mathrm{MIXER}}$ [dB]	confidence level [%]	total meas. error [dB]
−2	−5.11/ − 13.99	68	±3.9/ ± 1.9
−4	**−5.11 / −13.99**	**68**	**±3.1 / ±1.7**
−6	−5.11/ − 13.99	68	±2.5/ ± 1.7
−2	−5.11/ − 13.99	95	±7.6/ ± 3.7
−4	−5.11/ − 13.99	95	±6.0/ ± 3.4
−6	−5.11/ − 13.99	95	±4.9/ ± 3.3
−2	−5.11/ − 13.99	99	±10.0/ ± 4.8
−4	−5.11/ − 13.99	99	±7.9/ ± 4.5
−6	−5.11/ − 13.99	99	±6.5/ ± 4.3

Uncertainty of conversion loss look-up table is fixed at 3 dB according to datasheet information with confidence level of 95 %.

rors seems to be higher at the lower and upper bandwidth limits of the corresponding hollow waveguides than it is at center frequency. This is observed when using a calibrated E-band harmonic mixer, which has an overlapping frequency range with both, the V- and W-band mixers. The measured output power levels then show better agreement with the results from power meter measurements around 75 GHz. In consequence, the reader should keep in mind the presented spectral measurement data in subsections 2.6.1 to 2.6.5 and section 2.7 underlie the outlined restrictions. Precise output power level and conversion efficiency measurements are performed with power meters.

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