Chapter 1
Introduction

In this introduction the motivation for investigating deep-sub-micron and nanometer CMOS comparators in detail is described. Furthermore, comparators are classified and different types of analog continuous-time and clocked comparators are introduced. In addition digital comparators are shortly addressed.

1.1 Motivation

The further progress of technology is in most cases coupled with the increasing demand of handling more operations in a shorter time. As a tendency more functional blocks are implemented into the digital domain to have the possibility of easier and more individual implementation and adaptation with software. At the link between the analog and digital domain, analog-to-digital converters (ADCs) translate analog signals into digital values, which are discrete in time and amplitude. The translation from the digital into the analog domain is done by digital-to-analog converters (DACs). A fast computation in the digital domain also forces among other things the need of fast ADCs. For example in the future fast ADCs will be used in Ultra-WideBand (UWB) communication systems and in Software Defined Radio (SDR):

- The UWB technology [1] will cover wireless data transmission in the frequency band of 3.1–10.6 GHz. Data transmissions of higher than 100 MBit/s in distances of below 10 m are intended for Wireless Personal Area Networks (WPANs). In an UWB receiver ADCs may be placed in the base-band for a further decoding of the received signal with e.g. a Digital Signal Processor (DSP). So functions like decoding, correction sequences or controlling of e.g. Variable Gain Amplifiers (VGAs) or Phase Locked Loops (PLLs) in the receiver are implemented in an easier way with software.
- The concept of a SDR transceiver [2] is to place the ADC and DAC as close as possible to the antenna (see Fig. 1.1). This makes the transceiver to be reconfigured

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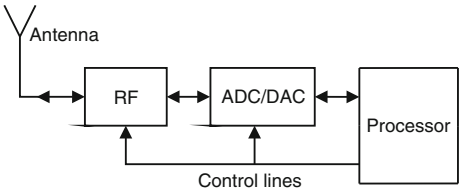

Fig. 1.1 Concept of an ideal SDR transceiver

very easily with the help of changing or extending the software. Various wireless standards may be handled with only a moderate amount of hardware components, which as a consequence reduces costs. It should be noticed, that in today's SDR transceivers there are many trade-offs, because the ideal implementation is very optimistic and would consume a considerable amount of power with state-of-the-art technology.

To save costs of production steps and to minimize the final product, several functional circuit blocks are combined into one chip and form a System on a Chip (SoC). So it is common to e.g. implement digital and analog blocks into one chip with additional ADCs or DACs. A key element in an ADC is the comparator. It compares an input voltage or signal with a reference voltage or another signal and has as a result a logical stage, which indicates whether the voltage at one input is lower or higher than at the other input at a distinct time point. In most cases in fast ADCs, e.g. a flash ADC or a folding converter system [3, 4], many parallel clocked regenerative comparators are implemented, which work in parallel. They use positive feedback to force a fast decision during a half clock period. The rest of the clock is generally used to reset the decision of the comparator.

Other applications of clocked regenerative comparator circuits are their usages in an analog rank-order extractor [5] or as a voltage sense amplifier in a SRAM [6–8] or for data regeneration in e.g. a fast demultiplexer [9, 10].

This work focuses on clocked regenerative comparators for an intended implementation in an ADC, but also other applications may be considered. The demands to the comparator are among many others e.g. a low power consumption, a high sampling clock, mostly a small area consumption on the chip and a sufficient sensitivity and offset.

1.2 Classification of Comparators

The principle electrical function of a comparator [11, 12] is depicted in Fig. 1.2. A comparator compares the input value VA_p with VA_n and gives as result a logical value at the output which determines, whether the VA_p is higher or lower then VA_n. In Fig. 1.2 the logical value is represented by an non-inverted output OUT and an inverted output $\overline{OUT}$. In another point of view it can be said that a comparator detects the sign of the difference $VA_p - VA_n$. The following sections give a rough general overview of different types of comparators, which may be implemented in CMOS circuit design.

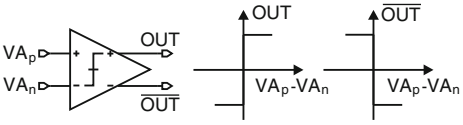

Fig. 1.2 Principle electrical function of a comparator

1.2.1 Comparators for Comparing Analog Values

Classified to the different types of analog input values, in CMOS circuit design typically comparators may compare voltages, currents or charges. As a result the comparator gives a logical value, e.g. the voltage levels of the supply voltage and the ground level for logical *high* and *low*, which indicates, whether one input value is higher or lower than the other one. Equality of both input values are mostly not treated, because the probability of appearing is extremely minimized. For this it is common, that a comparator is designed to have as high gain as possible to detect even small differences at the inputs. Other possibilities for treating equality are to introduce a hysteresis or adding sub-circuits for indication of equal input values.

Comparison of inputs can also be done by the comparator at distinct time points. Mostly these comparators need a clock or trigger signal. So it can be distinguished in a rough way between clocked or continuous-time comparators. Clocked comparators have to do their decision in a limited time slot. To minimize probability of appearance of errors due to equality of input values, in most cases positive feedback is used to enhance gain. In the literature sometimes clocked comparators are called dynamic comparators. This is due to the similarity to the function of dynamic logic [13], which needs during a clock period a pre-charge phase and a following evaluation phase, where a pull-up network (PUN) and/or a pull-down network (PDN) defines the logic state. Figure 1.3 shows the basic concepts of dynamic and complementary static logic styles. Complementary static CMOS logic, where the simplest implementation is the static CMOS inverter, consists of only a PUN and a PDN without a clock.

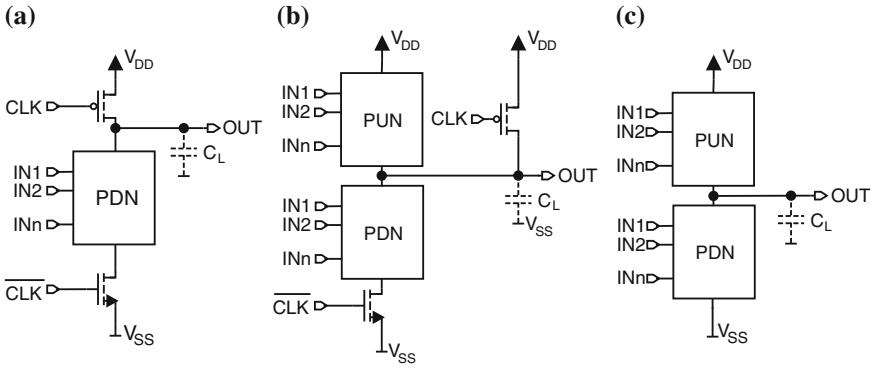

Fig. 1.3 Difference between static and dynamic logic. **a** Dynamic logic gate with pull-down network. **b** Dynamic complementary logic gate. **c** Static complementary logic gate

A comparator can also be designed to have only one input value, which is compared with an internal reference voltage, which may be defined by the operating point of the circuit structure.

To compare an input value with more than one reference values, multilevel comparators are built. They are used in e.g. multilevel logic, where more than two states exist in opposite to *high* and *low* of conventional logic or e.g. in a simple 1.5-bit ADC [14].

Figures 1.4, 1.5 and 1.6 show some examples of different types of CMOS comparators from the literature. A simple realization of a non-clocked voltage comparator is the **uncompensated OpAmp (operational amplifier) comparator** [15, 16], which is depicted in Fig. 1.4a. The input differential amplifier consists of input transistors $P1$ and $P2$, a current source transistor $P0$ and an active current-mirror load $N0$ and $N1$ for differential to single ended conversion. The output voltage OUT is generated by additional amplification with an active-loaded, common-source amplifier (transistors

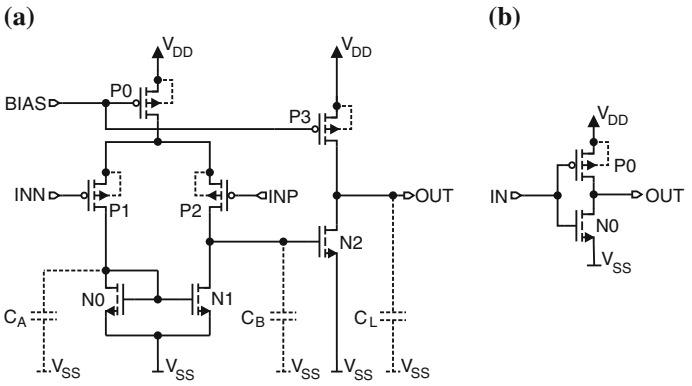

Fig. 1.4 Continuous-time CMOS voltage comparators. **a** OpAmp comparator [15, 16]. **b** Simple inverter as comparator [17]

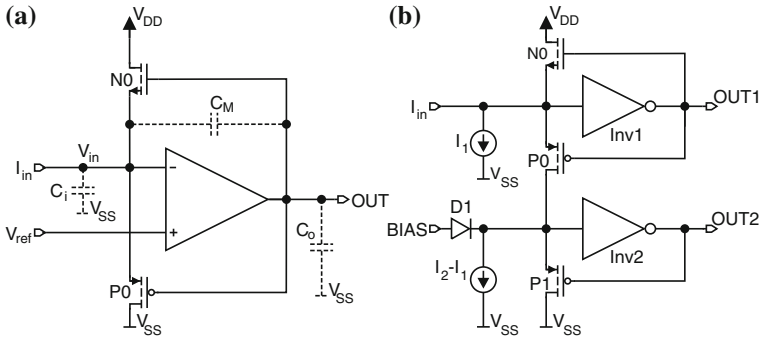

Fig. 1.5 Continuous-time CMOS voltage comparators. **a** Current switch comparator [19, 20]. **b** Multilevel current comparator [14]

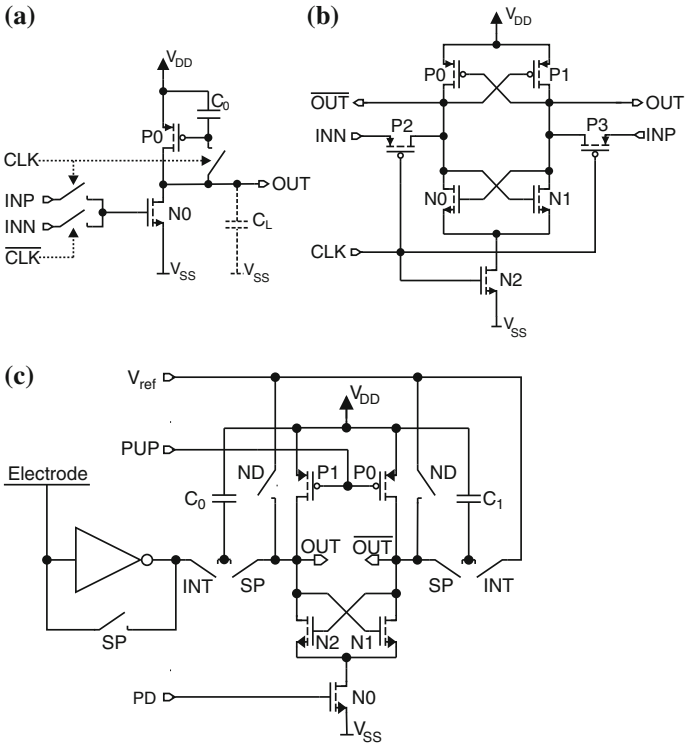

Fig. 1.6 Clocked CMOS comparators. **a** Simple dynamic CMOS voltage comparator [21]. **b** Dynamic CMOS latch [15]. **c** CMOS charge comparator [22]

*N*2 and *P*3). Here a typical compensation (e.g. Miller compensation) of the OpAmp is omitted to somewhat speed up the comparator and because to a comparator usually no circuitry for feedback is attached in opposite to an OpAmp. This comparator structure is still inherent slow, because during switching the internal parasitic capacitors C_A, C_B and the load capacitance C_L at the output node OUT have to be charged. Furthermore the minimum input voltage difference $INP-INN$, which causes a valid logical level at the output is defined by the amplification of the OpAmp comparator. In most Deep-Sub-Micron processes this amplification is typically low (in the area of 40 dB) due to different degrading effects of short channel MOS transistors. In opposite if these channels are designed longer, the parasitic capacitances increase due to larger gate-source or gate-drain capacitances thus reducing speed.

Figure 1.4b shows a **simple inverter used as comparator**. Such comparators were implemented in a flash ADC in [17]. Here the switching threshold V_{ST} of the inverter is the reference voltage to be compared, which is defined as the input voltage IN, that causes an equal output voltage OUT [18]. V_{ST} can be calculated in the ideal case with 1.1, where V_{tn} and V_{tp} are the threshold voltages, W_n and W_p the gate widths and L_n and L_p the gate lengths of transistors $N0$ and $P0$ respectively.

The mobility of electrons is denoted with μ_n and of holes with μ_p. If the voltage at IN is sufficiently higher than V_{ST} than OUT will switch to V_{SS} and in the other case to V_{DD}.

$$V_{ST} = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{\mu_n \frac{W_n}{L_n}}{\mu_p \frac{W_p}{L_p}}}}{1 + \sqrt{\frac{\mu_n \frac{W_n}{L_n}}{\mu_p \frac{W_p}{L_p}}}} \tag{1.1}$$

The amplification of the inverter and as a consequence the minimal detectable voltage difference $IN - V_{ST}$ is in principle defined by the transconductances and output resistances of transistors $N0$ and $P0$. The speed is determined mostly by the load capacitance of the output node, where also the parasitic gate-drain capacitances of $N0$ and $P0$ are added. Advantageous of the inverter comparator is the small amount of used transistors, a quite high switching speed and in most cases only a dynamic current consumption. Disadvantageous is, that V_{ST} suffers on the influence of mismatch, that the layout has to be changed for different V_{STH} and that there are several cases of static current consumption, e.g. if IN is between $V_{DD} - |V_{tp}|$ and $V_{DD} + |V_{tn}|$ for a rough estimation.

Figure 1.5 shows examples of continuous-time current comparators, where in Fig. 1.5a a so called **current switch comparator** [19, 20] is depicted. This comparator detects, whether the input current I_{in} is positive or negative. If as an initial condition is assumed, that $V_{in} = OUT = V_{ref}$ and transistors $N0$ and $P0$ are switched off, then a small positive input current I_{in}, which flows into the input node, will raise V_{in} slightly. This causes the output voltage OUT to decrease more than V_{in} raises due to the amplifier. Transistor $P0$ turns on and holds as a consequence V_{in} at level V_{ref}. The input node becomes a virtual ground. In the opposite case of a negative current I_{in} transistor $N0$ holds the input node at V_{ref}. OUT reaches a logical level and indicates, if I_{in} is positive or negative. If an ideal amplifier is assumed and the influence of the parasitic capacitance C_M, which consist of gate-source capacitances of $N0$ and $P0$, is neglected, a simple expression for $\Delta OUT(t)$ can be found with $\Delta V_{in} = (I_{in}/C_{in})t$ (see 1.2). GB is the gain-bandwidth of the amplifier.

$$\Delta OUT(t) = -\frac{GB}{2}\frac{I_{in}}{C_{in}}t^2 \tag{1.2}$$

Because of the parasitic capacitor C_M degrades the comparator's behavior, in [20] a current steering comparator was introduced, where instead of Fig. 1.5a the drain of $N0$ and $P0$ is connected to the output node and each gate is biased with an extra bias voltage.

To give an example of an **multilevel current comparator**, the comparator of Fig. 1.5a can be extended to that one of Fig. 1.5b [14]. Inverters (see Fig. 1.4b) are used instead of amplifiers, where V_{ref} from Fig. 1.5b is replaced by the inverter switching thresholds. Diode $D1$ with bias voltage $BIAS$ is only added to speed up the

circuit minimizing the voltage swing, where *BIAS* is chosen low enough to keep the node at the input of inverter Inv2 below the switching thresholds of Inv1 and Inv2. Following it will be assumed, that the current differences are sufficiently large so that the outputs of Inv1 and Inv2 switches between valid logical voltage levels like V_{DD} or V_{SS}. In the case that I_{in} is smaller than I_1 and I_1 smaller than I_2, $P0$ is off and $N0$ turns on to compensate $I_1 - I_{in}$ thus $OUT1$ and $OUT2$ are at V_{DD}. If I_{in} is between I_1 and I_2, $P0$ turns on and $OUT1$ switches to V_{SS}. The current difference $I_{in} - I_1$ flows to the input node of inverter Inv2 and is compared with the current difference $I_2 - I_1$. So $OUT2$ is V_{DD} if $I_{in} < I_2$ and switches to V_{SS}, if $I_{in} > I_2$. The application of such a multilevel comparator may be a simple 1.5-bit ADC.

Examples of different **clocked comparators** are given in Fig. 1.6. A **simple dynamic comparator** is depicted in Fig. 1.6a [21]. If *CLK* is *high*, pin *INP* is connected to the gate of transistor $N0$. Due to the fact, that transistor $P0$ is connected as MOS-diode and a capacitive load is assumed at node *OUT*, the appearing output voltage level is stored in capacitance C_0 (pre-charge phase). When *CLK* changes to *low*, *INP* is disconnected from the gate of $N0$, *OUT* is disconnected from the gate of $P0$ and instead *INN* is connected to the gate of $N0$. So in this phase the gate-source voltage of $P0$, caused by the current through $P0$ and $N0$ from the previous clock phase is stored in C_0. This current is now compared with the drain current, caused by *INN* (evaluation phase). If *INP* is larger than *INN*, the output node is charged by the difference current and the voltage level at *OUT* raises. In the opposite case node *OUT* is discharged and the voltage at *OUT* decreases. The advantage of this type of comparator is, that in principle the problem of transistor mismatch is avoided. Otherwise care has to be taken to parasitic charge injection of switches and the parasitic gate-drain capacitance of $P0$, which degrades the gain during evaluation. In [21] this comparator was built in a 0.9 µm CMOS process with a power supply of 1.5–3 V. At 3 V an offset of 1 mV was achieved.

The fastest types of comparators use **positive feedback**. In Fig. 1.6b a comparator is built with a **dynamic CMOS latch** [15]. The principle circuit block consists of two inverters $N0$-$P0$ and $N1$-$P1$, which are cross-coupled to a latch to achieve positive feedback. When *CLK* is *low*, transistors $P2$ and $P3$ are switched on and transistor $N2$ is switched off thus disconnecting current flow to V_{SS}. The output nodes *OUT* and $\overline{OUT}$ are pre-charged with *INP* and *INN*. When *CLK* changes to *high*, the latch is connected to V_{SS} and nodes *INP* and *INN* are disconnected. Due to the initial imbalance at the output nodes from the previous clock phase and the positive feedback, the latch pulls *OUT* to V_{DD} and $\overline{OUT}$ to V_{SS}, if *INP* was higher than *INN* and vice versa in the case *INP* is smaller than *INN*. The positive feedback of the latch is also called the regeneration of the latch. Due to the fast switching and the inherent high gain, caused by positive feedback, similar types of comparators are widely used in fast flash ADCs.

A charge comparator, which also has two n-MOS transistors $N1$ and $N2$ connected to positive feedback, is depicted in Fig. 1.6c [22]. The goal of this design was to measure the charge, which accumulates during a distinct time period to the electrode. The function of the comparator is divided into three phases. In the first phase, switches *ND* and *INT* are on, switch *SP* is off and transistors $P0$, $P1$ (*PUP*) and $N0$ (*PD*) are

off. The charge, which is collected by the electrode causes a small change in the electrode voltage, which is amplified by the inverter and finally stored in capacitor C_0. A reference voltage V_{ref} is connected to capacitor C_1 and nodes OUT and $\overline{OUT}$ are also pre-charged to V_{ref}. In the second phase SP is switched on and INT is released, while the other switches keep their position. The output of the inverter and the electrode is reset to the inverter's switching threshold. Node OUT is charged by capacitor C_0 and node $\overline{OUT}$ is charged from reference capacitor C_1. In the third phase switches ND and SP are off and switch INT is turned on. PUP changes to *low* and PD switches to *high* thus turning load transistors $P0$ and $P1$ and transistor $N0$ on. The latch regenerates due to positive feedback depending on the charge difference at nodes OUT and $\overline{OUT}$. In this phase capacitor C_0 begins to store the output voltage of the inverter, which depends on the accumulated charge, for next comparison. Capacitor C_1 is connected to V_{ref}. After a sufficient charge accumulation time the first phase is initiated once again.

This book concerns on **clocked regenerative comparators**, which compares two voltage levels and are designed in Deep-Sub-Micron processes. Such comparators are widely used in integrated flash ADCs.

1.2.2 Comparators for Comparing Digital Values

Comparators, which compare digital, binary values, are implemented in most cases in microprocessors. Figure 1.7 shows an example of an implementation of a comparator, which compares two 4-bit values A and B [23]. The XOR gate determines at what bits A differs from B and places there a "1". Equality of A and B can be detected by using a NOR gate at the 4-bit result after the XOR gate. Only if a value $0000b$ appears after the XOR gate, the NOR gate indicates a equality by having a "1" as result. With the priority encoder the most significant "1" (= most significant unequal bit of A and B) is detected from the value after the XOR gate. The 4-bit result, which contains the

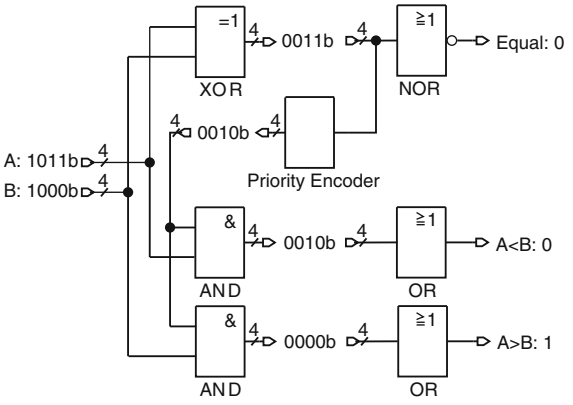

Fig. 1.7 Block diagram of a 4-bit comparator with a priority encoder [23]

most significant bit is used to detect from which value A or B it is originated. For this the AND- and OR gates are used. As a result a "1" at $A > B$ and a "0" at $A < B$ indicate that A is bigger than B and vice versa.

Comparators for comparing digital binary values are beyond the scope of this book.

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