

Chapter 2

Background

This chapter is going to present the theoretical background needed for the rest of the book. The blocks used in the design are going to be considered. This includes the quadrature voltage-controlled oscillator (QVCO), local oscillator (LO) buffer, injection-locked and static frequency dividers, low-noise amplifier (LNA) and the mixer.

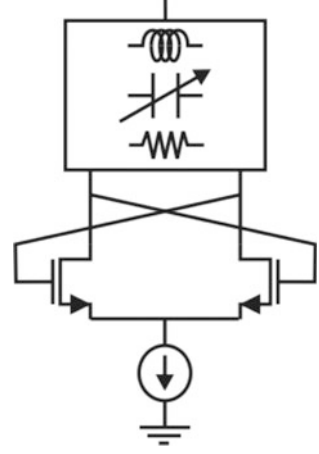
2.1 QVCO

This section includes an introduction to the QVCO. The oscillation condition and main parameters defined in the cross-coupled LC oscillators are going to be reviewed. An overview on the origins of phase noise in differential LC oscillators is presented. Finally, the QVCO topologies discussed in recent literature are shown.

2.1.1 VCO Basics

An oscillator is a circuit that generates a periodic signal in its steady state. The frequency of a voltage-controlled oscillator (VCO) is controlled by an external voltage source. It has no RF input signal, and it depends on the circuit noise to initiate a growing signal that settles to stable periodic signal in steady state. Oscillators may be used for frequency conversion in transceiver circuits and for clock generation in digital systems. An oscillator that generates a sine wave is a harmonic oscillator. A cross-coupled LC oscillator is widely used in communication systems. Compared to the resonator-less ring oscillator, it has superior phase noise performance but poorer quadrature accuracy when used to generate quadrature signals. As shown in Fig. 2.1, the cross-coupled LC VCO is composed of two parts; an active cross-coupled pair and a tunable resonator including the passive elements.

Fig. 2.1 Cross-coupled LC VCO



The transconductance and output resistance of the cross-coupled pair can be derived by connecting an AC voltage source at the output of the active part and deactivating independent sources, as in Fig. 2.2.

By relating V and I in Fig. 2.2, we can determine G_m and R_{out} as following:

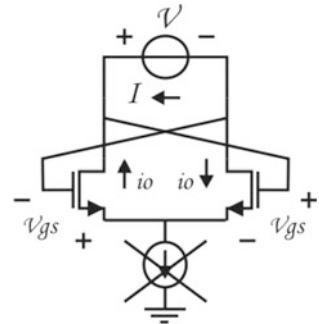
$$G_m = \frac{I_{out}}{V_{in}} = \frac{I}{V} = -\frac{i_0}{2V_{gs}} = -\frac{g_m}{2} \quad (2.1)$$

$$R_{out} = V/I = -2/g_m = 1/G_m \quad (2.2)$$

where G_m is the total active transconductance, $g_m (= i_0/v_{gs})$ is the transistor transconductance and R_{out} is the total active output resistance.

The impedance seen at the drain terminals of the cross-coupled pair can now be seen as a negative resistance $-R_m$ (R_m is assumed to be a positive number) with a noisy current source, as shown in Fig. 2.3. The equivalent impedance of the tank circuit at resonance reduces to a resistor, because both positive (inductive) and negative (capacitive) reactances cancel each other.

Fig. 2.2 Small-signal analysis of the active part



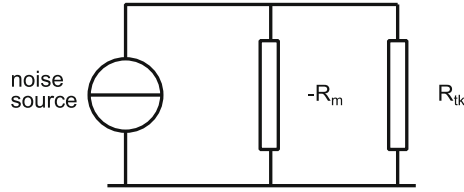


Fig. 2.3 Oscillator negative resistor model

The circuit will start oscillation, with the help of the noise source, when the negative resistance (resembling a power generating element) is higher in magnitude than the positive resistance (which is a power dissipative element) that represents tank losses. This is the oscillation condition, which is equivalent to saying:

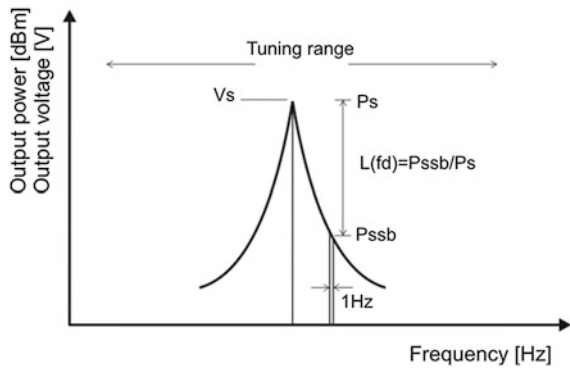
$$G_m > \frac{1}{R_{tk}} \quad (2.3)$$

where R_{tk} is the tank resistance. This is a single port model for the oscillator. The factor by which the negative resistance is higher than the positive one (R_m/R_{tk}) is the oscillation margin. This value should be greater than unity to ensure starting of oscillation.

2.1.2 Main Parameters

The voltage-controlled oscillator is characterized by four main parameters: center frequency, tuning range, output voltage swing and phase noise. Figure 2.4 is a graphical illustration of these parameters.

Fig. 2.4 VCO main defining parameters



The oscillator center frequency (f_0) is the frequency at which the output power is largest. This is defined by the resonant frequency of the tank circuit, which leads to the following result:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.4)$$

where L and C are the total inductance and capacitance seen at the drain nodes of the cross-coupled pair.

The oscillator tuning range is the difference between the maximum and minimum output frequency of the oscillator ($f_{\max} - f_{\min}$). This is usually controlled by a varactor, where the maximum and minimum capacitance of the varactor corresponds to the minimum and maximum output frequency of the oscillator, respectively.

$$f_{\max} = \frac{1}{2\pi\sqrt{LC_{\min}}} \quad (2.5)$$

$$f_{\min} = \frac{1}{2\pi\sqrt{LC_{\max}}} \quad (2.6)$$

$$f_0 = \frac{f_{\max} + f_{\min}}{2} \quad (2.7)$$

The oscillator's output voltage swing is the amplitude at the oscillator center frequency. It should be high enough to drive the following stage. This is usually not the case, and so a buffer is needed to deliver the required amplitude to the load. This will be shown in detail Sect. 2.2. Voltage swing is usually limited by tank losses (R_{tk}), and can be calculated, assuming a square wave output current, using the following equation:

$$V_{s-peak-diff} = A \approx \frac{2}{\pi} R_{tk} I_{tail} \quad (2.8)$$

The main assumption to the previous equation is that the output current arises from ideal on-off switching of the transistors, and therefore the tail current is commutated between either sides of the oscillator. The current through R_{tk} is then as shown in Fig. 2.5. The tank circuit is tuned to the fundamental tone of the square wave, which is then multiplied by the tank resistance to give a sinusoidal, differential output voltage swing.

Equation 2.8 is only valid as long as the bias current is not large enough to push the tail transistor into the triode region. When the bias current is increased, the gate-source voltage of the tail transistor is increased while the drain-source voltage is limited by the voltage headroom available from the supply. At the edge of the triode region, the voltage swing is limited by the supply, and no longer proportional to the

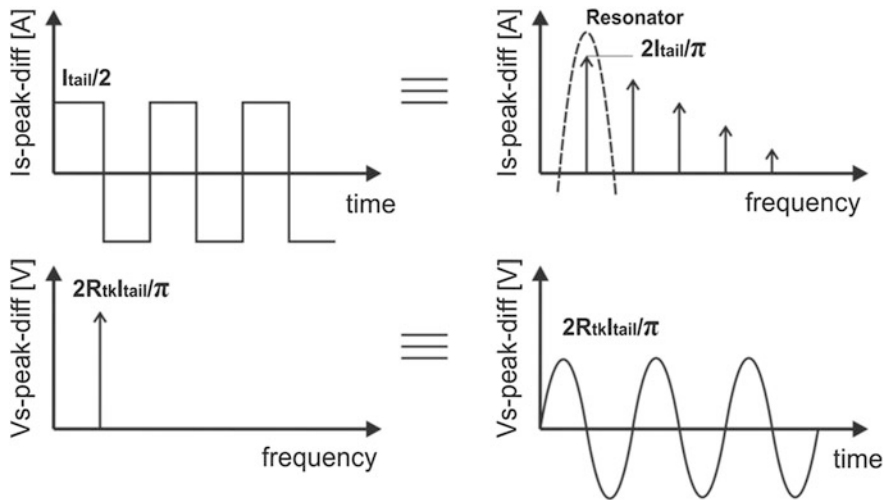


Fig. 2.5 Conversion from square wave current to sinusoidal output voltage through filtering by the resonator

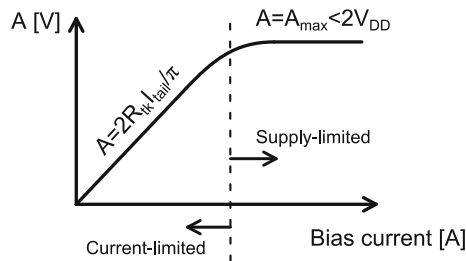


Fig. 2.6 Oscillator output differential amplitude based on the operation of the tail current transistor

tail current. Thus, two regions of operation are defined: the current-limited regime and the supply-limited regime [1]. The oscillator output differential amplitude within the two regions is shown in Fig. 2.6.

The spectrum of the output voltage signal of a real VCO circuit is not just a single frequency representing a pure sine wave. As shown in Fig. 2.4, the signal is spread in frequency having a skirt shape. In time domain, this can be seen as random variation of zero-crossings of the periodic sine wave signal representing the fundamental tone. In a phasor representation, this can be seen as a split into amplitude-modulated (AM) wave and phase-modulated (PM) wave as shown in Fig. 2.7, where both can yield phase noise, either directly or indirectly.

Phase noise is the parameter defining the spectral purity of the oscillator. The oscillator output signal is more “pure” when the fundamental component of its

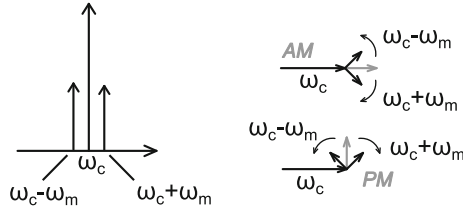
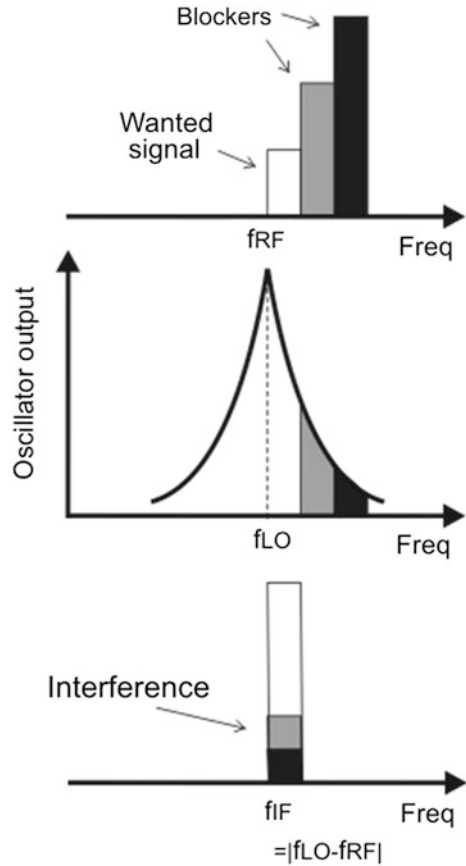


Fig. 2.7 Sidebands can be seen as AM and/or PM signals [2]

frequency domain is less spread in frequency. This is translated to a lower phase noise value. This parameter is very crucial, especially in receiver circuits. As shown in Fig. 2.8, an oscillator with a high phase noise can cause frequency down-conversion for unwanted adjacent channels, which cannot be distinguished from the wanted signal. This leads to signal interference and higher noise, reducing the system's signal-to-noise ratio (SNR).

Fig. 2.8 Down conversion of unwanted frequency bands due to oscillator spectral impurity



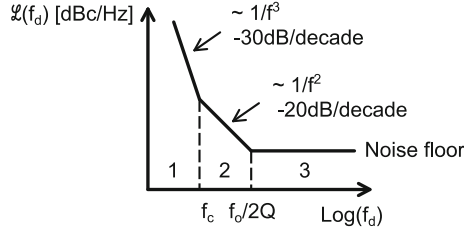


Fig. 2.9 Phase noise spectrum in dBc/Hz

As mentioned in [2, 3], phase noise is characterized using the single-sideband (SSB) phase perturbation spectral power in a 1 Hz bandwidth (spectral power density) at a frequency offset f_d away from the carrier frequency normalized to the power of this fundamental carrier frequency. Figure 2.9 shows the phase noise curve in dBc/Hz versus frequency. Three regions are defined according to the phase noise slope. The first region is independent of frequency, which is the white noise in the system. The second region is proportional to f^2 , and it shows the tank effect on the thermally induced noise sources in circuit components. Close-in phase noise is represented by the third region, which is proportional to f^3 and is due to active elements' flicker noise up-conversion close to the carrier frequency.

Several models and analyses for phase noise are presented in the literature aiming at understanding the relationships between circuit parameters and phase noise, and getting an equation that can predict the phase noise value [4–8]. More intuitive interpretations and closed form formulas were also developed [9, 10]. This is in order to have the possibility of exploring ways to reduce this unwanted effect in oscillators. Phase noise in the $1/f^2$ region, assuming a square wave output current and neglected parasitic capacitance, can be written in terms of circuit parameters as following [11].

$$\mathcal{L}(f_d) = 10 \log \left[\frac{kT}{C^2 A^2 R_{tk} f_d^2} (1 + \gamma_n) \right] \quad (2.9)$$

where C is the total VCO capacitance at the output nodes, A is the peak differential voltage swing, R_{tk} is the equivalent losses at the oscillator output and γ_n is the NMOS transistor excess channel noise parameter. This equation accounts for both tank and switch noise. Accurate prediction of the phase noise value is not expected using this equation at 60 GHz due to large parasitics. However, it is useful in determining the effect of circuit parameters on phase noise in the $1/f^2$ region.

2.1.3 Phase Noise Origins

Understanding phase noise origins can help choosing the correct modification in a circuit to reduce its value. A brief summary of phase noise origins will be presented

in this section. In [2] the differential LC oscillator phase noise is studied in great detail. The thermally induced phase noise can be a result of three main sources: the resonator, the differential pair and the current source.

2.1.3.1 Resonator Noise

Resistance R_{tk} representing tank losses is the noise generating element in the resonator. The noise current can be divided, due to the cross-coupled pair non-linearity, into AM and PM signals modulating the main oscillator tone. The AM signal can be filtered due to the limiting action of the cross-coupled pair. The cross-coupled pair negative resistance cancels the tank losses, and the PM signal is multiplied by the lossless resonator transfer function. This shows the importance of a lower bandwidth, i.e., higher quality factor resonator.

2.1.3.2 Differential Pair Noise

Noise in the cross-coupled pair will only be effective when both transistors are in the active region (this is mostly the case at 60 GHz). If one transistor switches off, the noise current of the other transistor will be in series with a constant current source I_{tail} , and thus eliminated. This can be modeled as the cross-coupled transistor white noise current multiplied by a pulsed G_m function with a frequency of $2f_o$. As shown in Fig. 2.10, the current noise of the cross-coupled transistors only at the fundamental frequency and its odd harmonics will cause noise to be folded at the oscillation frequency when multiplied by the pulsed G_m function. This analysis shows the importance of the noise generated at odd harmonics of the oscillation frequency from the cross-coupled pair. Note that the width of the time window at which both transistors are active doesn't affect the output referred noise density. The higher transistor transconductance, the less MOS transistors are in saturation region, and thus, the higher G_m sinc function bandwidth. But input-referred noise noise density is also lowered with higher transconductance. This leads to the same integrated rms output noise [12].

2.1.3.3 Tail Current Noise

Noise in the tail current will be commutated between the two sides of the oscillator. This can be modeled as being multiplied by a square wave with frequency components at the fundamental and odd harmonics.

Multiplications that will end up with noise components around the fundamental frequency are the square wave fundamental component with tail noise at DC and at second harmonic. Also the square wave third harmonic with the tail noise second harmonic, and so on. This is shown in Fig. 2.11. Note that only tail noise components at DC and even harmonics are causing noise components at the

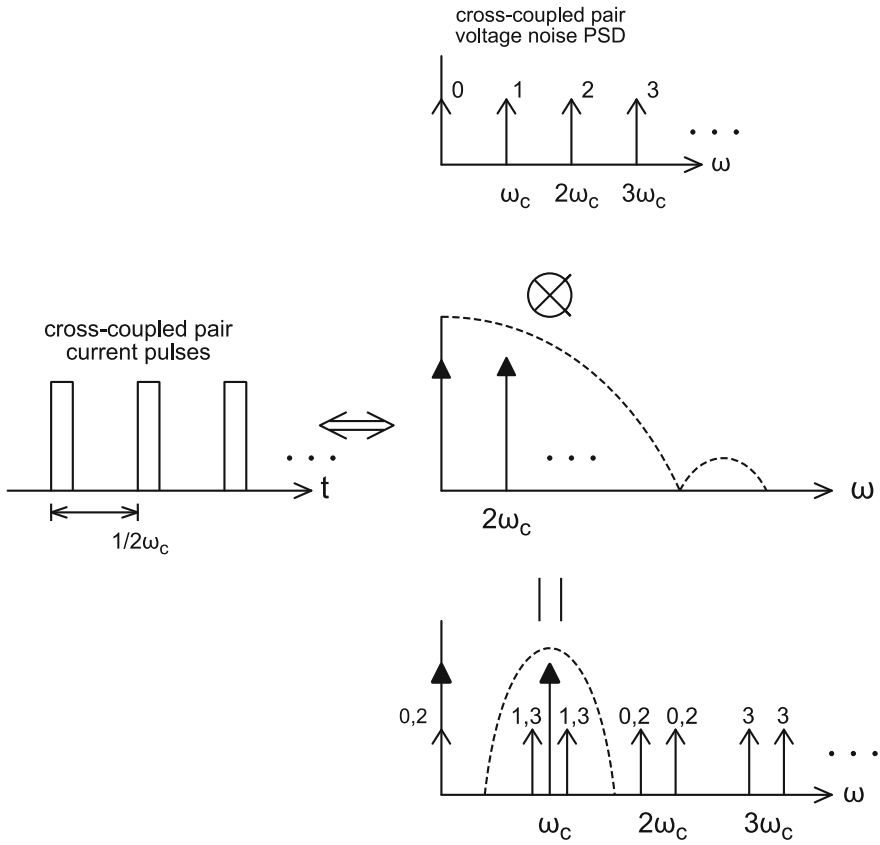


Fig. 2.10 Noise folding due to cross-coupled pair [2]

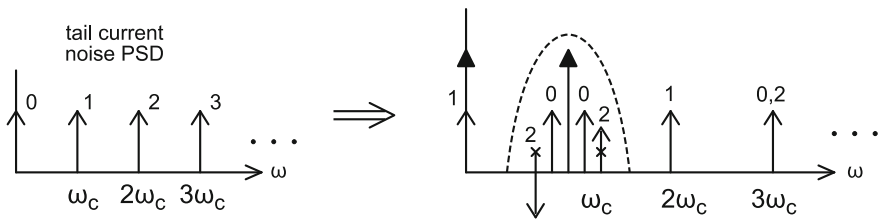


Fig. 2.11 Tail noise mixing with the cross-coupled pair [2]

fundamental frequency. Note also that tail noise component at DC will produce an AM signal. A varactor is a component that will convert voltage signal into a change in the capacitance value, and thus, a change in the operating frequency. Owing to

the varactor in the VCO, the AM signal generated from the DC component of the tail noise can be converted into an FM signal which appears as phase noise around the center frequency [13, 14].

2.1.4 Quadrature VCO

In direct conversion receivers, positive and negative sidebands of the RF signal spectrum are down-converted on top of each other at baseband [15]. In frequency and phase modulated signals, two down-converting paths with a 90° phase shifted oscillator signal are needed for demodulation. Quadrature voltage-controlled oscillator (QVCO) uses coupling mechanisms between two VCO's in order to produce four-phase outputs, all orthogonal to each other (Fig. 2.12).

One more parameter can be defined for the QVCO beside the main VCO parameters described before in Sect. 2.1.2: phase error or quadrature error. For multi-phase oscillators, phase error is the difference in degrees between the actual phase difference between two subsequent output terminals in the oscillator and the ideal value. In the QVCO with in-phase (I) and quadrature (Q) outputs, quadrature error is the deviation from the 90° phase difference between I and Q terminals.

Cross-coupled LC VCO's can be coupled in three different ways, each with its pros and cons: parallel coupling (P-QVCO), series coupling (with two different choices; TS-QVCO and BS-QVCO for top and bottom, respectively) and gate-modulated coupling (GM-QVCO) [16]. All of the main VCO parameters are affected by inserting the coupling transistor in the VCO core.

In the P-QVCO shown in Fig. 2.13, the coupling transistors are connected in parallel to the cross-coupled transistors. A, B, C and D outputs represent phase shifts of 0° , 180° , 90° and 270° , respectively. This topology is simple but has some disadvantages: phase noise is relatively high compared to the other topologies, and there is a trade-off between the phase noise and the quadrature accuracy through the coupling strength. The greater the coupling coefficient, the higher the phase noise but the better phase error, and vice versa.

The P-QVCO phase noise can be improved by independently biasing the gate of the cross-coupled pair [17]. This requires gate decoupling capacitors and biasing resistors as shown in Fig. 2.14. With a reduced gate voltage, the cross-coupled pair is allowed to provide more output voltage swings while operating in the saturation region.

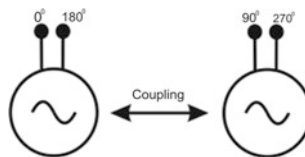


Fig. 2.12 Orthogonal signal out of the QVCO

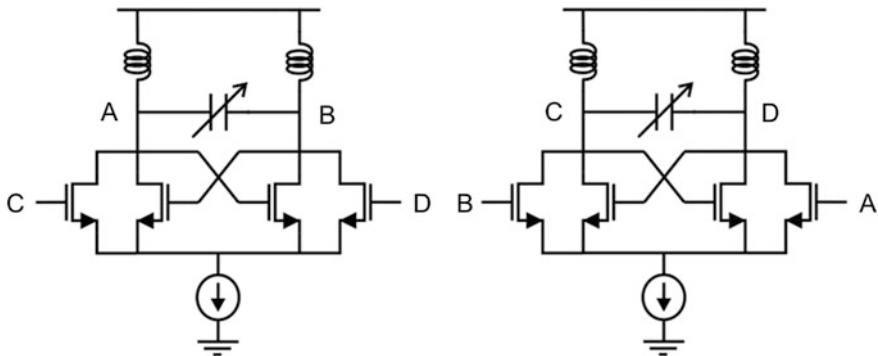


Fig. 2.13 Parallel QVCO (P-QVCO) topology

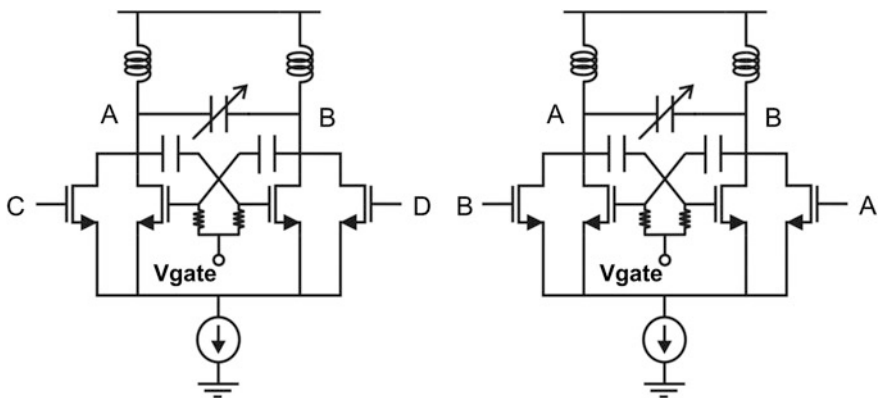


Fig. 2.14 P-QVCO with gate decoupling and external bias

In the top and bottom series-QVCOs of Fig. 2.15, coupling transistors are inserted in series with the cross-coupled pair. This takes from the voltage headroom available which is not so suitable for low-voltage applications. In the TS-VCO, large coupling transistors are needed to have lower phase error, which will dramatically increase the parasitic capacitance, and thus, reduce the tuning range. The BS-VCO, on the other hand, has higher phase accuracy and lower phase noise compared to the top-stacked one.

As shown in Fig. 2.16, a gate-modulated QVCO topology was proposed in [16]. The coupling transistors are placed in series with the gates of the switching transistors. This will improve the voltage headroom as compared to the series topologies. The GM-VCO was claimed to have the best quadrature accuracy and phase noise performances over the parallel and series ones. To ensure enough coupling strength from the opposite oscillator core, the coupling transistor sizes may need to be increased, which will lead to higher output parasitic capacitance, and thus, reduced tuning range.

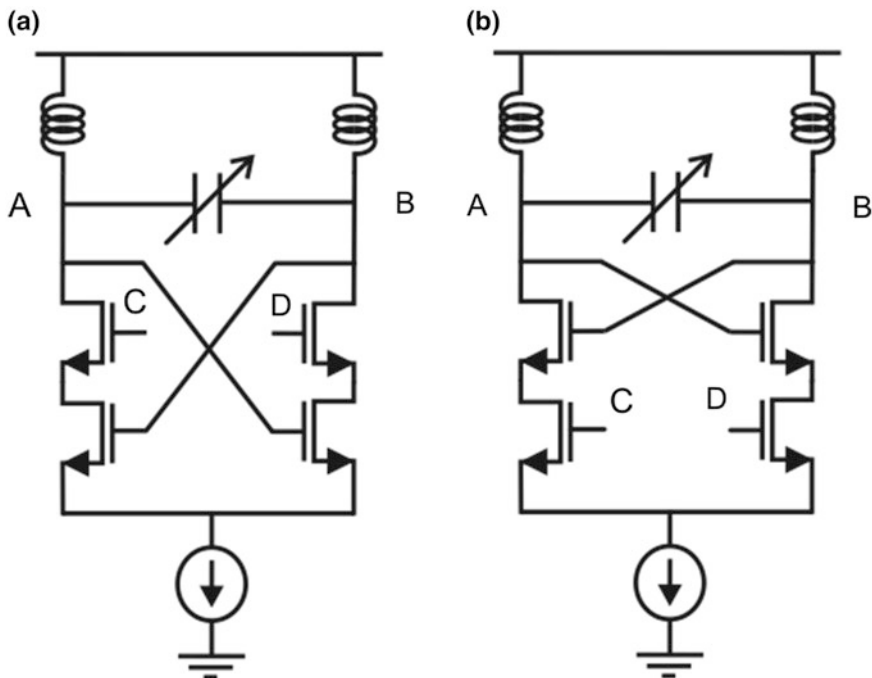


Fig. 2.15 Half-sections of series-QVCO in **a** top (TS-QVCO) and **b** bottom (BS-QVCO) configurations

2.2 LO Buffer

A buffer is usually needed after the VCO to minimize any effect of the output load on the oscillator signal. The VCO output can either feed another block in the system or go directly to the output for measuring purposes. In both cases, the VCO load can be modeled as a parallel combination of a capacitance and a resistance. The load capacitance can reduce the oscillation frequency and tuning range. The load resistance, however, can reduce the output amplitude. Thus, the phase noise can also be increased. Buffers are also needed to increase the output amplitude. Local oscillator (LO) buffers, for example, can deliver the output signal to a mixer. For higher conversion gain, the mixer input amplitude should be increased. LO buffers can be useless if it has a higher load than the following stage or if the VCO amplitude is large enough for the operation of the following circuit.

Two transistor configurations can be used as buffers for the VCO: source followers and common-source (CS) amplifiers. Source-followers reduce the VCO output amplitude (Fig. 2.17). They can be used if the VCO output is going to be directly measured stand-alone. In this case, large output swing is not required as it is used for testing purposes. The common drain transistor has a low output resistance, which is suitable for driving the output $50\ \Omega$ load.

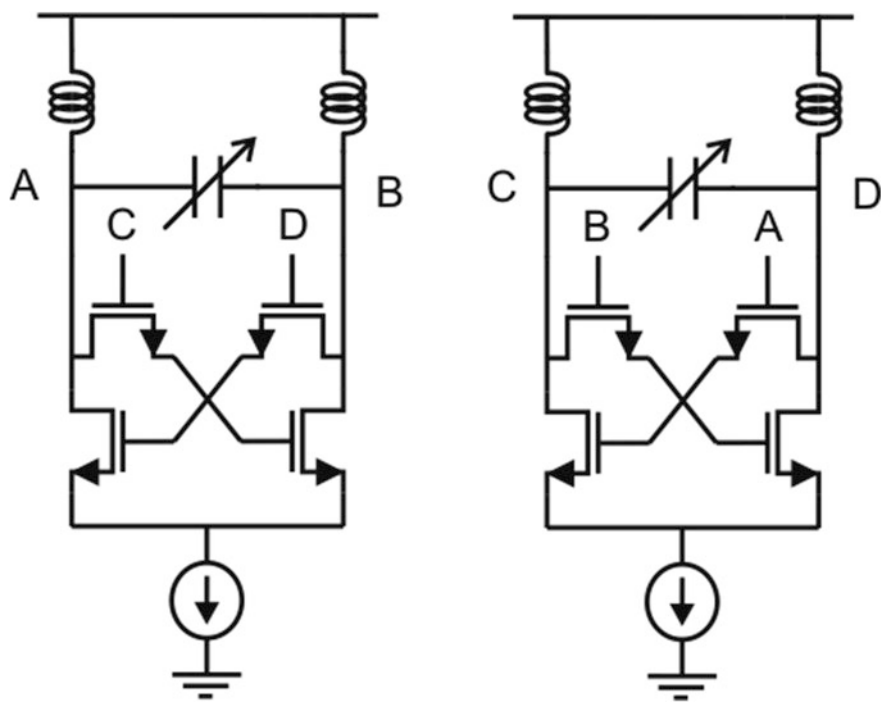
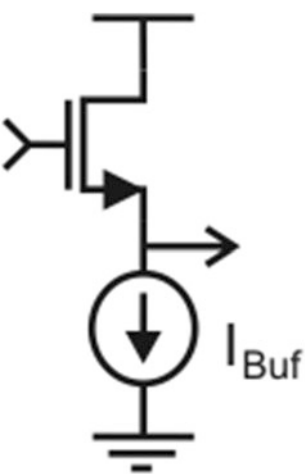


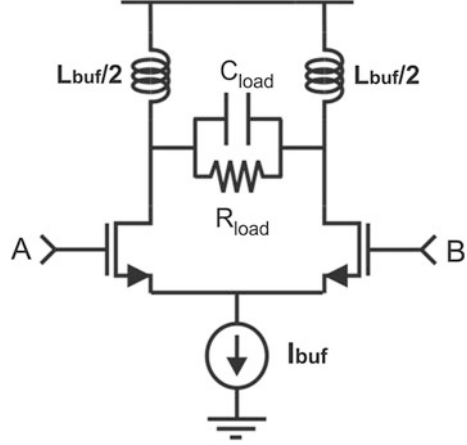
Fig. 2.16 Gate-modulated QVCO (GM-QVCO) architecture

Fig. 2.17 Source follower buffer



Common-source amplifiers can also be used after the VCO for buffering, as shown in its differential form in Fig. 2.18. Inductors can be used at high frequency to tune out all the parasitic and load capacitances at the output node. This allows the transistor to

Fig. 2.18 Inductively-tuned CS differential amplifier as a buffer



amplify the input signal within the required frequency range, with a peak at the tuning frequency f_{tune} , and a bandwidth limited by the current source I_{buf} .

$$f_{\text{tune}} = \frac{1}{2\pi\sqrt{L_{\text{buf}}C_{\text{tot}}}} \quad (2.10)$$

where $C_{\text{tot}} = C_{\text{parasitic}} + C_{\text{load}}$. When the buffer is used for measuring, an accurate prediction of the pad capacitance is required for choosing the buffer inductor value. Any mismatch between the buffer tuning frequency and the oscillator frequency will cause a significant reduction in the output amplitude.

The small-signal model of the buffer is shown in Fig. 2.19. If the inductor cancels all capacitive elements at the output node, the buffer gain can be calculated as following:

$$A_{\text{buf}} = G_m(r_{\text{out}} || R_{\text{load}} || R_{\text{par,L}}) = \frac{g_m}{2} R_{\text{out}} \quad (2.11)$$

If the total capacitance at the output node is not large enough, large inductor values will be required. Maximum inductance is usually limited by the inductor self resonance frequency, after which the lines forming the inductor behave capacitively. One way to get the gain peak at the required frequency is to add more capacitance at the output. Any additional capacitance comes with its parasitic resistance. This will add more load resistance to the output, and the total parallel resistance will be reduced, causing gain reduction.

$$A_{\text{buf}} = G_m(r_{\text{out}} || R_{\text{load}} || R_{\text{par,L}} || R_{\text{par,C}}) \quad (2.12)$$

Another way to get the tuning frequency with a limited inductor is to exchange the inductor load with a transformer as in Fig. 2.20a. The transformer used is

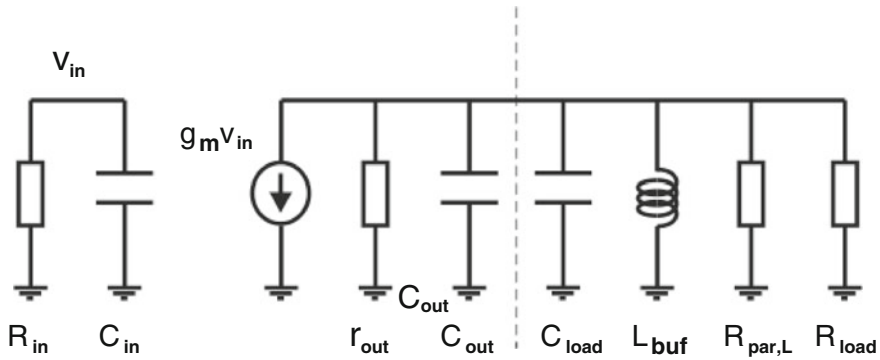


Fig. 2.19 Model of the active buffer

nothing but an increased equivalent inductance with the factor (k), which is the coupling coefficient. So:

$$L_{eq} = L_{tune}(1 + k) \quad (2.13)$$

It is worth noticing that a transformer is usually implemented with a lower quality factor than the inductor, as more than one metal layer should be used compared to the only top metal layer used in the inductor implementation. The gain can be the same as in Eq. 2.11 with a different inductor quality factor.

$$A_{buf} = G_m(r_{out} || R_{load} || R_{par,trafo}) \quad (2.14)$$

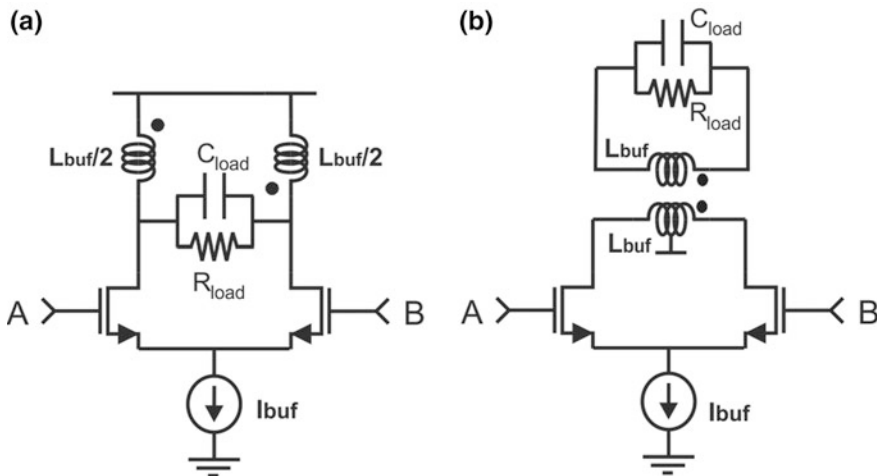


Fig. 2.20 Active buffer with transformer load **a** voltage output **b** current output

As shown in Fig. 2.20b, the transformer can be used in such a way that the output current of the common-source transistor is used instead of the output voltage. One side of the transformer will be connected to the buffer circuit, and the other side will be connected to the load.

This transformer-coupled differential amplifier is analyzed in [18]. If the load is assumed to be only capacitive, it will be transformed to the buffer output node with an equivalent impedance value that is elaborated in Appendix A, and given below in its final form:

$$Z_{\text{out}} = j\omega \left(L + \frac{\omega^2 L^2 C_{\text{load}} k^2}{1 - \omega^2 L C_{\text{load}}} \right) \quad (2.15)$$

This means that for practical values (for example, $f = 60$ GHz, $L = 100$ pH and $C_{\text{load}} = 20$ fF), the denominator will always be positive, and the common-source transistors will see an equivalent inductance value that depends on the load. Note that the equivalent inductance is higher than the primary value of the transformer. In practice, the buffer load is a transistor with an equivalent input parallel capacitance and resistance. The resistive component is transformed to the buffer output with a higher value (R'_{load}) [18]. Thus, the buffer voltage gain can be calculated as following:

$$A_{\text{buf}} = G_m (r_{\text{out}} || R'_{\text{load}} || R_{\text{par,trafo}}) \quad (2.16)$$

Note that the voltage-output transformer-coupled buffer is expected to provide higher gain (Eq. 2.14) compared to the current-output one (Eq. 2.16) because of the higher load resistance.

2.3 Frequency Divider

Frequency dividers are circuit blocks used to divide an input signal in the frequency domain. They can be categorized into static and dynamic dividers. Static dividers use bi-stable latches and, for operation at high frequencies, can be implemented using current-mode logic (CML) circuits [19]. Dynamic dividers don't quantize the divided signal in either amplitude or time. They are divided into regenerative, parametric and harmonic injection dividers [20]. The harmonic injection dividers are of interest because they can operate at smaller input signal amplitudes [20]. They depend on a free-running oscillator, and synchronizing the harmonics of the free-running frequency with an input source.

Static dividers have a trade-off between speed (and thus maximum input frequency) and power dissipation, and they can operate down to DC. Analog dividers, on the other hand, can operate at higher input frequencies with lower power consumption using only few transistors, but usually with limited input bandwidth (locking range).

2.3.1 ILFD

Oscillators depend on the non-linear behavior of circuit components to reach their steady-state. This non-linearity will enable harmonic components to appear together with the fundamental oscillation frequency. An input source can be injected at any of these harmonic frequencies, and synchronization of the oscillator output (i.e., injection locking) can take place. Locking range will decrease with higher order of the oscillator harmonic components because they have lower amplitudes.

Harmonic injection dividers are one group of injection-locked oscillators (ILOs). ILOs are divided into three categories; first-harmonic, sub-harmonic and super-harmonic ILOs. This depends on the relationship between the input signal frequency and the free-running oscillator frequency. The input frequency is the same as the oscillator free-running frequency in the first-harmonic ILO, lower and higher in the sub-harmonic and super-harmonic ILOs, respectively. So, harmonic injection dividers are super-harmonic ILOs, and they're also called injection-locked frequency dividers (ILFDs).

ILFDs can be modeled as shown in Fig. 2.21 [21]. The model includes a non-linear device that generates harmonic energy and a band-pass filter (BPF) to select one of these harmonics. The BPF output is then fed back to the non-linear device and oscillation keeps running independently. An input signal can then be injected in the oscillator signal path to be synchronized with the selected frequency component after the BPF.

As the input signal frequency changes, the output should follow this change. The range of input frequencies across which the oscillator is still locking and the signal is divided correctly is the locking range. A large locking range is important, as the frequency divider should cover the tuning range of the VCO plus a good margin. At high frequencies, larger margin is required to ensure proper operation within process, voltage and temperature (PVT) variations in the circuit.

ILFDs can be implemented using a cross-coupled LC oscillator generating the free-running signal. Traditional ILFDs [21] inject the input signal at the gate of the tail current transistor as shown in Fig. 2.22. They suffer from large input capacitance, small locking range and they operate at low input frequencies. This is due to the large tail transistor size. A shunt peaking inductor and capacitor were inserted at the common-source node of the cross-coupled pair to tune out the tail transistor output capacitance [22]. This solution improved the maximum frequency and locking range, but with the use of large area passives and the need for careful

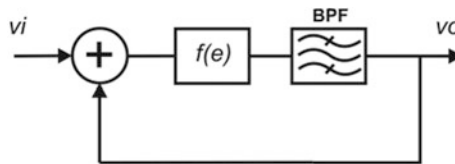
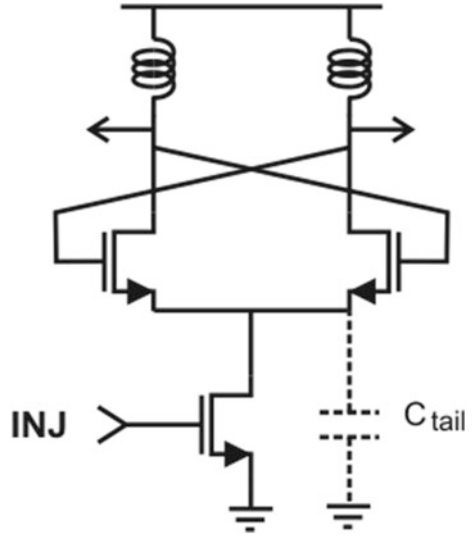


Fig. 2.21 Harmonic injection (injection-locked) frequency divider model [21]

Fig. 2.22 Conventional ILFD



adjustments of the inductor and capacitor values to get the required parasitic cancellation.

Another way to inject the input signal is through a transistor switch connected in parallel to the tank as shown in Fig. 2.23a [23–25]. The direct ILFD doesn't incorporate extra passives and provides a simpler circuit. The injecting signal modulates the oscillator output and the signal with frequency difference is selected by the tank. A block diagram explaining the behavior of the circuit is shown in Fig. 2.23b [26]. The output signal ($f_i/2$) is fed back and mixed with the input signal (f_i) generating the sum ($3f_i/2$) and difference ($f_i/2$) of both signal frequencies. The band-pass filter selects $f_i/2$ and passes it to the output, thus providing division. The transistor switch in Fig. 2.23a works as a drain-pumped mixer [27], and the cross-coupled pair with the tuning inductor form the feedback loop.

An analytical model for the direct ILFD is developed in [28]. The model depends on substituting the switching transistor (M_{in}) with passive elements. Figure 2.24 shows M_{in} and the relationship between the injected input voltage (V_{in}), the differential output voltage $V_{out\pm}$ and the channel current of M_{in} (I_{in}). The difference in phase shift between the input and output voltage signals is φ . The voltage and current waveforms for $\varphi = \pi/2$ and $\varphi = \pi/4$ are shown in Fig. 2.25. The locking range derived equation is as following:

$$\Delta\omega = 2g_{q,max}/C = 2\omega_0^2 L g_{q,max} \quad (2.17)$$

where L and C are the tank inductance and capacitance, respectively. $g_{q,max}$ is the equivalent injecting transistor output conductance ($g_{q,max} = I_q(\varphi)/2V_o$), which appeared as a result of modeling the injecting transistor as an inductor or a capacitor

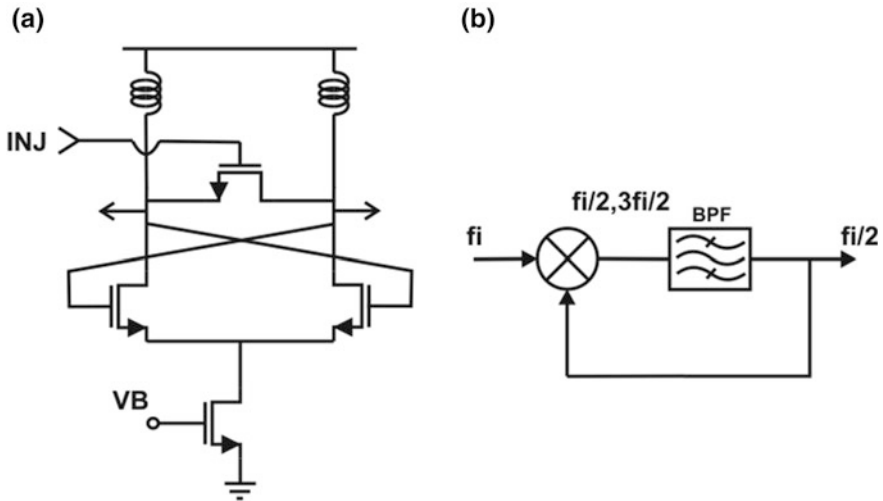


Fig. 2.23 Direct ILFD **a** circuit schematic and **b** equivalent model [26]

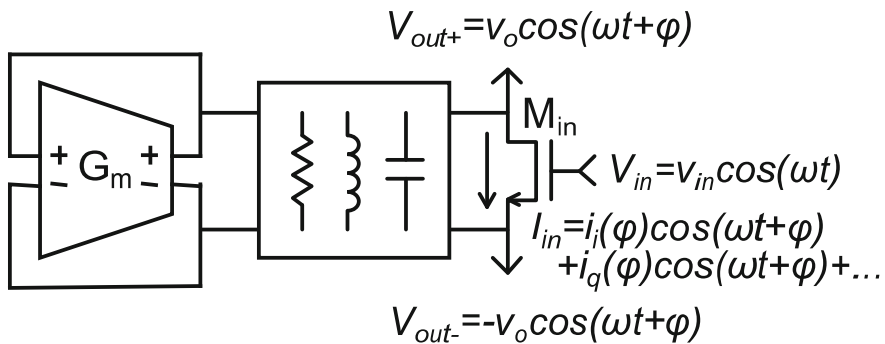


Fig. 2.24 Block diagram of the differential direct ILFD [28]

in parallel with a resistor. $I_q(\varphi)$ is the magnitude of the quadrature component of I_{in} , and v_o is the magnitude of the output voltage.

A Direct ILFD provides lower input capacitance and can operate at higher frequencies compared to the conventional one due to the smaller injecting transistor. Series peaking inductors were added in [29] to decrease the divider output capacitance and improve the locking range. Another approach that doesn't incorporate passive components is using two injecting transistors [26]. As shown in Fig. 2.26, the parasitic capacitance contribution of the injecting transistors to the divider output nodes is halved compared to using a single injecting transistor as in

Fig. 2.25 Voltage and current waveforms **a** at $\varphi = \pi/2$ and **b** $\varphi = \pi/4$ [28]

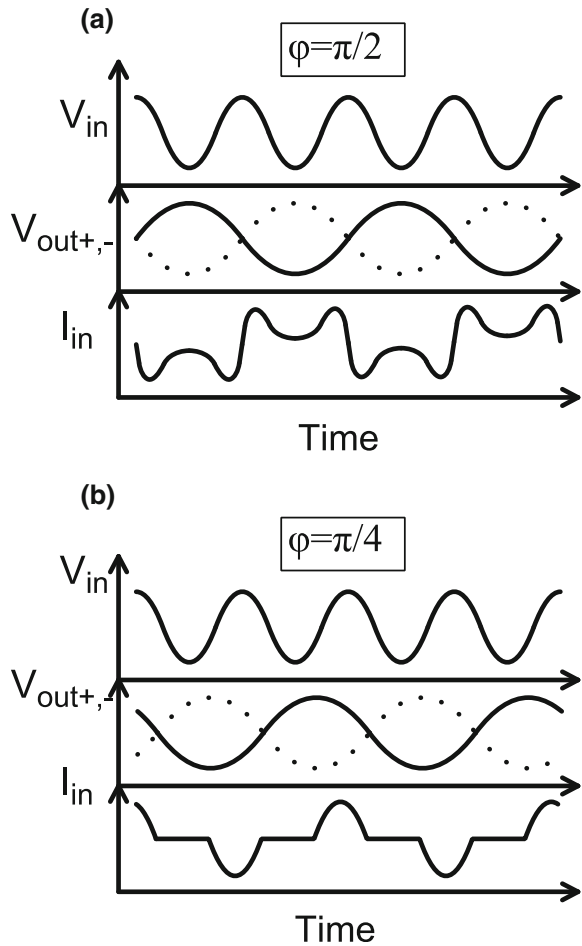
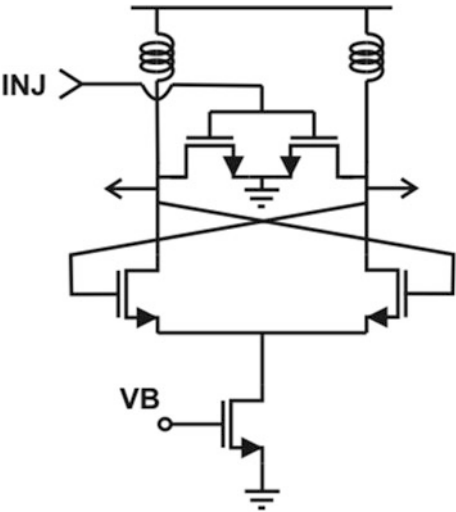


Fig. 2.23a. This allows doubling the injecting transistor sizes at the same output parasitic capacitance. Thus, the dual mixing technique is used to double the effective injecting conductance.

2.3.2 Static Divider

Digital static dividers at high frequencies depend in their implementation on CML circuits. It consists of three main parts, pull-up load, pull-down network (PDN) and a current source [30]. The circuit behavior is described depending on the logic blocks in the PDN and the input combination. The basic element of the static divider is a D-flip-flop (DFF). The DFF inverted output can be connected to the

Fig. 2.26 Dual-mixing direct ILFD circuit schematic



input terminal and the input signal connected to the clock terminal to form a divide-by-two.

Two level sensitive latches in master-slave configuration can be used to form the DFF required for the division. As shown in Fig. 2.27, the first stage is a gated D latch [31] that is transparent through a differential pair buffering the input signal when the CLK signal is high. When the CLK signal is low, the circuit is

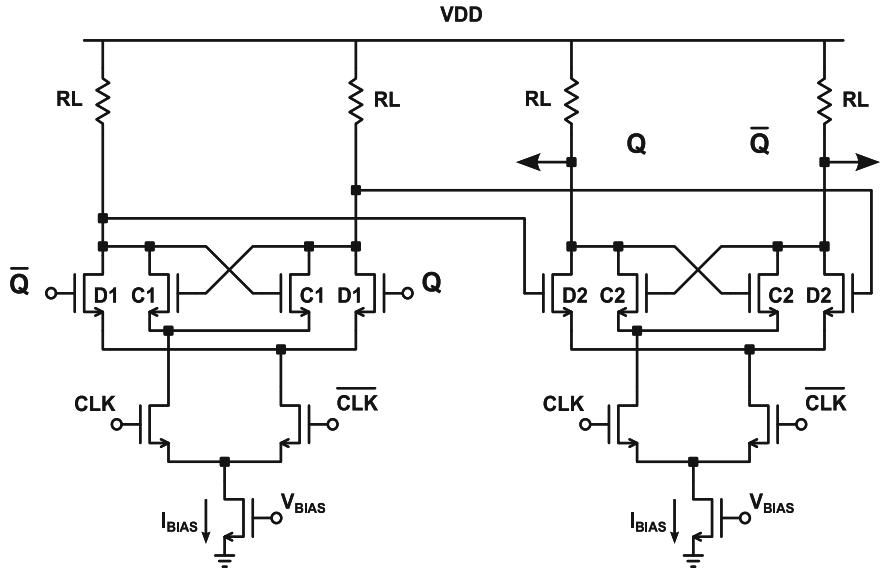


Fig. 2.27 Conventional CML latches in a master-slave configuration [32]

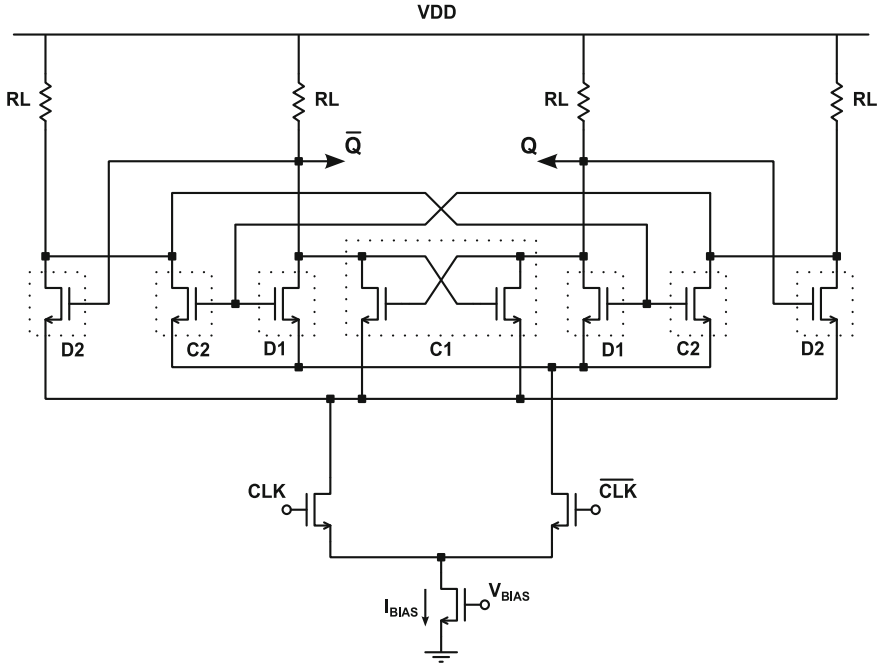


Fig. 2.28 High frequency CML divider (by two) [32]

non-transparent and the cross-coupled pair keeps the output state unchanged. The second stage works in the same way with inverted clock signals to implement the DFF.

The maximum operating frequency of the divider is limited by the CLK-Q time delay, which is a function of the total output capacitance and the load resistance, as well as the bias current. In [32], the cross-coupled pair size is reduced (to reduce the output capacitance) and the circuit is rearranged to have one tail transistor as shown in Fig. 2.28.

2.4 LNA

The low-noise amplifier (LNA) is usually used as the first block in the receiver front-end. It should add the lowest possible noise to the input signal. Noise degradation is usually measured with noise figure (NF). NF is a parameter that shows how much noise a block is adding to the system. Noise factor (F) is the linear equivalent of NF. LNAs should provide enough gain to overcome the noise figure of the following stages. This is suggested by Frii's formula, which calculates the system noise factor as following:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots \quad (2.18)$$

where G is the power gain of a block, and the subscript indicates the order of the block in the receiver. Assuming the LNA to be the first block in the system, Eq. 2.18 shows how the LNA (with noise factor F_1) is dominating the total noise, especially with a high gain (G_1) value.

The LNA input should be matched to 50Ω to provide the lowest possible reflections from the source. It shouldn't also distort the input signal. Signal distortion is caused by the non-linear behavior of a block. Non-linearity is usually specified by the third order input-referred intercept point (IIP3). The total IIP3 of a system can be calculated as following:

$$\frac{1}{IIP3_{\text{total}}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \frac{G_1 G_2 G_3}{IIP3_4} + \dots \quad (2.19)$$

Equation 2.19 shows that non-linearity of the latter stages are more effective due to the gain of the previous stages. So, the LNA distortion is not dominating the system non-linearity.

2.4.1 NF and IIP3

Noise figure of a linear two-port network as a function of the source admittance can be represented by:

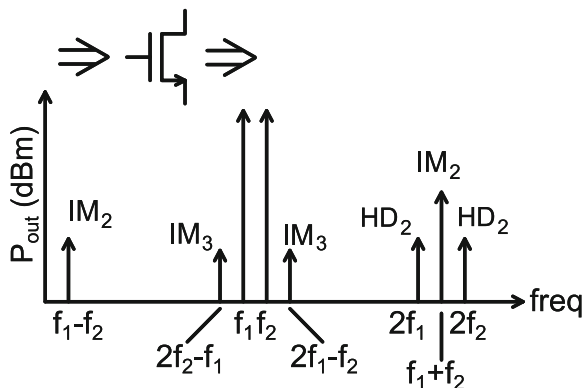
$$F = F_{\min} + \frac{R_n}{G_s} |Y_s - Y_{\text{opt}}|^2 \quad (2.20)$$

where F_{\min} is the minimum achievable noise factor, $Y_s (= G_s + jB_s)$ is the source admittance, Y_{opt} is the optimum load at which F reduces to F_{\min} (noise match condition) and R_n is the noise resistance defining the sensitivity of F to changes in the source admittance.

Note that these parameters can be related to circuit parameters, such as f_T , g_m and C_{gs} for a MOS transistor [33]. For minimum noise figure, F_{\min} should be minimized by choosing the correct bias point, and the LNA input should be matched to the optimum source impedance that gives the minimum noise factor (Z_{opt}). The source impedance for noise match is usually not 50Ω leading to the either a compromise between impedance and noise matching conditions or using a topology that allow for choosing the two impedances independently.

Non-linearity will cause additional tones to be generated at harmonic frequencies. If a signal with two frequency components at f_1 and f_2 enters the amplifier, more frequency components appear in the frequency band. Figure 2.29 shows the

Fig. 2.29 Two-tone excitation resulting tones (to the third-order) [34]



output spectrum with additional frequency components due to non-linearity (only to the third order).

Harmonic frequencies ($2f_1$, $2f_2$, $3f_1$, $3f_2$, ...) and second-order intermodulation components ($f_1 - f_2$ and $f_1 + f_2$) are of less importance as they can be easily filtered out. In a direct conversion receiver, ($f_1 - f_2$) falls in-band but is usually not effective when using differential circuits. The third-order intermodulation products (IM_3) are used in the definition of system non-linearity.

As shown in Fig. 2.30, the fundamental output tone eventually goes into compression with increasing input power. Linear extrapolation of the fundamental and IM_3 curves will intersect at the third-order intercept point (IP3). Referred to its input, the IIP3 is used to define non-linearity in a system. The point at which the fundamental tone is compressed with 1 dB is the -1 dB compression point (P-1 dB), which is also used to define the non-linearity of a system. The P-1 dB is

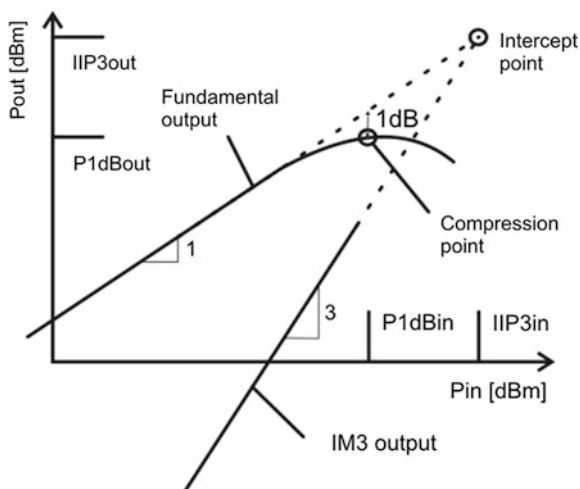


Fig. 2.30 Definition of important linearity parameters

easier to measure because it uses a single input tone, compared to the two-tone test for the IIP3 measurement. Input -1 dB compression point ($P-1$ dB,in) is around 10 dB lower than IIP3 [15], which gives an approximate value for the IIP3 when measured. Note that when dealing with a mixer, Fig. 2.30 is used with the x-axis (input power) at RF frequencies, while the y-axis (output power) is at the intermediate frequencies (IF) resulting after the frequency conversion.

2.4.2 LNA Topology

The commonly used topology for the LNA is based on a common-source transistor with inductive degeneration, as shown in Fig. 2.31a. If the small signal model of the transistor only contains an input capacitance C_{gs} and an output transconductance (Fig. 2.31b), the degenerated inductor can be transformed to the input using the β -transformation concept, leading to the following input impedance:

$$\begin{aligned} Z_{in} &= \frac{1}{j\omega C_{gs}} + j\omega L_{ss}[1 + \beta(\omega)] \\ &= \frac{1}{j\omega C_{gs}} + j\omega L_{ss} + j\omega L_{ss} \frac{\omega_T}{j\omega} \\ &= L_{ss} \frac{g_m}{C_{gs}} + j \left(\omega L_{ss} - \frac{1}{\omega C_{gs}} \right) \end{aligned} \quad (2.21)$$

where $\beta(\omega)$ is the current gain.

The input impedance contains a resistive part, which can be made equal to 50Ω , and a reactive part. As the inductor L_{ss} is chosen to vary the resistive part, the reactive part will usually have a non-zero value. As the input capacitance C_{gs} is a very small value, the reactive part is usually capacitive. An inductor inserted at the

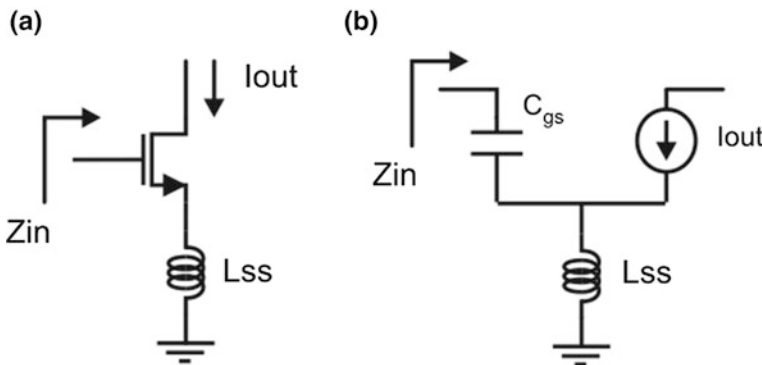
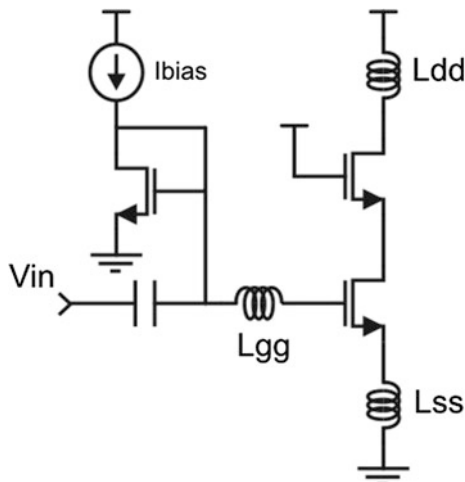


Fig. 2.31 **a** Inductively degenerated CS transistor and **b** small-signal model

Fig. 2.32 Single-ended cascode LNA using inductive degeneration



gate can be used to cancel the imaginary part of the input impedance, leaving only $50\ \Omega$ to match the source impedance of the LNA.

In our small-signal analysis to get the LNA input impedance, we neglected a lot of components. When added to the small-signal model, the transistor output resistance, through the overlap capacitance, can cause a significant drop in the real part of the input impedance [33]. This is due to the path created to the load of the LNA. A cascode transistor (maybe with a larger gate length leading to a higher output resistance) can be used to isolate the output load from the input circuit. This can keep good input matching properties for the LNA with the drawback of additional noise figure. The complete LNA can now be as shown in Fig. 2.32.

LNA design can now be simplified to adjusting the transistor width for noise match while keeping minimum gate length for maximum gain. Then, we can adjust L_{ss} to have real input impedance equal to the source impedance. And finally, L_{gg} can be chosen to cancel the imaginary part of the input impedance. Thus, impedance and noise matching can “ideally” be achieved.

2.5 Mixer

After the received signal is amplified by a low-noise block, a down-conversion mixer is then used to bring the RF signal down to low frequencies. Signal processing at baseband is much easier and economical from the chip area and power consumption point of views. So, the LO generated signal is multiplied by the low-noise amplified RF signal via the mixer, and the signal with frequency difference is filtered at baseband.

2.5.1 Main Parameters

As Eq. 2.19 suggests, the receiver blocks closer to baseband have more effect upon the total linearity. Thus, mixer distortion usually dominates the system non-linearity.

Two noise figure definitions are common in the mixer: single-sideband (SSB) and double-sideband (DSB) noise figures. In non-zero IF systems, the input frequency band includes the required RF signal and maybe another signal at the same distance from the LO signal as that between LO and RF signals. This is called the image frequency. Both frequencies, the RF and image, can down-convert to the lower IF frequency band, because they're at equal distance from the LO signal (on opposite sides). Noise from both frequency bands down-convert to the same frequency and contribute to the output noise. If we assume a noiseless mixer and useful information exists in the image band as well as the RF band, then the noise factor is $SNR_{in}/SNR_{out} = (P_i \times N_o)/(P_o \times N_i) = 1$ ($NF = 0$ dB). This is the way how DSB NF is calculated. In the SSB NF calculation, it is assumed that the image band doesn't include useful information (which is the usual case). So, the SNR at the output is doubled, because there is only noise coming from the image band. This will cause the noise factor to be 2 ($NF = 3$ dB). The two situations can be graphically illustrated as in Fig. 2.33. Unless otherwise specified, the DSB NF is usually used to define the noise figure of the mixer.

The input and output signals of the mixer are not at the same frequency. Thus, the conversion gain (CG) parameter is used in the mixer if it is providing gain (otherwise, conversion loss). CG is defined as the ratio of the desired IF output to the value of the RF input at a given LO signal level [3]. CG can be defined in the voltage domain (CG_v) or power domain (CG_p), and they're related through the ratio of the RF and IF port impedances, as shown in the following equations:

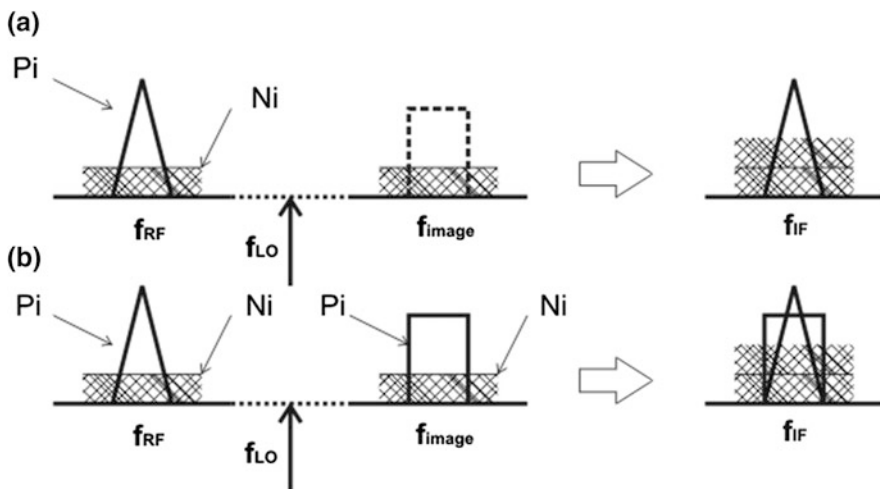


Fig. 2.33 Definition of **a** SSB versus **b** DSB NF

$$CG_v = \frac{V_{IF}}{V_{RF}} \quad (2.22)$$

$$CG_p = \frac{V_{IF}^2/R_{out}}{V_{RF}^2/R_{in}} = CG_v^2 \frac{R_{in}}{R_{out}} \quad (2.23)$$

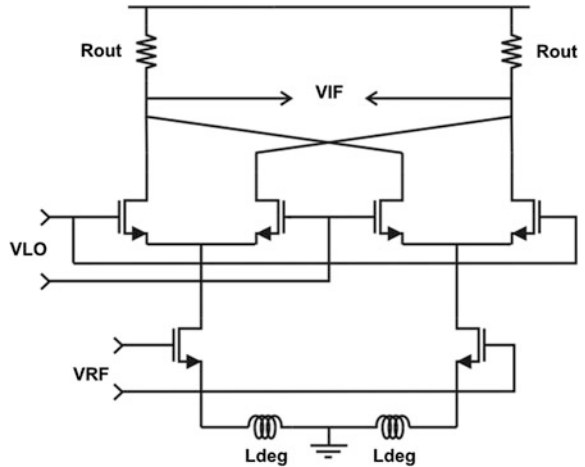
Mixer port impedances also should be defined unless the mixer interfaces remain internal to the IC. Isolation between ports is also important. For example, LO signal leaking to the RF port can reach the receiver antenna leading to unwanted signal radiation and additional frequency sidebands through the mixing action. Port-to-port isolation can thus be defined to avoid unwanted feed-through actions in the mixer.

2.5.2 Mixer Topology

Based on the way mixing is performed, mixers can be divided into three categories: single-ended, singly-balanced and doubly-balanced mixers [3]. Single-ended mixers depend on system non-linearity to generate second-order terms resulting in mixing behavior. This can be implemented using a single MOS transistor, which is characterized by the square law I-V behavior in saturation mode. Single-balanced mixers depend on multiplication in current domain to perform the mixing action [33]. One input (usually the RF signal) is single-ended and the (the LO signal) other is used differentially.

Double-balanced mixers use both input signals differentially to provide better port-to-port isolation. Active implementation of the double-balanced mixer employ two single-balanced mixers combined together. As shown in Fig. 2.34, the RF signal is first converted to current in a transconductor. The LO signal is then used to

Fig. 2.34 Active implementation of double-balanced mixer



drive the switching transistors. This is equivalent to multiplying the RF current signal with a square wave that depends on the LO signal. The LO signals enter the switching transistors in anti-parallel configuration, which allows the cancellation of all related LO components at the output. The fundamental frequency of the square wave, multiplied by the RF signal, will generate the required difference signal after low-pass filtering. The conversion gain for a square wave input can be calculated as following:

$$CG_v = \frac{g_m \times \frac{4}{\pi} \times R_{out}}{2} = \frac{2}{\pi} g_m R_{out} \quad (2.24)$$

where g_m is the transconductance of the RF transistor. The magnitude of fundamental component of the square wave is $4/\pi$, and the factor of 2 is because only the difference component at the output is considered.

If the LO signal is not large enough to switch the transistors, the conversion gain will be proportional to the LO input voltage. Very high LO swings can cause the switching transistors to go into the triode regime, leading to a degraded signal path for the RF input, and so a decreasing conversion gain.

Passive implementation of double-balanced mixers provides lower noise and higher linearity with the disadvantage of having conversion loss. As shown in Fig. 2.35, a CMOS passive mixer can be enhanced with an input g_m stage and an output Op-Amp stage to provide conversion gain [3]. The input node of the Op-Amp stage is settled at virtual ground, and the LO transistors work in triode region. If the LO signal causes the transistors to switch on and off, the mixer conversion gain can be, ideally, the same as that of the active one (Eq. 2.24). The output stage is a differential Op-Amp stage with resistive feedback, which has a limited bandwidth that can work as a LPF letting only the wanted difference signal to appear at the IF output.

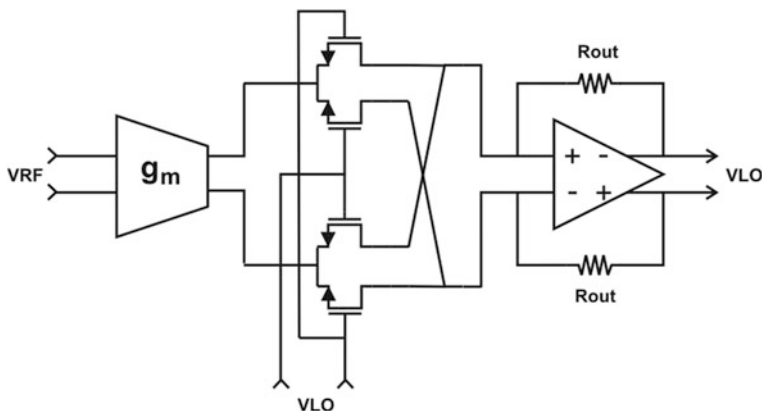


Fig. 2.35 Passive implementation of double-balanced mixer [3]

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