Chapter 2
ADCs Based on Successive Approximation

Chapter 1 discusses the various performance parameters and architectures of ADCs. The SAR ADC is presented as the ADC that is most frequently used in industrial applications, because it provides a high resolution (12–18 bit) at a medium sample rate (around 1 MSPS). This chapter therefore presents design and architectural basics and details regarding the components of a SAR ADC [1]. The principle block diagram is shown again in Fig. 2.1.

The input voltage V_{in} is frozen on a sample and hold stage, which is discussed in Sect. 2.1. Topics are the charge injection from the switches and the voltage coefficient from the sampling capacitor that will cause an offset error as well as linearity errors. The size of the sampling capacitor also determines the sampling noise.

The DAC, which is the heart of the SAR ADC, is explained in Sect. 2.2. Its offset and linearity are directly reflected in the ADC's transfer function. It is normally implemented with capacitors (CDAC) based on charge redistribution, where the capacitors are switched between the reference voltage and ground to set the appropriate output voltage. The switches to the capacitors are controlled via the comparator (Sect. 2.3) and the successive approximation register.

Settling issues and other error sources can be corrected towards the end of the conversion. A dynamic error correction is discussed in Sect. 2.4, which also opens the door for future correction schemes (Chap. 3). Settling effects of the reference are limiting the speed, noise and power consumption of the converter. Section 2.5 describes considerations regarding the reference topology.

Noise is an important specification. Different sources are analyzed and are summarized in Sect. 2.6. Finally Sect. 2.7 briefly discusses the limitations of state-of-the-art ADCs and leads to the modern research topics in Chap. 3.

F. Ohnhäuser, *Analog-Digital Converters for Industrial Applications Including an Introduction to Digital-Analog Converters*, DOI 10.1007/978-3-662-47020-6_2

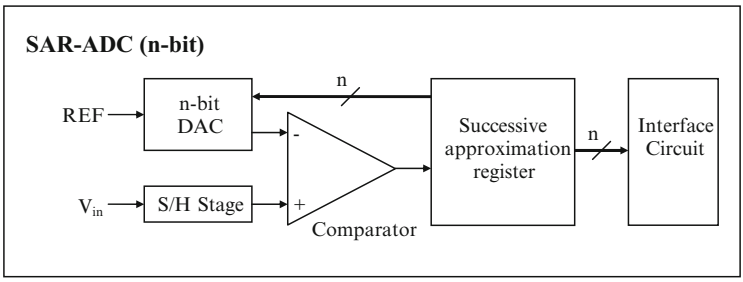

Fig. 2.1 Block diagram of a SAR ADC

2.1 Sample and Hold (S&H)

The S&H circuit is basically a capacitor, which is charged to the input voltage during the sampling time. For the conversion, the input voltage V_{in} is frozen on the capacitor by opening the input switch, which is typically realized as CMOS switch (see Fig. 2.2). Unfortunately, the charge injection of the input switch will generate an offset, which is heavily dependent on the input voltage.

In addition, the on-resistance of the input switch is voltage dependent. The on-resistance is forming a voltage dependent low-pass filter together with the sample capacitor and the parasitic capacitance of the switch. The voltage dependency causes distortion that is very significant at higher signal frequencies. The ratio of the transistor width to length $\frac{W}{L}$ of the input switch has to be large to minimize this effect. The high $\frac{W}{L}$ will on the other side increase the charge injection.

The circuit can therefore be improved with the structure in Fig. 2.3. The charge is frozen with the switch sw_1 to ground. This transistor remains at the same operating point independent of the input voltage, so that the on-resistance is constant and does not affect distortion. The width W of sw_1 can remain small to minimize charge injection. After freezing the charge with the small switch sw_1, the big input switch sw_2 can be opened without adding further charge to the capacitor. Not that sw_1 is called hold switch.

Finally, sw_3 is connecting the capacitor back to ground. This way, the capacitor is connected to a defined potential. As the voltage across the capacitor is frozen, the potential at the node V_{sample} equals $-V_{in}$.

The S&H from Fig. 2.3 will generate a good linearity, as the charge injection of sw_1 is now independent of the input voltage. However, it will still cause a severe offset error, which will change with the supply voltage and temperature.

This problem can be solved, if the sampling is performed fully differential like shown in Fig. 2.4.

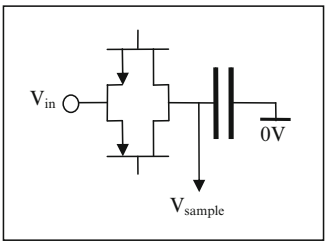

Fig. 2.2 Basic S&H circuitry

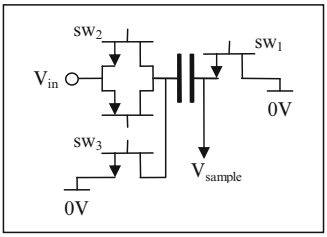

Fig. 2.3 Double switch S&H

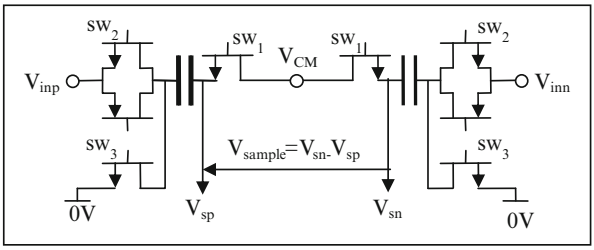

Fig. 2.4 Fully differential S&H circuit

The voltage $V_{sp/n}$ after freezing the input voltage $V_{inp/n}$ can be calculated to

$$V_{sp/n} = V_{CM} - V_{inp/n} + V_{charge}$$

V_{charge} is expressing an offset caused by the charge injection of the hold switches. A fully differential voltage is sampled, which can be calculated to

$$V_{sample} = V_{sn} - V_{sp} = V_{inp} - V_{inn}$$

Identical charge is injected by the two hold switches into V_{sp} and V_{sn}. The charge injection is eliminated in the differential voltage V_{sample}. This structure further allows adding a common-mode voltage V_{CM}, which can be used to select the ideal common-mode operating point of the comparator.

On typical 5 V (or less) CMOS processes, the on-resistor is low enough to realize the input switch sw_2 with a standard CMOS switch. The W ratio of the NCH and the PCH transistor is chosen to receive the most constant on-resistance over the input

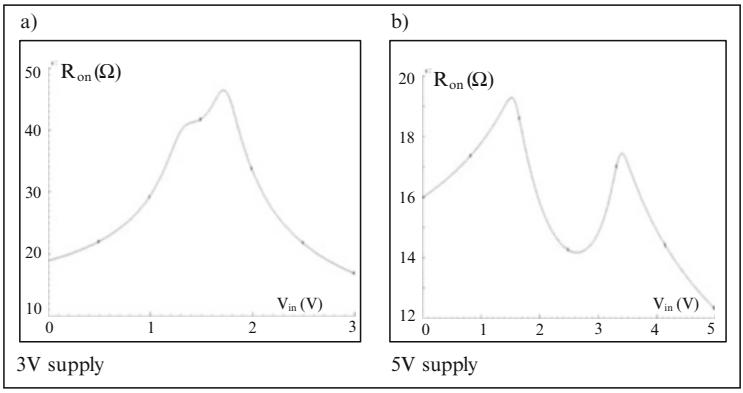

Fig. 2.5 Typical on-resistance of a CMOS sample switch at (**a**) 3 V supply and (**b**) 5 V supply

voltage as shown in Fig. 2.5, where the transistors were optimized for 5 V operation.

ADCs with a high voltage input range (+/−10 V) need to use high voltage input transistors, which show a severe body effect together with a high on-resistance and an essential parasitic capacitance. This causes high distortion. In these cases, a method is used, where the gate-source voltage of the input switch is biased to a constant voltage during the sampling phase. This method is called bootstrapping. The on-resistance of such switches is compared in Fig. 2.6. Note that bootstrapping comes with a significant circuit overhead.

In any case, the sample and hold stage fully relies on the quality of the capacitor. The voltage coefficient of standard Poly-NWell capacitors is so high that the integral linearity suffers. High-end ADCs require processes with special capacitors like poly-poly capacitors, metal-poly capacitor or metal-metal capacitors. Effects of the voltage coefficient are discussed in Sect. 3.4 [2].

A sample and hold circuitry can be considered as an *RC* circuitry, where the *R* is the on-resistance R_{on} of the input switch and the *C* the sample capacitor C_s. Every resistor is adding thermal noise [3] with the density n_{Ron} of

$$n_{Ron} = \sqrt{4kTR_{on}} \tag{2.1}$$

In this equation, *T* is expressing the temperature and *k* the Boltzmann constant.

Thermal noise is equally distributed over the whole frequency span. The bandwidth of the input circuitry however is limited to $f_{-3\text{dB}} = \frac{1}{2\pi R_{on}C}$. Even if the noise is suppressed for frequencies above $f_{-3\text{dB}}$, it is not eliminated as shown in Fig. 2.7.

Integrating the frequency responds of the first order low-pass filter will effectively result in $\Delta f = \frac{\pi}{2} \cdot f_{-3\text{dB}}$ [3], so that the rms-voltage of the low-pass filtered noise n_f during the sampling process $V_{rms,samp}$ can be calculated to

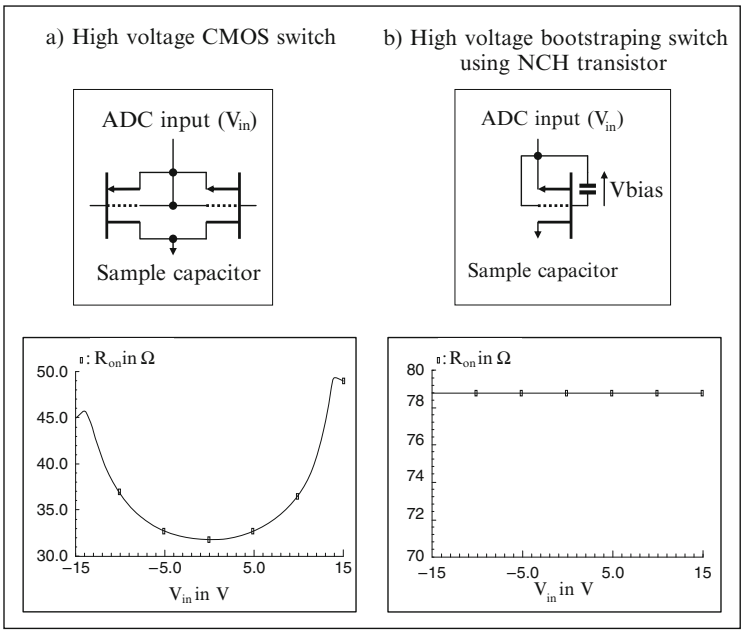

Fig. 2.6 On-resistance of high voltage switches during sampling

$$V_{rms,samp} = \sqrt{\int_0^\infty n_f^2 df} = \sqrt{n_{Ron}^2 \cdot \Delta f} = \sqrt{\frac{kT}{C}} \tag{2.2}$$

The sampling noise can only be influenced with the size of the sampling capacitor. If the input range of the ADC is reduced by a factor of 2, then the size of the LSB is also divided by two and the noise needs to be lowered by a factor of 2. For the sampling noise, this is only possible by increasing the sampling capacitor by a factor of 4.

New CMOS technologies with minimum gate lengths have the disadvantage of small supply voltages, which would limit the input voltage range. Several modern analog processes therefore leave the gate length between 0.35 µm (3.3 V) and 0.6 µm (5 V) and concentrate on other parameters like transistors with low 1/f noise, capacitors with low voltage coefficients or resistors with low temperature coefficient.

Note that the sample and hold circuitry from Fig. 2.4 is sampling on two sample capacitors, so that the noise needs to be considered twice. The rms-voltage needs to be multiplied with the square-root of two. The differential architecture however can be used to increase the signal amplitude by a factor of 2.

In the architecture from Fig. 2.4, the hold switch is connected to a common-mode voltage V_{CM}. Also the common-mode voltage is a potential noise source.

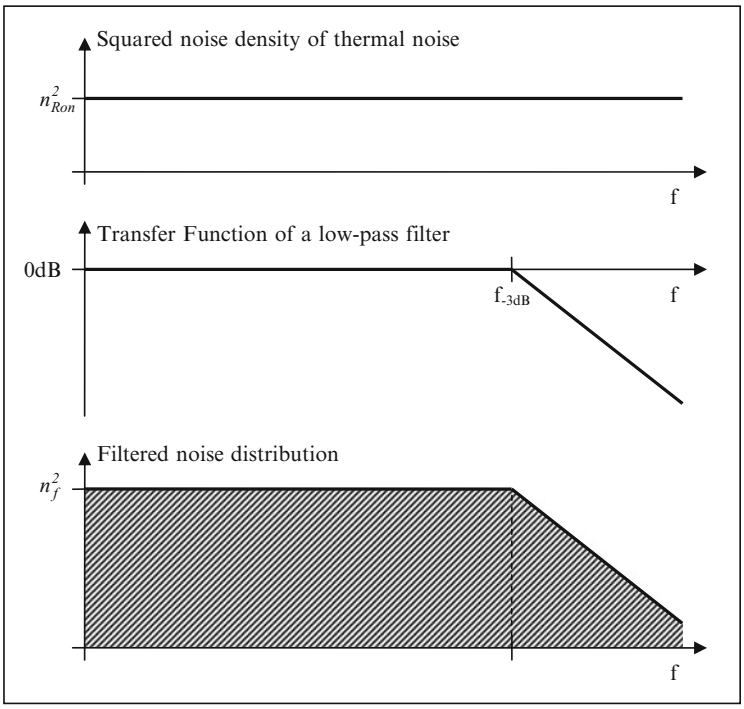

Fig. 2.7 Illustration of thermal noise shaped by a first order filter

However, the bandwidth of the voltage source is typically much smaller than the bandwidth of the sample and hold structure. This will cause the noise to be common to the positive and the negative sample and hold capacitor. The common noise will be suppressed by 60–80 dB by the common-mode rejection of the fully differential DAC and the fully differential comparator.

2.2 Capacitive DAC

The DAC is the heart of the SAR converter. Its differential and integral non-linearity will directly be reflected in the transfer function of the ADC. Typical DAC structures are the string DAC, the R – 2R structure or the current steering DAC (see Chap. 7). All of them show limitations in speed and performance [4].

Ideal is a capacitive DAC (CDAC), which is based on the principle of charge redistribution. An example for 3 bits is shown in Figs. 2.8, 2.9, 2.10 and 2.11.

In Fig. 2.8, all capacitors are connected to the input voltage V_{inp} for sampling. The charge, which is stored across the capacitors, can be calculated to

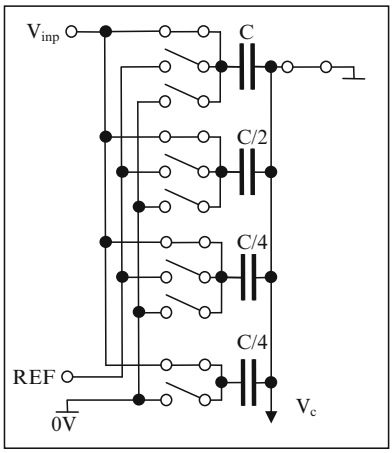

Fig. 2.8 CDAC during sampling process

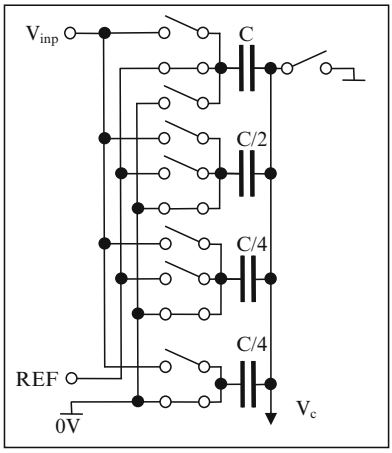

Fig. 2.9 CDAC during MSB decision

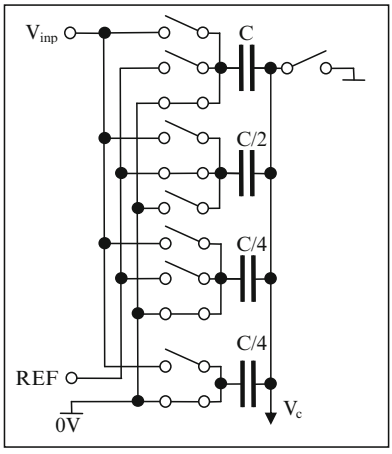

Fig. 2.10 CDAC during MSB-1 decision

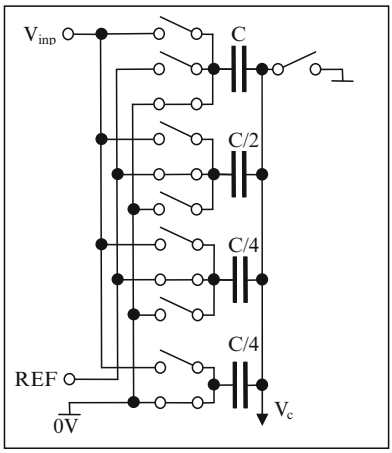

Fig. 2.11 CDAC during MSB-2 decision

$$Q_{samp} = \left(C + \frac{C}{2} + \frac{C}{4} + \frac{C}{4}\right) \cdot V_{inp} = 2C \cdot V_{inp}$$

The charge is frozen by opening the hold switch between V_c and ground. Then, the input switches coupling to V_{inp} open. For the evaluation of most significant bit (MSB), the capacitor of the size C is connected to the reference voltage REF, all other capacitors are connected to ground (see Fig. 2.9). The charge across the capacitors can be calculated to

$$Q_{MSB} = C \cdot (REF - V_c) + \left(\frac{C}{2} + \frac{C}{4} + \frac{C}{4}\right) \cdot (0\ \text{V} - V_c)$$

Q_{samp} and Q_{MSB} are equal, as the charge is frozen. This will lead to

$$2C \cdot V_{inp} = C \cdot (REF - V_c) + C(0\ \text{V} - V_c)$$

The equation can be solved to

$$V_c = \frac{REF}{2} - V_{inp}$$

V_c is connected to the negative comparator input, the positive comparator input is connected to ground. The comparator will therefore compare, if the voltage V_c is less or equal than 0 V

$$V_c = \frac{REF}{2} - V_{inp} \leq 0\ \text{V} \Leftrightarrow \frac{REF}{2} \leq V_{inp}$$

If the comparator output is 1, then the input voltage was higher than half of the reference voltage. For the MSB-1 evaluation, C would remain at REF and $\frac{C}{2}$ would

switch from ground to REF. In the example of Sect. 1.2.2, the reference was 4 V and the input voltage 1.9 V. V_{in} would be less than half the reference, so that the comparator output and therefore the MSB would be 0. The capacitor C will connect to ground, $\frac{C}{2}$ to the reference voltage.

Figure 2.10 shows the CDAC during the next bit decision. The total charge can now be calculated to

$$Q_{MSB\text{-}1} = \frac{C}{2} \cdot (REF - V_c) + \left(C + \frac{C}{4} + \frac{C}{4}\right) \cdot (0\ \text{V} - V_c)$$

Again, the charge is identical to Q_{samp}, so that

$$V_c = \frac{REF}{4} - V_{inp} \leq 0\ \text{V} \Leftrightarrow \frac{REF}{4} \leq V_{inp}$$

The comparator will now decide, if the input voltage was higher than a quarter of the reference. In the example of $V_{inp} = 1.9$ V, this would be the case, so that the comparator output and therefore the MSB-1 is one. The capacitor $\frac{C}{2}$ remains connected to the reference voltage and the next bit capacitor is switching from ground to the reference as shown in Fig. 2.11, which will lead to

$$Q_{MSB\text{-}2} = \left(\frac{C}{2} + \frac{C}{4}\right) \cdot (REF - V_c) + \left(C + \frac{C}{4}\right) \cdot (0\ \text{V} - V_c) \quad \text{or}$$
$$V_c = \frac{3REF}{8} - V_{inp} \leq 0\ \text{V} \Leftrightarrow \frac{3REF}{8} \leq V_{inp}$$

For the example, this is also true, so that the MSB-2 is also one. The 3 bit digital output of the ADC would be 011.

2.2.1 Basic CDAC Architectures

For converters with more than 10 bits, the ratio between the MSB capacitor and the LSB capacitor is getting significant due to the binary scaling (see Fig. 2.12). A serial capacitor can be placed between an MSB and an LSB capacitor array as shown in Fig. 2.13. The serial capacitor is also called scale-down capacitor. The solution with the scale-down capacitor has a larger LSB capacitor and less total capacitance if compared to the straight binary CDAC. Better matching can be achieved at a smaller CDAC size.

An alternative solution is shown in Fig. 2.14, where the LSBs are implemented by adjusting the voltage applied to the smallest capacitor. A resistive divider, also called string DAC, is used to tune the reference voltage, so that V_c changes in LSB steps.

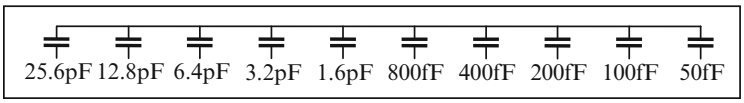

Fig. 2.12 Capacitor array within a standard binary weighted 10 bit CDAC

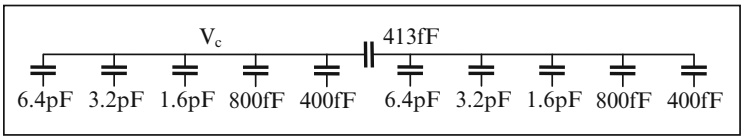

Fig. 2.13 Capacitor array of a 10 bit CDAC with serial scale-down capacitor

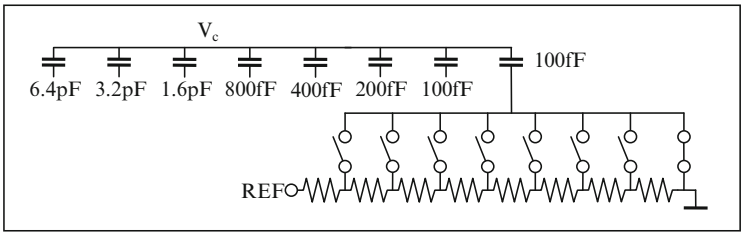

Fig. 2.14 CDAC combined with a resistive string DAC for the LSB evaluation

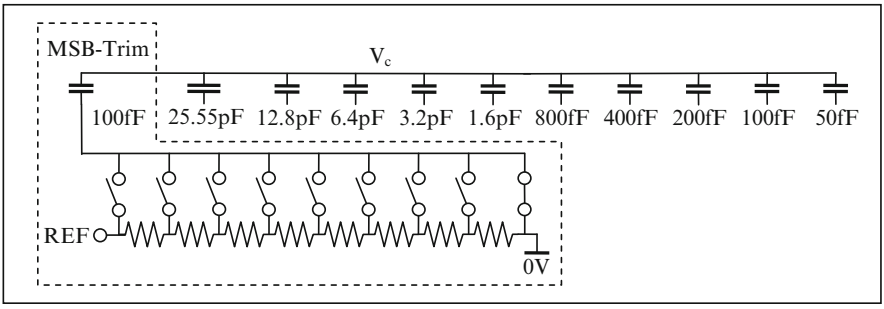

Fig. 2.15 MSB trim circuitry using a resistive string DAC coupling through a trim capacitor

Capacitors typically match up to 0.1 %, so that a 10 bit accuracy can directly be achieved. If the resolution is more than 10 bits, then a calibration or trim solution is required.

Figure 2.15 shows a trim solution for the MSB capacitor. The MSB capacitor is reduced by a value corresponding to one LSB and a trim capacitor of 2 LSBs is switched in parallel. If this trim capacitor is charged to half the reference voltage synchronously with the MSB capacitor switching to *REF*, then the MSB capacitor has the same charge redistribution than before. But now, the weight can be changed by either trimming or calibrating the ADC. The weight of the MSB capacitor can be

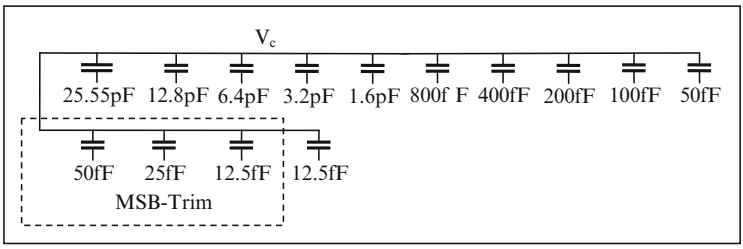

Fig. 2.16 MSB trim circuitry using additional capacitors

increased by 1 LSB, if the trim capacitor is charged to the reference voltage. In the same way, the weight is reduced by one LSB, if the 100 fF trim capacitor remains constantly at ground.

The disadvantage of this structure is that the reference has to drive a DC current through the string DAC, which is adding to the power consumption. This is especially true for 16 bit and 18 bit ADCs, where several bits are trimmed. An alternative is a capacitive trim, like shown in Fig. 2.16.

Programmed trim capacitors are switching in parallel with the MSB. The small size of the trim capacitors is causing an issue, which is discussed later.

2.2.2 Trim Solutions

Trim solutions are in common use since several decades [5–7]. The typical approach was laser cutting of thin film resistors or links, which are made out of poly or metal, during wafer probing. Unfortunately, the assembly process will shift the measured parameters. This is due to the mechanical packaging stress, but also to an inhomogeneous dielectric of the packaging material, which is called molding compound. This will change the parasitic capacitors inside the CDAC and influence the DNL of particular bits up to 6 LSB for 16 bit ADCs. In addition, the packaging shift has a significant variation associated, so that a perfectly trimmed CDAC is nearly impossible. Perfectly trimmed ADCs are therefore selected as high-grades, which are sold at a higher price.

The laser cutting can be done anywhere on the die and does not require additional circuitry. Therefore, the fuse can also be placed in the wiring, and capacitors can be disconnected easily and very space effectively.

In-package trim solutions were designed, where the trim information is either stored by blowing fuses electrically or by adding memory like EPROM (Electrically Programmable ROM) or OTPs (One-Time-Programmable-ROM).

The approach with the electrically blown fuse is very similar to the laser cutting of fuses. The only difference is that the fuse is blown with a high current flow instead of the laser. Unfortunately, this requires the fuse to be connected to a low

impedance transistor and a low impedance ground or supply. Due to the parasitic capacitance of the transistor, the electrically blown fuse can mainly be used to generate digital control signals. Note that fuses can be implemented on a standard CMOS process.

The electrically blown fuses and the OTPs generate digital signals. These signals are used to control switches for trim solutions. Both trim solutions from Figs. 2.15 and 2.16 can be realized with this technique.

Typically, only the matching of the binary weighted bit capacitors was trimmed. But much more than that is possible. Offset, gain and CMRR can also be adjusted inside the capacitor array. A general calculation is performed below on a fully differential CDAC, which will explain the various trim effects.

For the calculation, the CDAC in Fig. 2.17 is used. In most cases, the input voltage is directly sampled on the bit capacitors, but here the sampling capacitors $C_{sn,p}$ are separated from the bit capacitors, which are called $C_{1n,p}$ to $C_{Nn,p}$. The resolution of the CDAC is also kept general to N-bit. The input voltage range is bipolar. The fully differential topology will keep the charge injection of the hold switches (sw_{hp} and sw_{hn}) symmetrical. C_{jn} and C_{jp} ($j\epsilon\{1, \ldots, N\}$) are binary weighted ($C_{jn,p} = C \cdot 2^{-(j-1)}$), where C_{1n} expresses the capacitor for the MSB (Most Significant Bit or bit 1) and C_{Nn} the capacitor for the LSB (Least Significant Bit or bit N).

In sample mode, the inputs V_{inp} and V_{inn} are coupled to the sample capacitors C_{sn} and C_{sp}, while the remaining CDAC capacitors $C_{jn,p}$ are switched to 0 V. The nodes V_{cn} and V_{cp} that short the other pin of all capacitors is connected to a common-mode voltage V_{CM}, which can be used to set an anticipated common-mode operating point

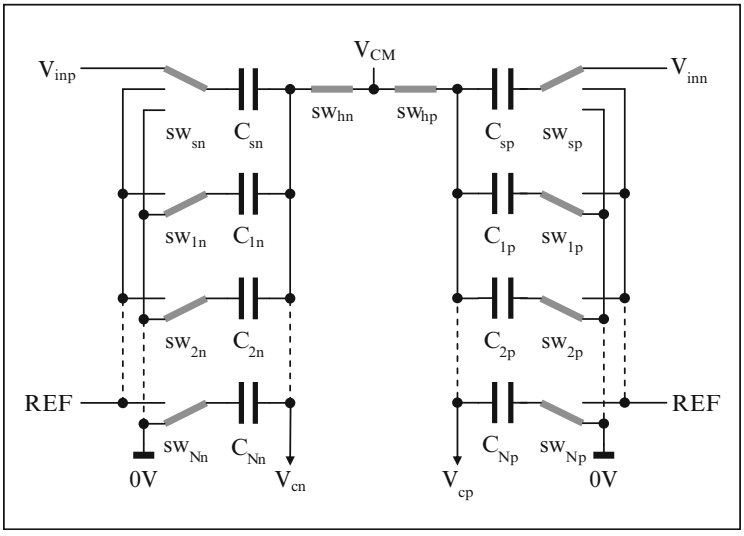

Fig. 2.17 Fully differential CDAC used below to calculate various trim schemes

of the comparator. The sampled charge Q_{sp} and Q_{sn} on the nodes V_{cp} and V_{cn} can be evaluated to

$$Q_{sp,n} = C_{sp,n} \cdot \left(V_{CM} - V_{inn,p}\right) + \sum_{j=1}^{N} C_{jp,n} V_{CM} \tag{2.3}$$

The charges Q_{sp} and Q_{sn} are frozen by opening the switches sw_{hn} and sw_{hp}, which in sample mode work at the equal operating point V_{CM} and ideally generate an identical charge injection. Thanks to the equal operating point, the switches further only show a minor influence to the ADC's distortion and can be minimized particular if V_{CM} is chosen to be close to 0 V or VDD, where either the NCH or respectively the PCH transistor are conducting well. The offset error and offset error drift can be optimized. After opening the sample switches, the capacitors C_{sn} and C_{sp} should be disconnected from the input nodes V_{inp} and V_{inn} and should in this example be conducted to the reference voltage REF for the complete conversion. The bit capacitors C_{jn} ($j \epsilon \{1, \ldots, N\}$) are now toggling between REF and 0 V based on the normal SAR algorithm. For the following calculation, the charge at the bit decision i should be named Q_{ip} and Q_{in}. The state of a particular bit switch $sw_{jn,p}$ ($j \epsilon \{1, \ldots, N\}$) should be expressed by x_{jp} and x_{jn}. $x_{jn,p} = 0$ indicates that the switch $sw_{jn,p}$ connects the capacitor $C_{jn,p}$ to 0 V. The capacitor $C_{jn,p}$ shall conduct to the reference REF with $x_{jp,n} = 1$.

$$Q_{ip,n} = C_{sp,n} \cdot \left(V_{cp,n} - REF\right) + \sum_{j=1}^{N} \left(C_{jp,n} \cdot \left(V_{cp,n} - x_{jp,n} \cdot REF\right)\right) \tag{2.4}$$

The charge after sampling and during a bit decision i equal each other $Q_{sp,n} = Q_{ip,n}$, as V_{cp} and V_{cn} are both in high impedance state during the conversion. Equations (2.3) and (2.4) are set equal and are solved for V_{cp} and V_{cn}. In the next step, the differential comparator input $V_c = V_{cp} - V_{cn}$ is evaluated. The comparator then decides if $V_c > 0$. The above steps are expressed in Eq. (2.5):

$$\begin{aligned} & V_{inp} \frac{C_{sn}}{C_{sn} + \sum_{j=1}^{N} C_{jn}} - V_{inn} \frac{C_{sp}}{C_{sp} + \sum_{j=1}^{N} C_{jp}} \\ & > REF \left[\frac{C_{sn} + \sum_{j=1}^{N} \left(x_{jn} \cdot C_{jn}\right)}{C_{sn} + \sum_{j=1}^{N} C_{jn}} - \frac{C_{sp} + \sum_{j=1}^{N} \left(x_{jp} \cdot C_{jp}\right)}{C_{sp} + \sum_{j=1}^{N} C_{jp}} \right] \end{aligned} \tag{2.5}$$

Ideally, the capacitance of a capacitor on the positive CDAC side equals the capacitance of the respective capacitor on the negative side ($C_{sn} = C_{sp}$ and

$C_{jn} = C_{jp}$). The bit capacitors should further be binary weighted ($C_{jn} = C \cdot 2^{-(j-1)}$ with $j \epsilon \{1, \ldots, N\}$). In this particular example, the sample capacitors should have the capacitance C as well ($C_{sn} = C_{sp} = C$).

2.2.2.1 DNL Trim

The DNL expresses the variance of a particular code from its ideal width of 1 LSB. The following calculation will prove that the DNL is dependent on the matching of the binary weighted bit capacitors. Most critical is the matching of the MSB capacitors (here C_{1n} and C_{1p}), which have to match to the sum of the bit capacitors $C_{jn,p}$ ($j \epsilon \{2, \ldots, N\}$). The code width is defined by two code transitions that can be calculated with Eq. (2.5). For the DNL of the MSB, the upper code transition V_{tr1} is defined with $x_{1n} = 1$ and $x_{jn} = 0$ ($j \epsilon \{2, \ldots, N\}$) and the lower code transition V_{tr2} with $x_{1n} = 0$ and $x_{jn} = 1$. In this example, the ADC should operate in single-ended mode, so that x_{1p} is always 1 and $x_{jp} = 0$ ($j \epsilon \{2, \ldots, N\}$). At a code transition, the ADC transfer function crosses from one ADC output code to the next. This means that at the critical bit decision in the course of the conversion the comparator just changes from output 0 to output 1. This can only be the case if the comparator input $V_C = 0$ V. Consequently, the Eqs. (2.6a) and (2.6b) use the equal sign. The following calculation should further show the effect of a mismatch ΔC of C_{1n}, so that $C_{1n} = C + \Delta C$

$$V_{tr1p}\frac{C}{3C + \Delta C - C_N} - V_{tr1n}\frac{C}{3C - C_N} = REF \cdot \left(\frac{2C + \Delta C}{3C + \Delta C - C_N} - \frac{2C}{3C - C_N}\right) \tag{2.6a}$$

$$V_{tr2p}\frac{C}{3C + \Delta C - C_N} - V_{tr2n}\frac{C}{3C - C_N} = REF \cdot \left(\frac{2C - C_N}{3C + \Delta C - C_N} - \frac{2C}{3C - C_N}\right) \tag{2.6b}$$

If ΔC is neglected in the denominator, then

$$\begin{aligned} V_{tr1} &= V_{tr1p} - V_{tr1n} = REF \cdot \frac{\Delta C}{C} \\ V_{tr2} &= V_{tr2\,p} - V_{tr2n} = -REF \cdot \frac{C_N}{C} = -1 \text{ LSB} \\ DNL_{MSB} &= V_{tr1} - V_{tr2} - 1 \text{ LSB} = REF \cdot \frac{\Delta C}{C} \end{aligned} \tag{2.7}$$

The capacitor mismatch ΔC is directly proportional to the DNL. It can be corrected by switching additional trim capacitors with the absolute value of ΔC in parallel to the bit of interest if ΔC is negative or anti-parallel to the bit of interest is positive,

which here is the MSB. The implementation of the in-package trim method is further explained in Sect. 2.2.3.

Please note that parasitic capacitance at the nodes V_{cp} and V_{cn} will add to the denominator similar as the sampling capacitors. If these capacitors remain at a constant potential all the time, then they will lower the voltage range at the comparator input, but will not influence the linearity, gain or offset. However, the lower voltage range will make the comparator noise more significant, which will reduce the SNR.

2.2.2.2 Gain Trim

Gain and offset can certainly be calibrated and corrected in the digital domain, but this would go on the cost of resolution. If for example a total gain adjustment needs to have a range of 20 % and an offset adjustment of another 5 %, then 25 % of the ADCs input range cannot be used, because they need to be reserved for the signal variations. The ADC retains its total input range, if offset and gain are corrected in the analog domain.

The absolute gain and offset errors of an application are adding up much more than the values of the ADC. Some ADCs on the market [8] therefore have an offset and gain correction implemented that can be controlled by the user through internal registers that are set through the digital interface.

The gain of the ADC is determined by the ratio of the sampling capacitor $C_{sn,p}$ to the sum of bit capacitors $C_{jn,p}$ in the CDAC, which are switching between ground and the reference. This can be proven by calculating the positive full-scale (PFS) and negative full-scale (NFS) with Eq. (2.5). For the PFS, x_{jn} all equal one ($x_{jn} = 1$, $j \epsilon \{1, \ldots, N\}$) and x_{jn} are all zero for the NFS ($x_{jn} = 0, j \epsilon \{1, \ldots, N\}$). Again the ADC should operate in single-ended mode, so that x_{1p} is always 1 and $x_{jp} = 0$ ($j \epsilon \{2, \ldots, N\}$). The calculation assumes that the capacitors on the positive side equal the capacitors on the negative side ($C_{sn} = C_{sp} = C_s$ and $C_{jn} = C_{jp} = C_j$)

$$V_{PFS} = REF \cdot \frac{\sum_{j=2}^{N} C_j}{C_s} \tag{2.8a}$$

$$V_{NFS} = -REF \cdot \frac{C_1}{C_s} \tag{2.8b}$$

$$V_{PFS} - V_{NFS} = REF \cdot \frac{\sum_{j=1}^{N} C_j}{C_s} \tag{2.8c}$$

The input range is proportional to the reference and to the ratio of the sum of the bit capacitors C_j to the sampling capacitor C_s. The gain of a SAR ADC can be adjusted by connecting more or less capacitors to the input pins V_{inp} and V_{inn} during

sampling. It is also possible to sample directly on bit capacitors C_{jn} and C_{jp}. Note that the ratio of sample capacitor to the bit capacitors on the negative side has to be identical to the same ratio on the positive side.

$$\frac{C_{sn}}{\sum_{j=1}^{N} C_{jn}} = \frac{C_{sp}}{\sum_{j=1}^{N} C_{jp}}$$

Otherwise, the gain on the positive CDAC array will be different than the gain of the negative array. If the common-mode voltage of the input varies, then it is processed differently on the two sides and will affect the common-mode rejection, which is shown later on.

To increase the input voltage range of the ADC, C_s has to be reduced, which is expressed in Eq. (2.8c). In the previous examples, the sampling was always performed on all CDAC capacitors, so that the input range resulted in 0 V to *REF*. If only the MSB capacitor is used for the sampling, then the input range would be 0 V to 2 *REF*. Several products are on the market, which use this method to switch between a variety of input ranges (±10 V, ±5 V, ±2.5 V, 0–5 V) [9, 10].

Equation (2.8c) can also be used to trim the ADC gain. In the example of Fig. 2.18, capacitors are added to lower the input voltage range by 1 LSB and 2 LSB. Therefore, they need to be connected to the input voltage during sampling and to the reference voltage or ground during the whole conversion.

Note that the scale-down capacitor C_{sd} needs to be readjusted, if additional capacitors are added to the scale-down array.

Originally, the value of the scale-down capacitor was estimated, so that the series capacitance of the scale-down capacitor and the sum of capacitors inside the scale-down array $C_{LSB-array}$ were equal to the smallest capacitor in the MSB array ($C_{MSB\text{-}4} = 400$ fF). In the CDAC from Fig. 2.13, the sum of the capacitors in the LSB array added up to 12.4 pF.

$$\frac{1}{C_{sd}} = \frac{1}{C_{MSB\text{-}4}} - \frac{1}{C_{LSB-array}} \Rightarrow C_{sd} = 413 \text{ fF}$$

If the LSB array is extended with the capacitors for the gain correction, then this equation is not valid anymore. If for example the biggest capacitor in the LSB array is switching from ground to the reference, then the charge in the CDAC of Fig. 2.13 is distributed between the other LSB capacitors and the scale-down capacitor. For the CDAC with extended capacitors such as in Fig. 2.18, the charge in the CDAC will also be distributed to the capacitors for the gain adjustment, which will divide the signal and will cause a gain error of the LSB array. The weight of all LSB capacitors together will be lower than the $C_{MSB\text{-}4}$ capacitor, which will generate DNL errors. This can easily be compensated by further increasing the scale-down capacitor.

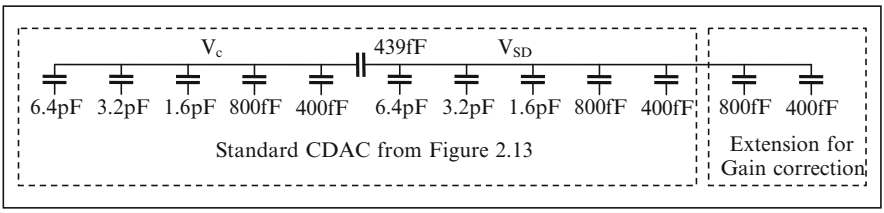

Fig. 2.18 Capacitor array of a 10 bit CDAC with additional capacitors for gain correction

For the correct calculation of the scale-down capacitor, the delta of the scale-down voltage V_{SD} is calculated by taking into consideration that the total charge will not change as it is frozen at the scale-down node. Initially, V_{SD} should be discharged (0 V) and all capacitors in the MSB and the LSB array are coupled to ground. The initial charge Q_1 is therefore zero. Now the biggest capacitor in the LSB array (now called C_{LSBh}) is switched from ground to the reference voltage, which will lead to the following equation

$$Q_2 = C_{LSBh}(V_{SD} - REF) + C_{rest} \cdot V_{SD} = 0 \Leftrightarrow V_{SD} = REF\frac{C_{LSBh}}{C_{LSBh} + C_{rest}}$$

C_{rest} includes the other LSB capacitors, which are equal to C_{LSBh} minus the LSB capacitor C_{LSB}, and it includes the capacitors for the gain adjustment C_{gain}, any parasitic capacitors C_{par} and the series capacitance $C_{SD,MSB}$ of the scale-down capacitor and the capacitance of the MSB array. If the scale-down voltage V_{SD} is applied to the scale-down capacitor C_{SD}, then the change in charge should be half compared to applying the reference voltage to the smallest capacitor in the MSB array C_{MSBl} (here $C_{MSB\text{-}4}$) so that

$$\frac{1}{2}C_{MSBl} \cdot REF = C_{SD} \cdot V_{SD} = C_{SD} \cdot REF \cdot \frac{C_{LSBh}}{2C_{LSBh} - C_{LSB} + C_{par} + C_{gain} + C_{SD,MSB}}$$

If V_{SD} is substituted and if $C_{SD,MSB}$ is estimated to C_{SD} as $C_{MSB} >> C_{SD}$, then

$$C_{SD} = \frac{C_{MSBl} \cdot 2C_{LSBh}}{2C_{LSBh} - C_{MSBl}} \cdot \left(1 + \frac{C_{par}}{2C_{LSBh}} + \frac{C_{gain}}{2C_{LSBh}} - \frac{C_{LSB}}{2C_{LSBh}}\right) \tag{2.9}$$

In the example of Fig. 2.18, parasitic capacitors are not included ($C_{par} = 0$), the gain capacitors are 1.2 pF, the LSB capacitor is 0.4 pF, C_{LSBh} is 6.4 pF and C_{MSBl} is 0.4 pF again, so that the scale-down capacitor can be calculated to 439 fF.

An additional method for a gain adjustment through the reference is also presented in Fig. 2.60 of Sect. 2.5.3. The method with the CDAC capacitors has the advantage that they are based on capacitive matching, so that they work especially accurate and with very low drift.

2.2.2.3 Offset Trim

If an offset voltage V_{off} is added to a signal V_{sig}, then the input voltage V_{in} of the ADC can be expressed by

$$V_{\text{in}} = V_{sig} + V_{off}$$

If the same offset is also added to the normal voltage of the CDAC V_{DAC}, then the CDAC output V_{CDAC} can be expressed to

$$V_{CDAC} = V_{DAC} + V_{off}$$

and the comparator is comparing

$$V_{\text{in}} > V_{CDAC} \Leftrightarrow V_{sig} > V_{DAC}$$

Equation (2.5) shows, how the offset can be compensated through the CDAC. The offset error V_{off} of the bipolar ADC is measured at mid-scale ($x_{1n} = 1$ and $x_{jn} = 0$ for $j\varepsilon\{2, \ldots, N\}$), if $V_{inp} = V_{off} + REF$ and $V_{inn} = REF$. If all capacitors are ideal, then Eq. (2.5) leads to

$$V_{off} = \frac{REF}{C_s} \cdot \left(C_1 - \sum_{j=1}^{N} \left(x_{jp} \cdot C_j \right) \right) \tag{2.10}$$

Equation (2.10) assumes that $C_{sp} = C_{sn} = C_s$ and $C_{jp} = C_{jn} = C_j$ ($j\varepsilon\{1, \ldots, N\}$).

The generated offset is 0, if C_{1p} is connected to REF after sampling and all other capacitors C_{jp} to ground. A positive offset can be generated, if C_{1p} remains at ground. Other capacitors C_{jp} can connect to REF to adjust the offset. Finally, a negative offset is set, if capacitors C_{jp} beside C_{1p} are switched to the reference after sampling [11, 12].

It is also possible to extend the CDAC from Fig. 2.13 with capacitors for offset compensation. In Fig. 2.19, two capacitors are added inside the scale-down array.

Adding capacitors for the offset correction might be required, if the CDAC scheme uses the capacitors C_{jp} for a fully differential conversion process.

Switching the 400 fF capacitor of the offset correction from ground to the reference will have the same effect like switching the 400 fF LSB capacitor to the reference voltage. In this way, an offset of one LSB can be added to V_c.

During the sampling phase, where V_c is connected to a common-mode voltage, the second electrode of the offset capacitors is connected to ground. The selected offset capacitors are switched to the reference as soon as V_c is disconnected from its common-mode source. The selected offset capacitors remain at the reference voltage as long as the conversion is in process and switch back to ground with the start of the next sampling phase.

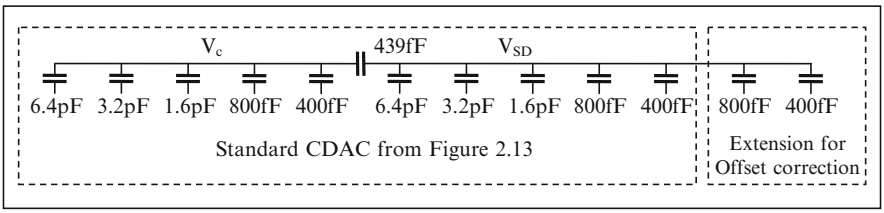

Fig. 2.19 Capacitor array of a 10 bit CDAC with additional capacitors for offset correction

The structure of Fig. 2.19 can also realize negative offset voltages. The only difference is that the capacitors are pre-charged to the reference voltage during the sampling phase and are then connected to ground during the conversion phase.

If capacitors for offset adjustment are added inside the scale-down array, then the scale-down capacitor needs to be adjusted identically to the gain correction. The gain and offset adjustment can both be implemented into one CDAC.

2.2.2.4 CMRR Trim

The common-mode rejection ratio (CMRR) inside the SAR ADC can be considered as the change of the CDAC output voltage $dV_c = dV_{cp} - dV_{cn}$ versus the change of the external common-mode voltage dV_{in}. The differential input voltage during common-mode measurement is zero ($V_{inp} = V_{inn} = V_{in}$). Adding these to Eq. (2.5) leads to

$$CMRR = \frac{dV_c}{dV_{in}} = \frac{C_{sn}}{C_{sn} + \sum_{j=1}^{N} C_{jn}} - \frac{C_{sp}}{C_{sp} + \sum_{j=1}^{N} C_{jp}} = \frac{C_{sn}}{C_{totn}} - \frac{C_{sp}}{C_{totp}} \tag{2.11}$$

To achieve an ideal common-mode rejection ratio $CMRR = 0$, the ratio of the sampling capacitor C_{sp} to the total capacitance C_{totp} on the positive side has to be identical to the same ratio on the negative side. The CMRR can therefore either be trimmed by modifying the sampling capacitance C_s on only one side of the CDAC or by continuously adding or removing capacitance from V_c to ground on only one side of the CDAC.

2.2.2.5 Trim Capacitor Array

Trim schemes regarding Eqs. (2.7) and (2.8a, 2.8b, 2.8c) as well as Eqs. (2.10) and (2.11) require capacitors, which correspond to a fraction of an LSB. These capacitors are generally difficult to generate. Their size can be increased, if they are placed inside the LSB-array as discussed above. However, adding all trim

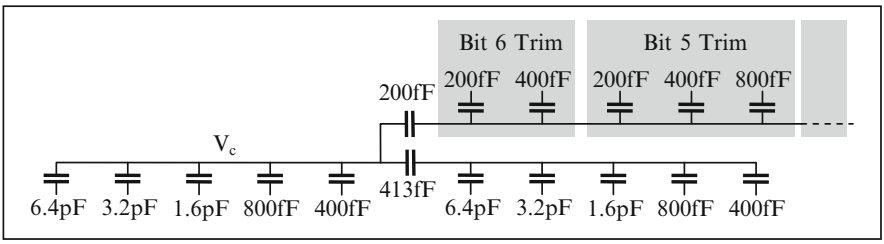

Fig. 2.20 Capacitor array of a 10 bit CDAC with additional trim capacitor array

capacitors to the LSB-array will add too many parasitic capacitors, so that a high variation in the LSB weight might be visible, which would require additional DNL trim range.

An alternative was found by adding a trim capacitor array, which is connected to the MSB array with a trim-scale-down capacitor as shown in Fig. 2.20. The trim capacitors can be realized with a reasonable size, so that they are matching well to the other capacitors. This reduces trim time and production costs. The realization of such a trim solution is shown in the next chapter, where a 16 bit CDAC implementation is discussed.

2.2.3 Implementation of a Pseudo Differential 16 bit CDAC

The CDAC of this example should be based on the CDAC in Fig. 2.13 including a scale-down capacitor. The CDAC is implemented as pseudo differential architecture, which requires a negative side.

Figure 2.21 shows the implementation. C_1 represents the MSB, C_2 the MSB-1 and so on. The MSB capacitors require trimming, which is illustrated with the capacitors C_T. The capacitance is illustrated with a number. The smallest capacitor (C_6) in the MSB array is realized with one unity capacitor. For good matching, the larger capacitors are realized with multiple unity capacitors. C_5 for example is realized with two unity capacitors instead of one capacitor with twice the area of C_6. Reason is that the etching process in production varies slightly from lot to lot depending on the exact temperature or acid concentration. Consequently, the fringe varies from wafer lot to wafer lot causing a change in capacitance, which is dependent on the fringe. Two capacitors that differ in the outline will therefore match worse than two capacitors with the same outline.

The layout of the CDAC and particularly the unity capacitor as illustrated in Fig. 2.22 needs to be performed very carefully:

1. The top plate is mostly responsible for the matching. The corners should have 45° angles, as the edging process will always round off corners. On the other side, a significant amount of capacitor mismatch is generated by the fringe. The

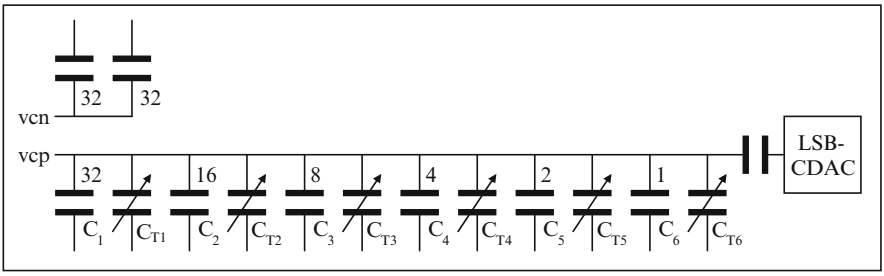

Fig. 2.21 Capacitor array of a pseudo-differential CDAC implementation

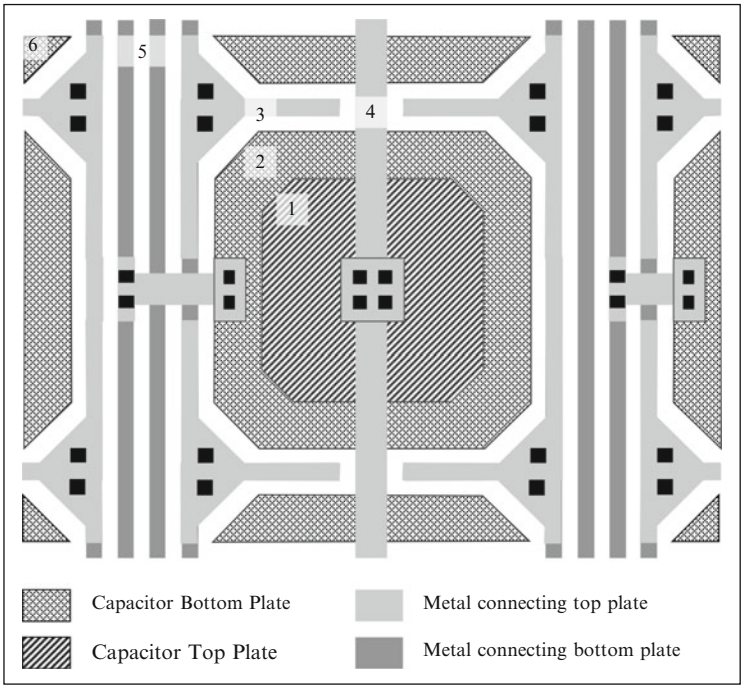

Fig. 2.22 Layout suggestion for a unity capacitor used inside a CDAC

outline to area ratio should therefore be small. Consequently, the chamfer should remain short. Octal structures should be avoided.

2. The bottom plate might have a significant parasitic capacitance to the substrate (up to 10 %), which reduces the settling speed of the capacitors. The corners of the bottom plate might also have 45° corners. The bottom plate typically overlaps the top plate, so that the mismatch caused by the fringe is limited to the top plate. Due to the parasitic capacitance to the substrate, the bottom plate is not used for the high impedance connection V_{cp} and V_{cn} from the CDAC to the

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Analog-Digital Converters for Industrial Applications
Including an Introduction to Digital-Analog Converters

Ohnhäuser, F.

2015, IX, 333 p. 309 illus., Hardcover
ISBN: 978-3-662-47019-0