# Preface

This work titled *A Digital Phase Locked Loop based Signal and Symbol Recovery System for Wireless Channel* is intended to serve as a document covering fundamental concepts and application details related to the design of digital phase locked loop (DPLL) and its importance in wireless communication. It documents some of the work done during the last few years covering rudimentary design issues, complex implementations, and fixing configuration for a range of wireless propagation conditions. The work reported here is a result of extensive analysis and practical design carried out while designing DPLL-based systems which are considered to be part of systems intended to perform data, carrier, and symbol recovery in stochastic wireless channels. There are a total of 13 chapters covering basic concepts and application details of the DPLL system described in the book. The first chapter is introductory in nature. It talks about the background of the work, highlights the historical perspective, application of phase locked loops (PLL), and the importance of PLL in communication system. It also provides a brief note about the shift from PLL to DPLL.

In Chap. 2, the focus is on transmitter receiver techniques so important for communication. It highlights the issues related to base band and pass band signals. Some of the issues though are rudimentary and are available in the common literature, which are included to provide certain background reading about the issues discussed later in the remaining chapters.

Chapter 3 focuses on modulation techniques and signal processing. It covers modulation types and issues, discusses certain modulation techniques with focus on quadrature amplitude modulation (QAM), pulse shaping, line coding, wireless channel and fading, and issues related to representation of Nakagami modeling.

Chapter 4 is introductory in nature and discusses mainly about the issues of PLL, types, and working. It also includes a nonlinear description of PLL and the importance of a complex-domain analysis.

The key issues, basic concepts, and essential building blocks related to DPLL are included in Chap. 5. It highlights the importance of DPLL, provides a discrete time model of DPLL, describes the components of the DPLL, types of DPLL, and their

importance. The chapter is expected to help the reader to develop certain insights into the design of DPLL-based systems.

Synchronization is a key issue in communication systems. Certain basic ideas related to synchronization, working, and types constitute Chap. 6. Synchronization in terms of coherent and non-coherent reception, carrier synchronization, timing or symbol synchronization, frame synchronization, and the essential details are included in this chapter.

Chapters 7–12 are descriptions derived from the actual work. Chapter 7 highlights a zero crossing algorithm-based digital phase locked loop. The work is the implementation of the essential components of a DPLL for better reception of signals with certain modulation transmitted through Nakagami-m channels. A sixth order polynomial fitting algorithm for better phase-frequency detection is implemented, which has helped to attain optimum performance of DPLL. The results of simulation of the proposed DPLL with Nakagami-m fading and QPSK modulation show that the proposed method provides better performance than existing systems of similar type.

Chapter 8 describes a modified structure of a Least Square Polynomial Fitting Filter-based DPLL-based system for dealing with Nakagami-m fading. The emphasis of the work is the implementation of the essential components of a DPLL for better reception of signals with certain modulation transmitted through Nakagami-m channels. A sixth order Least Square Polynomial Fitting (LSPF) block and Roots Approximator (RA) for better phase-frequency detection has been implemented as a replacement for Phase Frequency Detector (PFD) and Loop Filter (LF) of a traditional DPLL, which has helped to attain optimum performance of DPLL. The results of simulation of the proposed DPLL with Nakagami-m fading and QPSK modulation show that the proposed method provides better performance than existing systems of similar type.

A modified structure of a DPLL-based system for dealing with Nakagami-m fading is proposed in Chap. 9. The emphasis of the work is to generate input signal under various fading conditions with certain modulation transmitted through Nakagami-m channels and to evaluate the performance of the proposed DPLL in terms of Bit Error Rate (BER). Statistical characteristics of the faded input signal have been evaluated in terms of Probability Distribution Function (PDF), Level Crossing Rate (LCR), and Average Fade Duration (AFD). A sixth order Least Square Polynomial Fitting (LSPF) block and Roots Approximator (RA) for better phase-frequency detection is implemented as a replacement for Phase Frequency Detector (PFD) and Loop Filter (LF) of a traditional DPLL, which has helped to attain optimum performance of DPLL.

Carrier and symbol recovery in severely faded Nakagami-m channel is a challenging area. It requires design of certain systems that can capture the carrier and symbols during the reception process. There are several known approaches but very few report the use of Phase Locked Loop (PLL)-based methods. In Chap. 10, we propose a Digital Phase Locked Loop (DPLL)-based system for carrier and symbol recovery in severely faded Nakagami-m channel. We report the performance of the proposed system in terms of Symbol Error Probability (SEP) while recovering

carrier and symbols from QPSK-modulated signals in the presence of phase error. SEP performance of the DPLL is compared for cases of un-coded and BCH (15, 7) coded conditions.

In Chap. 11, the design of a digital receiver for carrier phase tracking is presented. The receiver architecture includes a Least Square Polynomial Fitting (LSPF)-based DPLL. BER performance of the proposed system for dealing with Rayleigh and Rician fading for different numbers of paths with coded and un-coded channel is presented here. The performance of the DPLL for carrier phase tracking with signal using QPSK modulation transmitted through Rayleigh and Rician fading channels are compared with coded and un-coded conditions. Simulation results show that the proposed DPLL-based approach shows significant improvement using BCH coding both in Rayleigh and Rician fading channels. Several essential processes like noise and co-channel interference (CCI) cancellation, equalization, etc., that are integral to the traditional frameworks are made redundant by the proposed DPLL-based approach. The composite outcome of these separate processes is combined by the DPLL action making it a reliable and efficient mechanism.

In Chap. 12, the structure of a squaring loop-based DPLL for carrier detection over multipath Nakagami channel is presented. The emphasis of the work is the implementation of the essential components of a squaring loop for better carrier synchronization to the received signal with certain modulation transmitted through Nakagami channels. A Zero Crossing algorithm-based phase-frequency detection technique is implemented, which has helped to attain optimum performance of the loop. The results of simulation of the proposed DPLL with Nakagami fading and BPSK modulation show that the proposed method provides efficient carrier synchronization despite signal being corrupted under severely faded condition.

Chapter 13 summarizes the description and discusses the certain future direction.

The contents of the chapters are expected to help readers and researchers with certain design issues derived out of theoretical analysis and experimental work. The authors are thankful to everyone associated with the work in related areas at Gauhati University and Indian Institute of Technology Guwahati (IITG), two of the leading institutions of higher learning in north-eastern India. Special thanks go to the Department of Electronics and Communication Technology, Gauhati University, Department of Electronics and Electrical Engineering, IITG, Department of Physics, IITG and Ministry of Information and Communication Technology, Government of India for their respective contributions while executing different stages of the work. The authors are thankful to the family members for their constant support and encouragement. Heartfelt thanks goes to the team members related to review, design, editing, and publication associated with Springer. Their roles have been vital in making the compilation reach this end.

Guwahati, June 2014

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http://www.springer.com/978-81-322-2040-4

A Digital Phase Locked Loop based Signal and Symbol Recovery System for Wireless Channel

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2015, XXI, 244 p. 118 illus., Hardcover
ISBN: 978-81-322-2040-4