

# Preface

Modern very-large-scale integration (VLSI) chips contain millions of transistors. It is envisaged that VLSI chips will contain more than three billion transistors in the coming decade. VLSI chips find wide applications in all modern electronic circuits and systems. In highly-scaled VLSI technology nodes, more and more functionalities are being housed on a chip. Various functional blocks of the chip are connected to each other with interconnects. Interconnects distribute clock, supply voltage, and signals in a VLSI chip. Chip sizes are also decreasing due to technological advances. High chip complexity requires dense interconnections to communicate information between devices and circuit blocks. As a result, long interconnects have become common on-chip features. However, long interconnects cause various deleterious effects, viz., high propagation delay, degradation of signal waveforms, excess power dissipation, and crosstalk. Consequently, the increased number of interconnects in present-day VLSI chips has made the interconnection design problem complex and challenging.

In recent years, power dissipation is given comparable weightage to the area and speed considerations. The primary driving factor is increasing prominence and fast growth of battery operated applications such as micro-sensor networks, pacemakers, hearing aids, and many other portable devices, which require stringent energy constraints for longer battery lifetime. Subthreshold operation of devices presents an opportunity for energy-constrained applications with its ultra-low-power consumption. Subsequently, the benefits from ultra-low-power operation have carved out a significant niche for subthreshold circuits. Though the subthreshold operation shows huge potential toward satisfying the ultra-low-power requirements of portable systems, it holds design issues both for interconnects and circuit design. These issues lead to significant increase in the design complexity of integrated circuits. There are not many works that address these challenges for subthreshold circuit design in an integrated and comprehensive manner. This book provides a detailed analysis of concerns related to subthreshold interconnect performance from the perspective of analytical approach and design techniques. It also presents a qualitative summary of the work reported in the literature by various researchers in the design of digital subthreshold circuits. Particular emphasis is laid on the

performance analysis of coupling noise and variability issues in subthreshold domain to develop efficient compact models. The different tasks accomplished in this book are mentioned below.

A new parameter called subthreshold drain conductance is defined. Two new sub-regions of MOS operation are identified. Compact analytical expressions governing output voltage, propagation delays, and coupling noise are developed. The impact of coupling on aggressor delay is analyzed. The proposed analytical approach gives physical insight into the parameters affecting the transient behavior. This is essential for avoidance of dynamic crosstalk and circuit malfunctioning. Remedial design techniques are suggested to mitigate the effect of coupling noise caused by the interconnect coupling capacitance. The effects of wire width, spacing between the wires and wire length are thoroughly investigated. In addition, the effect of parameters like driver strength on peak coupling noise has also been analyzed. Process, voltage, and temperature variations are prominent factors affecting subthreshold design and have also been investigated. Analytical expressions characterizing variability based on the parametric analysis are developed. The process variability analysis has been carried out using parametric analysis, process corner analysis, and Monte Carlo technique. The impact of temperature on subthreshold interconnect performance is also investigated.

To summarize, this book will serve as a platform for researchers and graduate students with deeper insights into subthreshold interconnect models in particular and designing complex logic gates in general. This book will best fit as a textbook and/or a reference book for students who are initiated in the area of research and advanced courses in nanotechnology, ultra-low-power interconnect design, and modeling.

Rohit Dhiman  
Rajeevan Chandel

Compact Models and Performance Investigations for  
Subthreshold Interconnects

Dhiman, R.; Chandel, R.

2015, XIII, 113 p. 45 illus., Hardcover

ISBN: 978-81-322-2131-9