

Chapter 2

Multilevel Converter Topologies for STATCOMs

Anshuman Shukla and Alireza Nami

Abstract To implement the STATCOMs for transmission and distribution applications, high power converters are needed. A multilevel converter is a logical choice for such applications as it can meet the imposed line side current and voltage harmonic distortion standards without extending its device ratings. Several types of monolithic multilevel converters have been proposed based on different structures of a DC link voltage (or current) to generate staircase output voltage (or current) levels. The multilevel current source converters (CSC) are also a potential configuration for STATCOM. Multilevel CSCs using fully controllable switches have the advantages of low output harmonics and controllable active and reactive power. During the last decade, modular multilevel converters have shown a breakthrough and have made their way to commercial high power applications. Modularity, in general, refers to a technique to develop comparably large systems by combining smaller subsystems. For power converter topologies, this means, a cascaded connection of converter cells seems to be an interesting solution to reach high voltage and high quality waveforms with a minimum complexity. This chapter provides an overview on monolithic and modular multilevel converter topologies, targeting high-power applications and in particular STATCOM. Modular multilevel converters can be built either straightforward by applying the modular building block cells or by a combination of cells with monolithic multilevel topologies. The monolithic and modular CSCs can also be realized by employing the duality concept on each corresponding Voltage Source Converter (VSC). This chapter summarizes the most recent developments made for multilevel converter

A. Shukla (✉)

Department of Electrical Engineering, Indian Institute of Technology Bombay,
Mumbai, India
e-mail: ashukla@ee.iitb.ac.in

A. Nami

RDPTEPS, ABB AB, Corporate Research, Västerås, Sweden
e-mail: alireza.nami@se.abb.com

topologies, by covering new promising topologies and operational issues. In addition, emerging trends, challenges, and possible future directions of the multi-level converter technologies are outlined.

Keywords VSC • CSC • STATCOM • Multilevel • Submodule • Modular

2.1 Introduction

The most important component in a STATCOM is a power electronic based static converter. The main objective of this converter is to produce an AC output waveform from a DC power supply. According to the type of DC source used, i.e., voltage or current, there are two types of converter topologies prevailing: VSC and CSC, as illustrated in Fig. 2.1. These converters are constructed using power switches, like IGBTs. In a VSC, each basic switching element is composed of a fully controllable, unidirectional semiconductor switch with a diode connected in antiparallel to it. In a CSC, each switching element is required to block bipolar voltage when open and to conduct at least unidirectional current when closed. A bidirectional current conducting switch may also be used for enhanced flexibility and functional improvements. A reverse blocking device can be composed by a fully controllable switch in series with a diode. The fully controllable semiconductor switch considered in this chapter is the IGBT as it suits the high frequency switching operation for both low and medium voltage distribution system compensation as well as can meet the high voltage and power requirements for transmission system compensation [1–11].

There are various converter configurations available for both single and three-phase applications. The most fundamental of all these are single-phase half bridge and full bridge (H-bridge) VSC and CSC as shown in Fig. 2.2. The single-phase half-bridge is a one-leg converter consisting of two switching elements. This topology can be used to obtain a two-level output of the VSC. The single-phase H-bridge is a two-leg converter with each leg consisting of two switching elements. The H-bridge VSC is more popular for single-phase applications because with same DC input voltage the output of the full bridge is twice that of the half bridge. This topology of VSC can also be used to obtain a two-level output. Additionally a zero

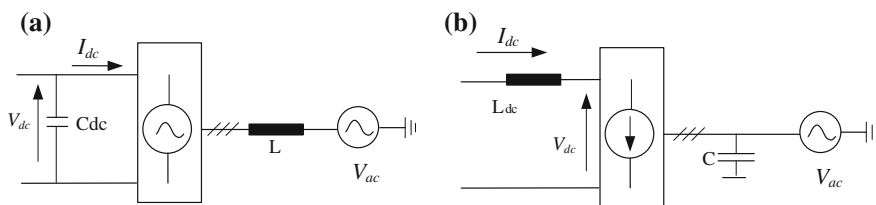


Fig. 2.1 Grid connected converters: **a** VSC **b** CSC

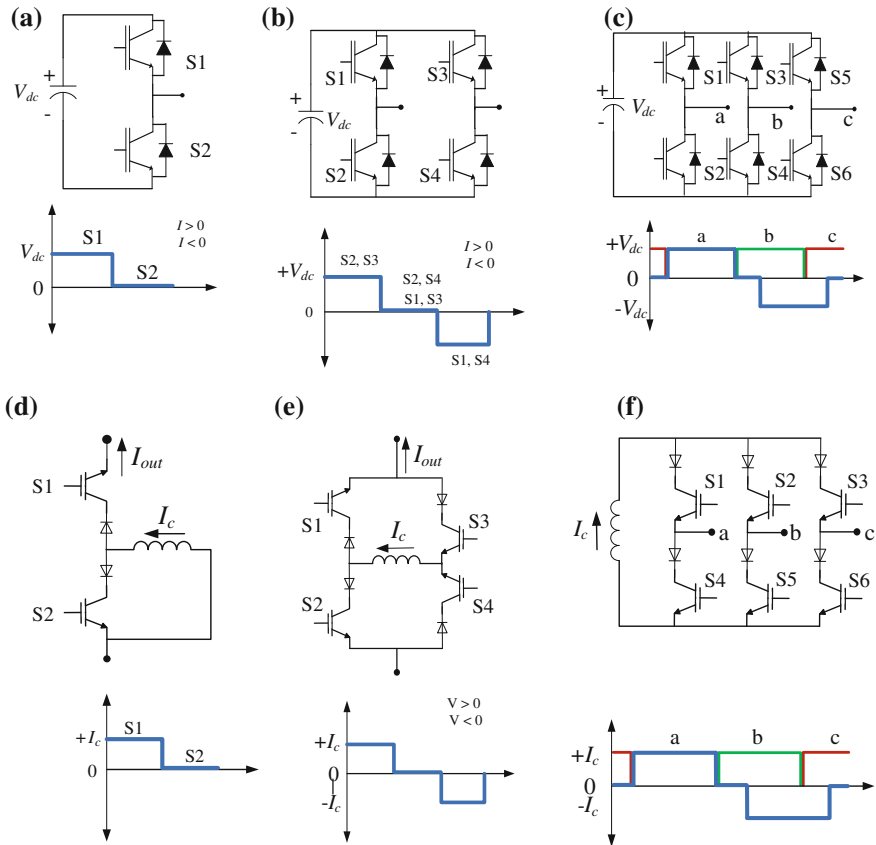


Fig. 2.2 **a** Half bridge VSC, **b** full bridge or H-ridge VSC, **c** three-phase two-level VSC, **d** half-bridge CSC, **e** full bridge CSC and, **f** three-phase two-level CSC

voltage can be placed with the full bridge to obtain a three-level output. The H-bridge topology with the aid of suitable transformers is used for both low voltage and medium voltage distribution system compensation [12]. Finally a three-phase two-level converter can be synthesized by parallel connection of the half-bridge phase legs across the DC-link. CSC topologies may be generated from the respective VSC topologies by employing the duality principles. The half-bridge CSC is shown in Fig. 2.2c which is exactly the dual of the half-bridge VSC converter. Therefore, dual to the voltage source full- and three-phase bridges, is realized by connecting the inductor cells in parallel as shown in Fig. 2.2e, f.

The STATCOM can be used in different power levels depending on the applications. There are mainly three-main areas for the STATCOM application on the basis of different power levels as shown in Fig. 2.3. To implement the STATCOMs at medium and high power level, high power converter is needed that in most cases exceeds the power handling capability of a simple two level converter without

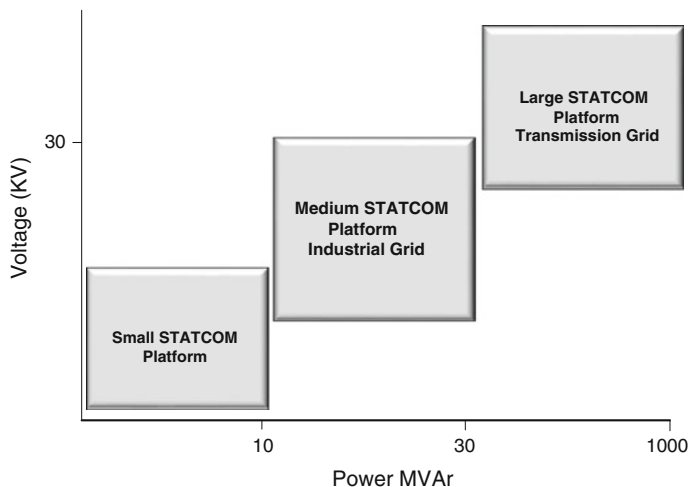


Fig. 2.3 Power level of STATCOMs

device series/parallel connection. Conventionally, for such high power applications and for boosting up the DC bus voltage beyond the voltage rating of an individual switch, the two level converter has to use series connected devices. Similarly, In this case, the series connected low rating devices act as a single switch like one of the switches shown in Fig. 2.1. However, due to the different scattering times of semiconductor devices, the following issues must be well considered in order to avoid voltage-sharing problems among the switches. The electrical and thermal characteristics of the semiconductor devices in the same switch need to be matched. The synchronization of the switching is very difficult and may result in voltage unbalance between the devices. Additional care is needed for the turning-off process of the switch, as well as for its gate currents. As a result of these restrictions, power dissipation during conduction and switching is such that the switching frequency is severely limited. This causes a slow system response and bulky output filter circuits. Large snubber circuit parameters are also required to compensate transient voltage unbalance and to achieve static voltage balancing. It may also lead to more switching losses and relatively longer switching time. Although the blocking voltage of the switch in the two-level converter is increased, a step-up transformer is still needed for coupling to the transmission networks. Moreover, extra efforts are needed to match the harmonic standards at the two-level converter outputs.

Another possible way of achieving such high power requirement is to use magnetic transformer coupled multi-pulse converters [5]. Traditional magnetic coupled multi-pulse converters typically synthesize the staircase voltage wave by varying transformer turns ratio with complicated zigzag connections. For example, a typical 48-pulse converter consists of eight 6-pulse converters connected together through eight zigzag-arrangement transformers using the harmonic cancellation

technique, or connected through Wye/Delta and Delta/Delta connection transformers and using sophisticated control schemes, in order to reduce harmonic distortion and to reach high voltage. The patent of Unified Power Flow Controller (UPFC) [13] shows that the shunt-side and the series-side of the UPFC are based on eight, 2-level, three-phase bridge VSCs. A high power converter arrangement is then achieved by synthesizing the voltage waveform using complicated zigzag transformer connections to ensure that the Total Harmonic Distortion (THD) standards are finally met. In 1995, the first ± 100 MVA STATCOM was installed at the Sullivan substation of Tennessee Valley Authority (TVA) in northeastern Tennessee [14]. This unit is mainly used to regulate 161 kV bus during the daily load cycle to reduce the operation of the tap changer of a 1.2 GVA-161 kV/500 kV transformer. Its 48-pulse power converter consists of eight two-level VSCs with complex-interface magnetic circuits. Because this is a two-level VSC, a series connection of five of gate-turn-off (GTO) thyristors is used as a main switch. The control scheme used in this STATCOM is a 60 Hz staircase. Due to the slow switching speed of the GTOs, the firing angles of the output waveform are fixed; therefore, the amplitude of each output waveform is controlled by exchanging active power of the DC-link capacitor with the power grid. Since it began operating, several weak points of the TVA-STATCOM system have been pointed out [15]. Some of these weak points were due to the use of series connected switching devices as discussed above. Taking feedback from the experiences of this installation, in the AEP UPFC installation, Inez area, eastern Kentucky, USA, the VSCs were designed to make use of three-level configuration instead of a two level used earlier in the TVA STATCOM project [15]. However, this structure still used the multi-pulse arrangement. The limitations with this multi-pulse arrangement with magnetic transformer coupling method are [16]: (i) they are very expensive, (ii) produce about 50 % of the total losses of the system, (iii) occupy up to 40 % of the total system's real estate, (iv) cause difficulties in control due to DC magnetizing and surge overvoltage problems resulting from saturation of the transformers in transient states and (v) are prone to failure. Therefore, the capacitor voltage synthesis method is preferred to magnetic coupling method for achieving higher rating converters. An attractive alternative to the above discussed topologies and most recent development in the field of high power converters is the multilevel converter.

For the STATCOM applications in utility and distribution systems, the conventional two-level converters are most commonly used in low to medium voltage levels. For medium and high-voltage networks, the conventional STATCOM structures are designed on the basis of simple two-level converter and use transformer to meet the desired voltage profile. In some cases, in order to achieve higher power level, converters are connected in parallel to the DC bus. This type of connection requires a transformer with multiple secondary windings, increasing the cost and complexity of the power topology. Further, the transformer adds to the losses in the system and it may saturate once the load draws any DC current. For the STATCOM applications in utility and distribution systems, it is preferable to perform faster switching actions to have fast dynamic response, improved robustness and a continuously spread harmonic spectrum. However, at higher power, the long tail current associated with the

device (IGBT) characteristics prohibits higher switching frequency operation at a high power and the efficiency of the compensator is lower due to significant switching losses [17]. Therefore, the compensator control in high power applications faces difficulties. Further, such higher frequency operation using the two-level converter based compensator is not always possible because of the switching frequency limitation imposed on presently available higher rated devices. Again, the series connection of devices and/or multistep converter configuration is not recommended due to their respective limitations stated above.

For medium to high power applications and to meet the line side imposed current and voltage harmonic distortion standards, the multilevel converter is a logical selection without extending its device ratings. As discussed above, the series connection of the devices faces voltage unbalance problem. In case of a VSC, the best method of stabilizing voltages applied to the devices is by clamping those using DC voltage sources or large capacitors, which transitorily behave as voltage sources. Multilevel VSC topologies are based on this principle and therefore, the voltage applied to the device can be controlled and limited. The multilevel CSC topologies are based on the principle of current clamping using inductors. All the available multilevel CSC topologies have been derived from their corresponding equivalent multilevel VSC topologies using the duality principle [9]. In the following, the discussion presented focuses mostly on the multilevel VSC topologies. However, these can be interpreted similarly for the CSC topologies using the duality principle.

Without semiconductor devices connected in series, the multilevel VSCs show feasible capability of clamping the voltages across individual devices below their limitations. This allows the recent semiconductor devices to be utilized in higher-voltage applications without incurring voltage-sharing problems. In a multilevel converter, the number of possible operating states increases and as a consequence, the flexibility of the converter improves. Another significant advantage of the multilevel configuration is the harmonic reduction in the output waveform with very low switching frequency. Hence the output voltages can be filtered with smaller reactive components. They also provide lower electromagnetic interference and lower acoustic noise. Besides the high-voltage capability, multilevel converters also provide other advantages over the two-level converters. As all the devices are individually controlled, better control over voltage magnitude and harmonic suppression can be achieved. Use of a multilevel converter reduces the required transformer voltage ratio and sometimes even makes possible direct connection of the compensator to the increased voltage supply systems without needing interconnecting transformer. The multilevel converter topologies are attractive for continuous control of system dynamic behavior and to reduce power quality problems such as voltage harmonics, voltage imbalance or sag and have better properties under sudden changes of loads. Besides, a multilevel compensator, in comparison with its two level counterparts, makes more exact formation of the compensating currents possible. Hence, these are suitable for STATCOM applications in both transmission and distribution systems [18–21].

There is a wealth of literature available on the characteristics and controls of the multilevel converters. For the past two decades, multilevel VSC technology has

been a rapidly developing area in power electronics and has been proposed as the best choice in several medium and high voltage applications. It promises power-conversion equipment for applications that operate in the medium-voltage (4.6–13.8 kV) grid without requiring step-up transformers [22]. With the step-up transformer, the multilevel converter may also be operated at higher voltage levels, such as transmission levels. Multilevel VSC technology has recently been utilized in various types of industrial applications, such as AC power supplies, reactive power compensations, adjustable speed drive systems, etc. [3, 4]. Besides, it has also found applications in enabling the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel converter system for a high power application [23]. Another application for multilevel converters is to interconnect different power grids [24]. In the following sub-section, the concepts, features, advantages, limitations and classification of multilevel VSCs have been presented.

2.1.1 Multilevel Converters: Basic Concepts and Features

The concept of multilevel converters was first introduced in 1975 [25]. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed [1–4]. The elementary concept of a multilevel VSC to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources. The DC voltage sources can be realized by capacitors, batteries, and renewable energy voltage sources. These multiple DC sources are aggregated using the power semiconductor switches in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches is kept at only a fraction of the total DC voltage. The AC voltage produced from these DC voltages approaches a sinusoid with increasing the number of levels. The multilevel VSC can work in both rectifier and converter modes as it uses the bi-directional switches.

Fundamentally, as discussed earlier, the output voltage waveform of a multilevel VSC is synthesized from different levels of voltages obtained from DC voltage sources. Figure 2.4 shows an equivalent circuit of a half bridge of a multilevel VSC. A bi-directional, single-pole, multi-throw switch is a key element of the multilevel topology. By controlling the way in which the switch is connected to a portion of the capacitors, a number of output voltage levels can be synthesized. To generate a negative output voltage, the reference of the output can be connected to different segments of the capacitor string. Two or more half bridge of the converter shown in Fig. 2.2 can be utilized to form a multiphase, multilevel converter.

Figure 2.5 illustrates an example of a multilevel converter output voltage waveform. In this figure, an eleven level Pulse Width Modulation (PWM) waveform is shown with a peak-to-peak voltage of 1.0 kV. In this case, the multilevel converter produces a fair approximation to a sinusoidal waveform.

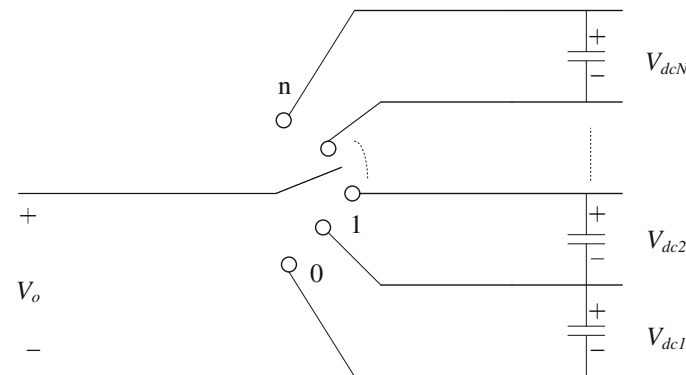


Fig. 2.4 Equivalent circuit of multilevel voltage-source converters

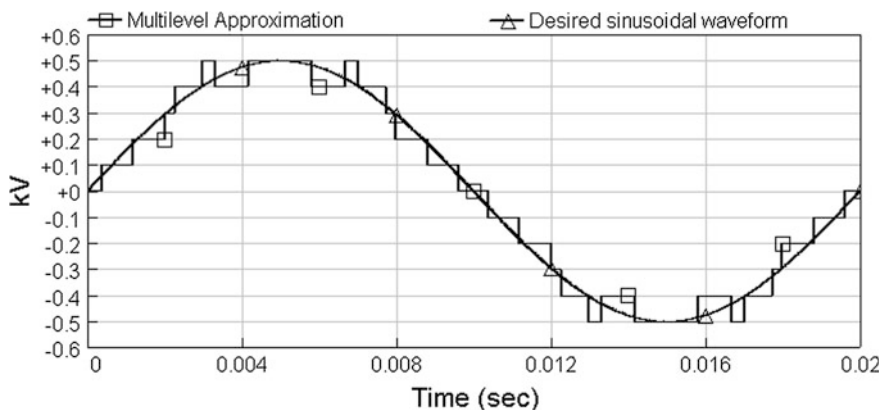


Fig. 2.5 Example multilevel sinusoidal approximation using eleven-levels (V_0)

As one can see in Fig. 2.4, the multilevel converter output stepped waveform contains sharp transitions. This phenomenon results in harmonics, in addition to the fundamental frequency of the sinusoidal waveform. The key issue for a converter modulation is the harmonics elimination. The increased number of levels provides the opportunity to eliminate more harmonic contents. Eliminating some harmonic contents will make it easier to filter the remaining harmonic content. As a result, filters will be smaller and less expensive. There are many schemes available in the literature for reducing the harmonic contents. In Fig. 2.4, the multilevel waveform has been obtained using a multicarrier PWM modulation technique. This scheme simply refers to switching on or off the converter switching devices based on intersection of the modulation signal (mostly, a sinusoidal waveform) with a number of carrier signals (mostly, of triangular shape) in a certain fashion. The number of carrier signals depends on the number of phase output voltage levels of the converter.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency PWM. Some important attractive features of a multilevel converter can be briefly summarized as follows [1–4].

- *Multilevel waveform quality*: The electromagnetic compatibility (EMC) problems can be reduced as the multilevel converters generate the output voltages with lower distortion and reduced dv/dt stresses.
- *Common mode (CM) voltage*: Multilevel converters produce smaller CM voltage and it can be eliminated using some advanced modulation techniques; therefore, the premature failure of the motor bearings and the EMI issues can be avoided.
- *Input current*: The input current drawn by the multilevel converters is of lower distortion.
- *Voltage transients*: Multilevel waveforms naturally limit the problems of large voltage transients.
- *Switching frequency*: The switching frequency of the power semiconductor switches in a multilevel converter can be much lower than that in a two-level converter for the same harmonic spectrum of the converter outputs. A lower switching frequency implies lower switching loss and higher efficiency.
- *Switch ratings*: Since multilevel converters usually utilize a large number of DC voltages, several switches are required to block smaller voltages. Since switch stresses are reduced, required switch ratings are lowered.
- *System reliability*: If a component fails in a multilevel converter, most of the time it can still be used at a reduced power level. Furthermore, a desired voltage can be produced by more than one way as the multilevel converters tend to have switching redundancies.
- *Application practicality*: Multilevel converters allow for the utilization of smaller, more reliable components.
- *Ride through capability*: Under emergency conditions, like when voltage sags or load swings are experienced at the utility connection, the multilevel converter can also be used to provide ride-through capability if the DC sources are banks of batteries or capacitors.

Unfortunately, multilevel converters do have some disadvantages as listed below [1–4].

- It uses a greater number of power semiconductor switches. Although lower rated switches can be utilized but each switch requires a related gate drive circuit. It may lead to a more expensive and complex system (part of the increased cost may be offset by the fact switches with lower ratings are being used). Using more devices also means the probability of a system failure will increase.
- Another disadvantage of multilevel converters concerns control of the switches. The increased number of switches will result in more complicated control.
- A multilevel converter arrangement requires several DC voltage sources, which are usually provided by capacitors. Balancing the voltages of these capacitors

according to an operating point is a difficult challenge. Capacitors are also prone to failure.

- The number of the achievable voltage levels is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints, complexity of the controller, and, of course, capital and maintenance costs.

Despite these drawbacks, multilevel converters have emerged as the most preferred candidate for high power applications. Furthermore, as prices of power semiconductors and other associated components continue to decrease, the use of multilevel topologies is expected to extend to medium/low power applications (those of less than 10 kW) as well. Fast power devices (e.g., CMOS transistors), which can operate at very high switching frequencies, can be used for low voltages. Therefore, the values of the reactive components will undergo significant reduction. Furthermore, new power devices are expected to appear in the near future and these may also extend the application of multilevel topologies.

During the last two decades, several state-of-the-art multilevel converter topologies have been introduced by both academia and industries. These topologies can be broadly classified in two groups namely; (i) Monolithic converters and (ii) Modular converters. Both the VSC and CSC configurations are available for these topologies. The monolithic VSC and CSC topologies have been described first in the following section.

2.2 Monolithic Multilevel Converters

Several types of monolithic multilevel converters have been proposed based on different structures of their DC voltage (or current) sources to generate staircase output voltage (or current) levels. The two most actively developed of these topologies are the diode-clamped multilevel converter and flying capacitor multilevel converter. There are other names also used to define these topologies. For example, when referring to the three-level diode-clamped converter, it is called the neutral-point-clamped (NPC) converter. Similarly, the flying capacitor converter is also known as floating capacitor and capacitor clamped converter. In the following sub-sections, these two monolithic multilevel converter topologies have been described. The intention is to give a brief review of these basic topologies with their specific features, advantages, drawbacks, operating principles and their comparison.

2.2.1 Diode-Clamped Multilevel Converter (DCMC)

The first practical (and still widely studied) multilevel topology is the neutral-point-clamped (NPC) PWM topology first introduced by Nabae et al., in 1981 [26]. This is essentially a three-level diode-clamped Converter. The VSC and CSC configurations of DCMC are described in the following sub-sections.

2.2.1.1 DCMC

Figure 2.6 shows the three-phase NPC topology. The NPC consists of two pairs of series switches (e.g., S_1, S_2 and S_{11}, S_{21} in phase-a, Fig. 2.6) in each phase. The DC-link consists of two series capacitors (C_1, C_2 in Fig. 2.6). In each phase, two diodes, called the clamping diodes are used (e.g., D_1, D_2 in phase-a, Fig. 2.6) where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the total DC-link voltage into smaller voltages, which is shown in Fig. 2.6. If the point n is taken as the ground reference, the three possible phase voltage outputs are $-V_{dc}/2, 0$, and $V_{dc}/2$. The line-line voltages of two legs with the common DC capacitors are: $V_{dc}, V_{dc}/2, 0, -V_{dc}/2$ and $-V_{dc}$. Table 2.1 lists the switching states for producing three-level phase voltage outputs per phase in the topology of Fig. 2.6. As is evident from this table that the switch pairs (S_1, S_{11}) and (S_2, S_{21}) are complementary. Similar switch states exist in all the three phases to produce corresponding three-level voltage outputs. The key components that distinguish this circuit from a conventional two-level converter are the clamping diodes. These diodes clamp the switch voltage to half the level of the DC-link voltage. For example, when both S_1 and S_2 turn on, the voltage across a and n is $V_{dc}/2$, i.e., $V_{an} = V_{dc}/2$ (Table 2.1). In this case, D_{11} balances out the voltage sharing between S_{11} and S_{21} with S_{11} blocking the voltage across C_1 and S_{21} blocking the voltage across C_2 .

The three-level topology discussed above can be extended to higher-level configurations. Several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static

Fig. 2.6 Three-phase three-level structure of a DCMC

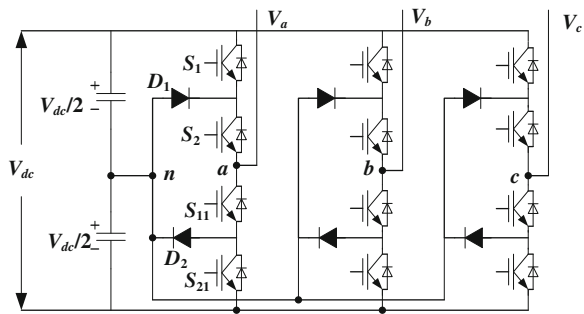


Table 2.1 Switching scheme for NPC

S_1	S_2	S_{11}	S_{21}	V_{an}
1	1	0	0	$V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

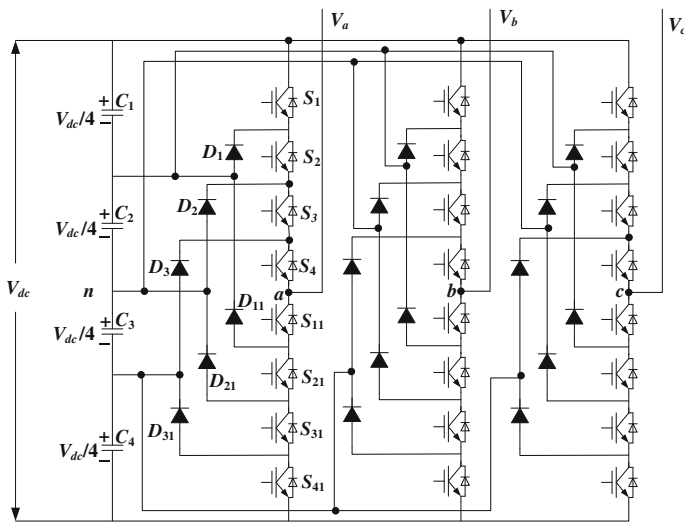


Fig. 2.7 Three-phase five-level structure of a diode-clamped multilevel converter

VAr compensation, variable speed motor drives, and high-voltage system inter-connections, etc. [1–4, 27]. A three-phase five-level DCMC is shown in Fig. 2.7. Each of the three phases of the converter shares a common DC bus, which is subdivided by four capacitors into five levels. The voltage across each capacitor is $V_{dc}/4$, and the voltage stress across each switching device is limited to $V_{dc}/4$ through the clamping diodes. Table 2.2 lists the possible output voltage levels for one phase of the five-level converter with the neutral point n taken as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has four complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg a are (S_1, S_{11}) , (S_2, S_{21}) , (S_3, S_{31}) and (S_4, S_{41}) . Table 2.2 also shows that four adjacent main devices are on and in series for any voltage level output. For the higher voltage levels ($V_{dc}/2$, $-V_{dc}/2$), the four on devices clamp the phase output to the top or bottom of the DC bus. For the lower voltage levels ($-V_{dc}/4$, 0 , $V_{dc}/4$), the on devices together act as a short connecting two of the clamping diodes back-to-back. The other end of these back-to-back

Table 2.2 Switching scheme for a five-level diode-clamped converter

S_1	S_2	S_3	S_4	S_{11}	S_{21}	S_{31}	S_{41}	V_{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

clamping diodes are connected to one of the nodes (2, n , or 3, Fig. 2.7) along the DC bus. The circuit then can be thought of as a type of multiplexer, attaching the output to one of the five available voltage levels.

Figure 2.8 shows a line-line voltage output of a five-level converter, which is a nine-level waveform. This means that an m -level DCMC has an m -level output phase voltage and a $(2m - 1)$ -level output line voltage.

In a DCMC, although each active switching device is required to block only a voltage level of $V_{dc}/4$, the clamping diodes require different ratings for reverse voltage blocking. Using phase a of Fig. 2.7 as an example, when all the lower switches S_{11} through S_{41} are turned on, D_3 must block three voltage levels, or $3V_{dc}/4$. Similarly, D_2 must block $V_{dc}/2$ and D_1 must block $V_{dc}/4$. This rule can be similarly defined for an m -level converter. If the converter is designed such that each blocking diode has the same voltage rating as the active switches then D_n and D_{n1} (for $n = 1, 2$, or 3) in Fig. 2.7 will require n diodes in series. Consequently, the number of diodes required for each phase would be $(m - 1) \times (m - 2)$. Similarly, an m -level converter requires $(m - 1)$ capacitors at the DC bus as is also evident from Figs. 2.6 and 2.7. Also, each phase leg consists of $2 \times (m - 1)$ active switches. The net DC voltage (V_{dc} , Figs. 2.6 and 2.7) should be evenly distributed among the DC capacitors for having symmetric and desired m -level waveform.

It should be noted that DCMCs with odd number of levels ($m = 3, 5, 7, \dots$) offer a neutral point access. It is also possible to synthesize topologies with even number of levels ($m = 4, 6, 8, \dots$). However, in single-phase applications where a neutral point is needed, DCMC with even number of levels cannot be used. Though they have proven to be well suited for drive applications [27].

The DCMC is the most researched topology among the different multilevel converter topologies. One application of the DCMC is an interface between a High Voltage DC (HVDC) transmission line and an AC transmission line [28]. Another application is a variable speed drive for high-power medium-voltage (2.4–13.8 kV)

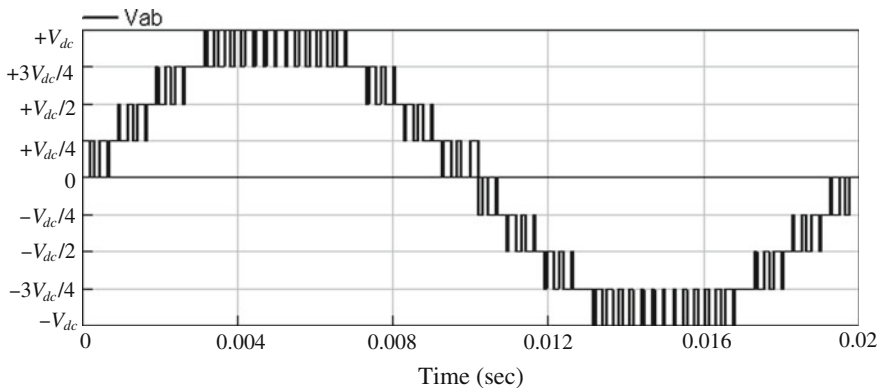


Fig. 2.8 Line voltage waveform of a five-level diode-clamped converter

motors. For drives applications, it is the most widely used structure [27]. STATCOM is another application where the DCMC has found wide acceptance. The world's first UPFC was based on DCMC [14, 15]. Some recent proposals for the STATCOM applications are also based on DCMC [18–22].

The main advantages and disadvantages of multilevel diode-clamped converters are as follows [1–4, 27].

Advantages

- All phases share a common DC bus, which minimizes the capacitance requirements of the converter. Therefore, a back-to-back topology is possible and also practical for uses such as a HVDC and an adjustable speed drive.
- The DC capacitors can be easily precharged as a group unlike the other multilevel converter structures, where precharging and startup are more complex.
- The current ripple in the capacitors is of the order that is greater and or equal to 3rd harmonics (in the flying capacitor converter, the capacitors current ripple may be of the order of fundamental frequency or greater depending on the modulation strategy).
- Although some additional clamping diodes are required, it requires a low number of capacitors. A low number of reactive components is usually preferred from the standpoint of cost.

Disadvantages

- For more than three-level DCMC structure, the voltage stresses across the clamping diodes are non-uniform. For example, in Fig. 2.7, D_1 , D_{31} are subjected to the voltage stress of $V_{dc}/4$, D_2 , D_{21} are subjected to the voltage stress of $V_{dc}/2$, and D_{11} , D_3 are subjected to the voltage stress of $3V_{dc}/4$. This issue complicates the design and raises reliability and cost concerns.
- For some operating conditions, it has been demonstrated that the charge balance of the DC capacitors cannot be achieved in topologies with a high number of levels (more than three). These balancing problems appear when dealing with high modulation indices and active currents. Therefore, the achievable AC output voltages kept limited. Some solutions for this problem are proposed in the literature.
- When switched in PWM, the reverse recovery of the clamping diodes becomes the major design challenge in high voltage high power applications. Although measures to alleviate this problem can be applied.
- It requires different current ratings for switches due to their conduction duty cycle. This can be verified from Table 2.2 where it can be seen that S_1 conducts only for $V_{an} = V_{dc}/2$, while S_4 conducts over the entire cycle except for $V_{an} = 0$. Such an unequal conduction duty requires different current ratings for switching devices. If the converter design is to suit the worst case then each phase will have $2 \times (m - 2)$ outer devices oversized.

Despite the limitations as mentioned above, the three-level NPC is still the most popular topology that has found widespread practical applications. Its simple structure enables excellent reliability and availability [27]. Based on the highly

competitive Insulated Gate Controlled Thyristor (IGCT) technology a very compact NPC IGCT PEBB, called PowerStack, serving multiple medium-voltage applications has been introduced to the market and the first commercial installations were commissioned in the year 2000 [28]. The NPC IGCT PEBB has been successfully introduced into the market to serve multiple, highly demanding, mature and emerging applications like 15–60 MVA energy storage systems based on regenerative fuel cell technology or NiCd battery technology to enhance grid stability or to reduce power fluctuations, 9–27 MVA medium-voltage applications, and 22 MVA dynamic voltage restorers to safeguard the highly critical processes of a semiconductor plant.

One of the main structural limitations of the 3-level NPC is the asymmetrical loss distribution. To make the loss distribution uniform across the semiconductors, active switches can be used in place of the clamping diodes and the resulting circuit is called three-level Active NPC (ANPC), introduced first in 2001 [29]. Higher level ANPCs can be similarly derived. Based on ANPCs, a wide range of high power MV drives, and STATCOMs are available in the market [27]. The new technologies introduced with the ANPC IGCT have been developed to further improve the power density and the cost competitiveness of the leading IGCT technology which is able to deliver up to 16 MVA output power. The main new technologies introduced to achieve higher output powers are: increased current rating of IGCTs and improved thermal management by means of the ANPC topology [30]. The distribution of junction temperatures among the semiconductors can be balanced applying optimum switch states and commutations.

As discussed above, one of the major problems associated with DCMCs is the unbalancing (or unequalization) of its DC-link capacitors voltage. Marchesoni et al. have theoretically demonstrated that correct voltage balancing of these capacitors cannot be guaranteed in all operating conditions with a large number of levels [32]. Since those conditions include high modulation indices and high power factors, it limits the practical applications of these converters. The unbalancing of DC capacitors voltage results in divergence of capacitor voltages, causing collapse of some and rise of others due to non-uniform power drawn from them. This may result in poor quality voltage outputs, affecting the control performance, causing violation in the safe operating limits leading to converter malfunctioning. Therefore, the DC capacitors voltage balancing is required under all conditions, which determines both the safety and efficiency of DCMCs. Two possible solutions of the voltage imbalance exist: (i) installing of voltage balancing circuits on the converter DC side [20, 21, 32] and (ii) modifying the converter switching pattern according to a control strategy [31, 33]. The latter is preferable in terms of cost, as the former requires additional power hardware, which adds to cost and complexity. For applications involving only reactive power (like STATCOM), the switching pattern modification strategies can be used for voltage balancing. However, reactive power control would be influenced if priority were given to voltage balancing. Further, the switching pattern modification strategy cannot be used to control the capacitor voltages, except at low modulation indices [31]. It is also to be noted that for the applications like UPFC, where two such converters are back-to-back connected, the

switching modification strategy necessitates the two converters to operate at a fixed AC voltage ratio for the capacitor voltages equalization. This constraint would seriously limit the flexibility of the UPFC. The voltage balancing circuit based solutions have also been reported for many applications. A schematic of the voltage balancing circuit is shown in Fig. 2.9, where the semiconductor switches (S_{C1} , D_{C1}) – (S_{C4} , D_{C4}) and inductors L_1 , L_2 are chopper elements while R_1 , R_2 represent the losses. This chopper is shown to be connected to the DC-link of a single-phase DCMC. It works on the principle of transferring the energy from the overcharged capacitor to the undercharged one through an energy storing inductor. In this way, the capacitor voltages at the DC-link are equalized. Although the inclusion of such circuit increases the cost and complexity, it is more reliable and robust against line faults, transients and disturbances. Further, it does not impose any theoretical limits on the operating range of the converter, as is the case with other available methods. Even though utilization of these additional balancing circuits can improve the operation of multilevel converters, the devices of these circuits have to handle high current and voltage ratings, sometimes higher than ratings of the devices of main converter. A voltage balancing circuit employing lower voltage rating devices was proposed in [34]. In [32], four different schemes were presented for controlling of the chopper circuit at DC-bus of DCMC for DC capacitor voltages equalization.

One of the limitations of DCMCs as described above is multiple blocking voltage of the clamping diodes. To overcome this limitation, a modified DCMC configuration was proposed in [35] with the single-phase schematic shown in Fig. 2.10 for the five-level topology. An m -level modified DCMC requires $(m - 1)$ storage capacitors, $2(m - 1)$ switches and $(m - 1) \times (m - 2)$ clamping diodes of same voltage rating, which are the same with the conventional DCMC with

Fig. 2.9 Single-phase five-level DCMC with voltage balancing chopper circuit

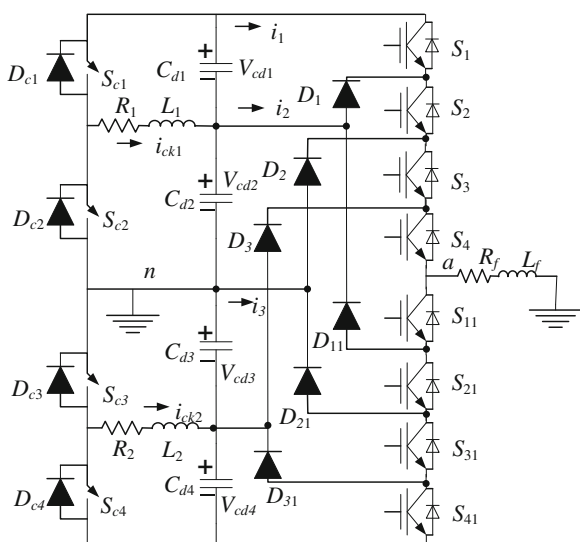
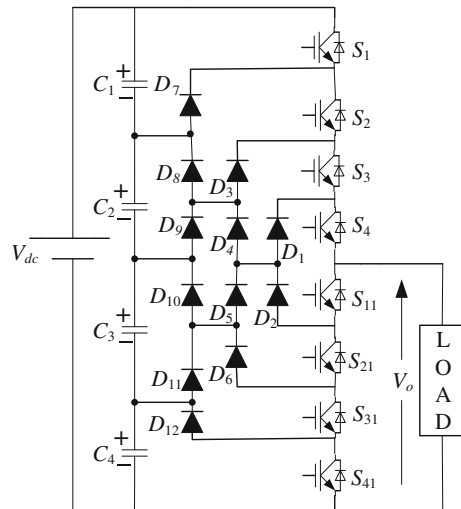


Fig. 2.10 Single-phase five-level schematic of the modified DCMC



clamping diodes in series. The switching scheme for the modified configuration remains same as that for the conventional configuration. However, the main limitation of DCMC, i.e., the unbalancing of its DC-link capacitors voltage is still not resolved for this modified configuration too.

To illustrate the balancing of DC capacitor voltages in DCMC, a three-phase five-level DCMC is simulated with the voltage balancing chopper of the configuration shown in Fig. 2.9 and controlled using the single-pulse control method described in [32]. In Fig. 2.11, e_{vcd1} and e_{vcd2} represent the errors in the corresponding DC capacitor voltages. It is evident from this figure that the capacitor

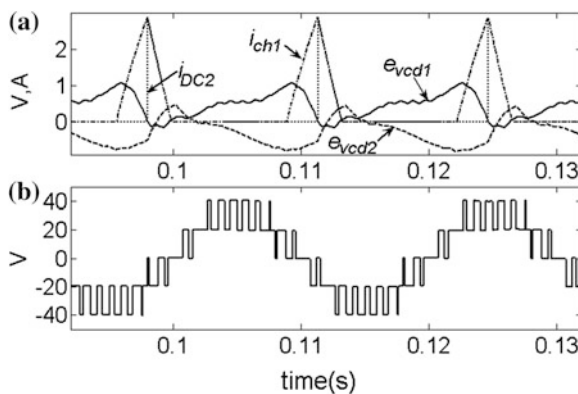
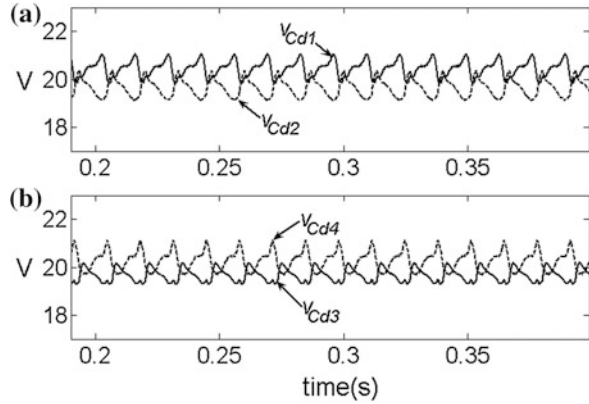


Fig. 2.11 Key results illustrating DC capacitors voltage balancing using voltage balancing chopper circuit in five-level DCMC modulated using PD PWM. **a** Capacitor voltage errors and chopper current, **b** phase-a converter output voltage

Fig. 2.12 Key results illustrating DC capacitors voltage using voltage balancing chopper circuit in five-level DCMC modulated using PD PWM



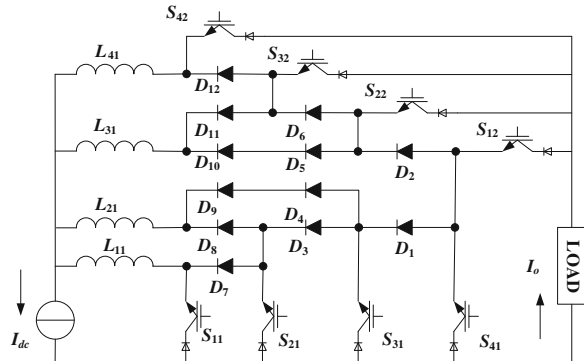
voltages are regulated around at their reference value, i.e., 20 V. As the capacitor voltages are balanced, the converter output phase voltage is of good quality five-level waveform as can be seen from Fig. 2.12. The other phase output voltages also have similar waveform.

For STATCOM applications, a CSC has also found to be suitable due to its various advantages [36]. Being a current injection device, the CSC topology injects smaller current harmonics than the voltage harmonics injected by an equivalent VSC based STATCOM. Moreover, a CSC when used to realize a STATCOM requires lower DC energy storage than that of VSC. A VSC and an equivalent CSC are considered to be a pair of dual structures. The multilevel CSC topologies are derived from the dual transform of the corresponding multilevel VSC topologies [9]. In the following sub-section, the dual CSC configuration of DCMC is described.

2.2.1.2 Dual CSC Structure of DCMC

It is known that only planar circuits can be transformed using the duality principle. A planar circuit is a circuit that can be drawn on a plane with no crossing branches. It can easily be verified that the DCMC circuit of Figs. 2.6 and 2.7 are not planar while the modified DCMC topology of Fig. 2.10 is planar. Therefore, the duality transformation can be applied to the circuit of Fig. 2.10 only. As discussed earlier, in duality transformation, the controlled bidirectional conducting switches are transformed into controlled unidirectional switches and capacitors are transformed into inductors. The dual structure of the circuit of Fig. 2.10 is shown in Fig. 2.13, where similar to its VSC counterpart there are four complementary switch pairs: (S_1, S_{11}) , (S_2, S_{21}) , (S_3, S_{31}) and (S_4, S_{41}) [9]. In Fig. 2.10, the DC capacitors $C_1 - C_4$ corresponds to equal division of DC voltage source V_{dc} . Similarly, in Fig. 2.13, the inductors $L_1 - L_4$ correspond to equal division of DC current source

Fig. 2.13 Dual structure of Fig. 2.9



I_d , so that the current carried by each inductor is $(1/4)I_d$. Further, each inductor current passes through only one complementary switch pair. For example, the current through L_1 passes only through the switch pair (S_1, S_{11}) and so on. Based on these considerations, the dual circuit of Fig. 2.10 can be further simplified to the one shown in Fig. 2.14. This topology is called single-rating inductor topology as the DC source current I_d is divided equally among all the inductors. The switching scheme of the circuit of Fig. 2.14 is listed in Table 2.3 for five levels of load current values.

Using different switching states, it is possible to synthesis a multilevel current waveform as a dual of the voltage waveform in VSC NPC. However, similar to the VSC type NPC structure, special consideration needs to be paid on the proper current sharing between the inductors. It is apparent that unbalance current in different inductor branches leads to an excessive current flow through the devices and thus the device failure is occurred. Although the proper current sharing is difficult for the higher level NPC type CSC, similar methods presented for voltage sharing of the VSC type converter is applicable for the CSCs.

Fig. 2.14 Single phase single-rating inductor five level CSC

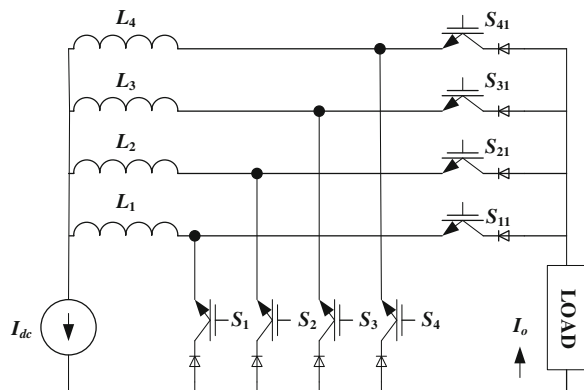


Table 2.3 Switching scheme of the single-rating inductor five-level CSC

I_o	Switching scheme							
	S_1	S_2	S_3	S_4	S_{11}	S_{21}	S_{31}	S_{41}
0	1	1	1	1	0	0	0	0
$I_{dc}/4$	0	1	1	1	1	0	0	0
	1	0	1	1	0	1	0	0
	1	1	0	1	0	0	1	0
	1	1	1	0	0	0	0	1
$I_{dc}/2$	0	0	1	1	1	1	0	0
	1	1	0	0	0	0	1	1
	0	1	0	1	1	0	1	0
	0	1	1	0	1	0	0	1
	1	0	1	0	0	1	0	1
	1	0	0	1	0	1	1	0
$3I_{dc}/4$	0	0	0	1	1	1	1	0
	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
I_{dc}	0	0	0	0	1	1	1	1

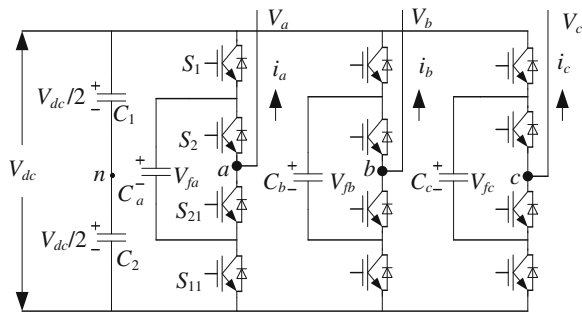
2.2.2 Flying Capacitor Multilevel (FCM) Converter

Meynard and Foch introduced a flying-capacitor multilevel converter (FCMC) in 1992 [37]. The VSC and CSC configurations of FCMC are described in the following sub-sections.

2.2.2.1 FCM VSC

The structure of FCMC is similar to that of the diode-clamped converter except that instead of using clamping diodes, the converter uses capacitors in their place. In FCMC, the clamping capacitors which ‘float’ with respect to the DC source are used to achieve multilevel waveform and voltage clamping. These floating capacitors are commonly called as ‘flying capacitors’ and due this arrangement this topology is named as flying capacitor topology. In the three-level flying capacitor topology shown in Fig. 2.15, the capacitors C_a , C_b and C_c are flying capacitors of the three individual phase legs and C_1 , C_2 constitute the DC-link, and the complementary switch pairs are (S_1, S_{11}) and (S_2, S_{21}) . It is to be noted that the complementary pair of a switch in the upper half of a phase leg is placed differently in the lower half of the phase leg in flying capacitor topology in contrast to that in the diode-clamped topology, which can be seen by comparing Figs. 2.4 and 2.15. In the three-level converter of Fig. 2.15, all the capacitors shown are regulated at a voltage of $V_{dc}/2$. Depending on the modulation scheme used, the three-level converter is

Fig. 2.15 Three-phase 3-level structure of a FCM VSC



switched in such a way to maintain the flying capacitors voltage at $V_{dc}/2$. By doing so, the voltage stress across the semiconductor devices also keeps limited to $V_{dc}/2$. The flying capacitor voltage balancing is achieved by using the redundant switch states available to generate same voltage level at the converter output in this topology. This is further evident from Table 2.4 in which the switching states for producing three-level voltage outputs per phase are listed with respect to the topology of Fig. 2.15. It can be seen that two different switching states can produce '0' voltage level. The corresponding states of flying capacitor with respect to the voltage level output are also listed in Table 2.3. Turning on S_1 , S_2 together outputs $+V_{dc}/2$ without changing the state of C_a , which is represented by NC state of the flying capacitor in Table 2.4. Similarly, turning off S_1 , S_2 together outputs $-V_{dc}/2$ with NC state of C_a . However, when S_1 -ON and S_2 -OFF are chosen to output '0' voltage level, charging of C_a is achieved while its discharging is achieved by choosing S_1 -OFF and S_2 -ON for 0 voltage level output. It is to be noted that the switch states listed in Table 2.4 are only for positive half cycle of the converter line current waveform (i_a , Fig. 2.15), which is equivalent to the outgoing direction of i_a as shown in Fig. 2.15. For negative half cycle of i_a (incoming i_a), the capacitor states in Table 2.4 for zero voltage level will reverse which can be also analyzed from Fig. 2.15.

It is clear from the configuration of Fig. 2.15 and Table 2.4 that intermediate voltage levels (except the extreme voltage levels $+V_{dc}/2$ and $-V_{dc}/2$) at the converter output are generated by adding or subtracting the flying capacitor voltage with the DC-link voltage. In a generalized way, for any initial state of flying capacitor voltage the three-level FCM VSC output voltage is given by,

Table 2.4 Switching scheme for three-level FCM VSC

S_1	S_2	V_{an}	C_a
ON	ON	$+V_{dc}/2$	No change (NC)
ON	OFF	0	Charging (+)
OFF	ON	0	Discharging (-)
OFF	OFF	$-V_{dc}/2$	No change (NC)

$$V_{an} = S_1(V_{dc} - V_{fa}) + S_2 V_{fa} - V_{dc}/2 \quad (2.1)$$

In (2.1), the switching states S_1 and S_2 take the value 1 if the corresponding switch is conducting and 0 otherwise. Based on (2.1), the switch combinations given in Table 2.4 are used to synthesize the output voltage V_{an} of phase- a with respect to n .

In a similar manner as in the diode-clamped topology, higher level flying capacitor topology can be formed by extending the three-level structure of Fig. 2.15. In Fig. 2.16, a three-phase five-level FCM VSC is shown. Assuming that each capacitor has the same voltage rating, the series connection of capacitors in Fig. 2.16 is to indicate the voltage level between the clamping points. Again, three inner loop flying capacitors for phase- a , C_{f1} , C_{f2} and C_{f3} are independent from those for the other two phases. Similar independence exists among all the three phases. All phase legs share the same DC-link capacitors C_1 .

Similar to that in a DCMC, the phase voltage of an m -level converter has m levels and the line voltage has $(2m - 1)$ levels. In general, an m -level flying capacitor converter requires $(m - 1)$ pairs of power semiconductor devices and $(m - 1) \times (m - 2)/2$ clamping capacitors per phase leg in addition to $(m - 1)$ main DC bus capacitors provided that all the capacitors are of same size. The number of capacitors can be reduced by sizing the capacitors in a single leg as an equivalent one. In this chapter, from here onwards, a single capacitor, sized equivalently in each clamping leg of the flying capacitor converter has been considered. The size of the voltage increment between two consecutive clamping legs defines the size of voltage steps in the output waveform. The voltage of the innermost clamping leg (e.g. C_{f3} in

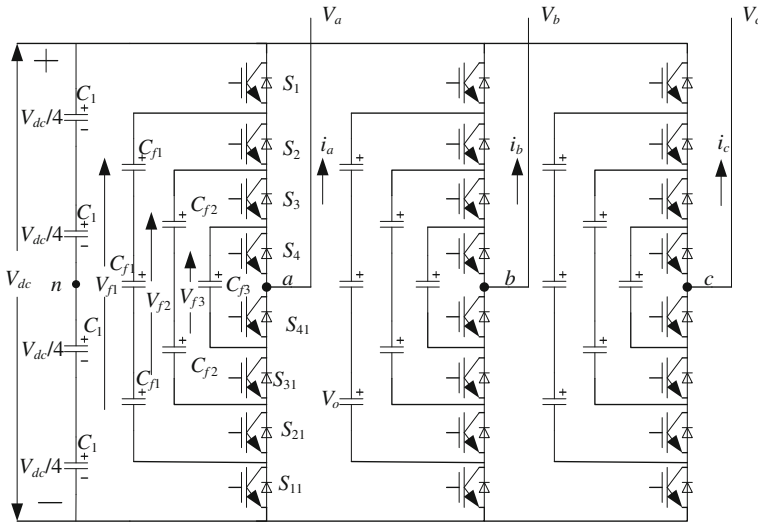


Fig. 2.16 Three-phase five-level structure of a FCM VSC

Fig. 2.16) clamping the innermost two devices is $V_{dc}/(m-1)$. The voltage of the next innermost clamping leg will be $V_{dc}/(m-1) + V_{dc}/(m-1) = 2V_{dc}/(m-1)$ and so on. Thus, each next clamping leg will have the voltage increment of $V_{dc}/(m-1)$ from its immediate inner one. The voltage stress across each capacitor is $V_{dc}/(m-1)$. The voltage levels and the arrangements of the flying capacitors in this topology assure that the voltage stress across each main device is same and is equal to $V_{dc}/(m-1)$. Similar to the phase output voltage equation defined by (2.1) for the three-level topology, the five-level converter output voltage is given by

$$V_{an} = S_1(V_{dc} - V_{f1}) + S_2(V_{f1} - V_{f2}) + S_3(V_{f2} - V_{f3}) + S_4 V_{f3} - V_{dc}/2 \quad (2.2)$$

Again, as defined earlier, the switching states S_{1-4} take the value 1 if the corresponding switch is conducting and 0 otherwise in (2.2). Based on (2.2), the switch combinations given in Table 2.5 are used to synthesize the output voltage V_{an} of phase-a of the five-level converter. Table 2.5 also indicates the states of flying capacitors corresponding to the switching combinations chosen. The state NC indicates that the capacitor neither charges nor discharges in this mode. The states + and - denote the charging and discharging of the corresponding capacitors respectively. The switching states given are for the positive half cycle of the current waveform (indicated as outgoing current i_a in Fig. 2.16). The capacitor states (+ and -) will reverse for the negative half cycle of the current.

It can be seen from Table 2.5 that the structure offers multiple switching combinations for $V_{an} = V_{dc}/4, 0$ and $-V_{dc}/4$. As such redundancies are available, one can choose a preferential switching state that will help in maintaining the capacitor voltages constant. This redundancy is enough to guarantee balanced voltages of the

Table 2.5 Switching scheme for five-level FCM VSC

S_1	S_2	S_3	S_4	C_{f1}	C_{f2}	C_{f3}	V_{an}
ON	ON	ON	ON	NC	NC	NC	$+V_{dc}/2$
ON	ON	ON	OFF	NC	NC	+	$+V_{dc}/4$
ON	ON	OFF	ON	NC	+	-	
ON	OFF	ON	ON	+	-	NC	
OFF	ON	ON	ON	-	NC	NC	
OFF	OFF	ON	ON	NC	-	NC	
OFF	ON	OFF	ON	-	+	-	
OFF	ON	ON	OFF	-	NC	+	0
ON	OFF	OFF	ON	+	NC	-	
ON	OFF	ON	OFF	+	-	+	
ON	ON	OFF	OFF	NC	+	NC	
ON	OF	OFF	OFF	+	NC	NC	
OFF	ON	OFF	OFF	-	+	NC	
OFF	OFF	ON	OFF	NC	-	+	
OFF	OFF	OFF	ON	NC	NC	-	
OFF	OFF	OFF	OFF	NC	NC	NC	$-V_{dc}/2$

flying capacitors using proper modulation technique. However, the switching combination chosen affects the current rating of the capacitors. For example, for $V_{an} = V_{dc}/4$, if the first and the last combinations are used (Table 2.5), only one capacitor (C_4 or C_2) is involved. In the other two combinations more than one capacitor are required to be charged or discharged. Therefore, the rms current ratings of the capacitors will necessarily be higher for the single capacitor case than that in the two-capacitor case. This feature of different current rating is present in almost every case (except for the levels of $V_{dc}/2$ and $-V_{dc}/2$). The switching sequence chosen therefore affects the rms current ratings of the capacitors. Thus, optimization of the switching sequence is required, i.e. one which minimizes the capacitor cost and the system losses. As compared to DCMC, the FCMC topology has the advantage that it has redundancies for inner voltage levels, as observed above. Moreover, FCMC has *phase* redundancies, whereas DCMC has only *line-line* redundancies. Unlike DCMC, the FCMC does not require all of the switches that are on (conducting) be in a consecutive series. In DCMC, to avoid the recovery problem associated with the diode, the switching modulation is limited to provide for the voltage unbalance between each leg. Since the FCMC has a wealth of redundant switching states, there are enough combinations between switching states to provide for voltage balancing. Furthermore, compared to DCMC, the FCMC eliminates a mid-capacitor point for each switch pair which results in simple converter structure. The drawback of FCMC is that its control is more complicated and it requires a large number of capacitors. Fortunately, the size of flying capacitors can be reduced by an increased switching frequency [38–41].

After the introduction of FCMC in the 1990s, there have been numerous articles published related to this topology. Both industries as well as academia have shown significant interest in the FCMC topology and its various applications have been explored. At present, around 80 T13 locomotives in the European railways use this topology as input chopper [42]. In the drive applications, as early as 1996, Cegelec (which later became ALSTOM Industry) showed interest in FCMCs and development using the biggest IGBTs available at that time was initiated. Today, a complete range of such drives is proposed to comply with the European standards. For power systems compensation applications as well, the flying capacitor converter has gained significant interests. In [43], a five-level FCMC is selected and designed for a 6.6 kV STATCOM. To decrease size of the flying capacitor by increasing a switching frequency, the Auxiliary Resonant Commutated Pole (ARCP) Converter is used, and its parameters are optimized based on loss-implemented simulation.

In summary, advantages and disadvantages of FCM VSC are as follows [1–4, 37–43].

Advantages

- Large amount of capacitors, in terms of the flying capacitors, may provide extra ride through capabilities during power outages.
- The redundant switching combinations provide added flexibility in controlling and balancing the balancing different voltage levels.

- It eliminates the clamping diode problems present in DCMC topologies and the dv/dt stress across the devices is naturally limited.
- Unlike DCMC, the redundant switching states in FCMC can control the charge balance in all flying capacitors, even if the phase current is unidirectional. This makes this topology attractive even for the DC/DC converters.
- Each phase leg can be analyzed differently from the others. This is an important difference with DCMC, in which the entire three-phase system must be considered for the balancing issue (without using additional chopper circuits).

Disadvantages

- An excessive number of flying capacitors is required for higher level converter configuration. Such configurations are expensive and more difficult to package with the required bulky capacitors.
- The flying capacitor voltage controller adds complexity to the control of the whole circuit.
- The rms current rating of flying capacitors is higher.
- For low switching frequency operation, large sizes of flying capacitors are required.
- There is a potential for parasitic resonance between decoupling capacitors.
- Precharging and startup are more complex.

As detailed earlier, an FCMC uses flying capacitors to split the input voltage and clamp the voltage stresses across the semiconductor switches. It is the primary requirement of functioning of an FCMC is to have balanced flying capacitor voltages at their corresponding reference values as it dictates both the safe and efficient operation of the converter under all operating conditions. If voltage imbalance occurs, the quality of the output voltages will deteriorate and blocking voltages imposed on certain devices may increase the rated values. Therefore, it is necessary to take into account the balancing of flying capacitor voltages while designing the converter control schemes. Additionally, the evolution of the flying capacitor voltages must be carefully studied since the survival of the converter depends on it. There are many different control strategies available in the literatures taking into account the flying capacitor voltage balancing for FCMCs.

Many studies have shown that under certain conditions, a simple open loop control guarantees natural balancing of the flying capacitor [38–40]. The self-balancing mechanism ensures safe operation under most operating conditions where a high enough switching frequency is chosen and the load is not purely reactive [38, 39]. Nevertheless, in this case, the dynamics involved in the balancing transient depend on the impedance of load at the switching frequency. If the impedance at the switching frequency is high then the natural balancing is very slow and may not be guaranteed. Further, by using such an open-loop control, unbalance may occur in applications with low switching frequencies or if the reference waveform contains harmonics that are close to the switching frequency [38, 39]. Following these observations, a filter circuit of the R - L - C type (called, ‘balance-booster’) tuned at the switching frequency and connected in parallel with

the load may also be used to achieve the natural balancing [39]. It has the advantage of being reliable but the extra filter increases the cost of the overall system, introduces extra power losses especially in high-voltage applications and may be too slow to follow rapid variations of the input voltage [39]. While assuming the natural balancing of the flying capacitors voltages, it is considered that the capacitor voltages are balanced with each switching period provided that the control signals have the same duty cycles, the power devices have the same characteristics and the load currents are symmetrical. However, these conditions cannot be met in real systems due to non-ideal conditions and disturbances, such as unequal capacitance leakage currents, unequal delays in switching, asymmetrical charging/discharging of capacitors and load disturbances. Consequently, the voltages of flying capacitors will vary. Therefore, the need for an external control loop for each flying capacitor voltage may arise for most of its applications due to the dependency of the natural balancing quality on the modulation pattern as well as the load parameters [38–40].

To illustrate the natural balancing property of FCMC, simulation studies using PSCAD/EMTDC are performed on a single-phase five-level FCMC. It is evident from Fig. 2.17a that the flying capacitor voltages attain their target operating values confirming the natural balancing of FCMC. The converter switched output voltage and current are shown in Fig. 2.17b, c, respectively. The five different voltage levels in the phase leg confirms that the flying capacitor voltages have stabilized to their target operating values.

Fig. 2.17 Key results illustrating natural balancing when the single-phase five-level FCMC is modulated using PD PWM. **a** Flying capacitor voltages; **b** FCMC phase-leg switched voltage, and **c** load current in steady state

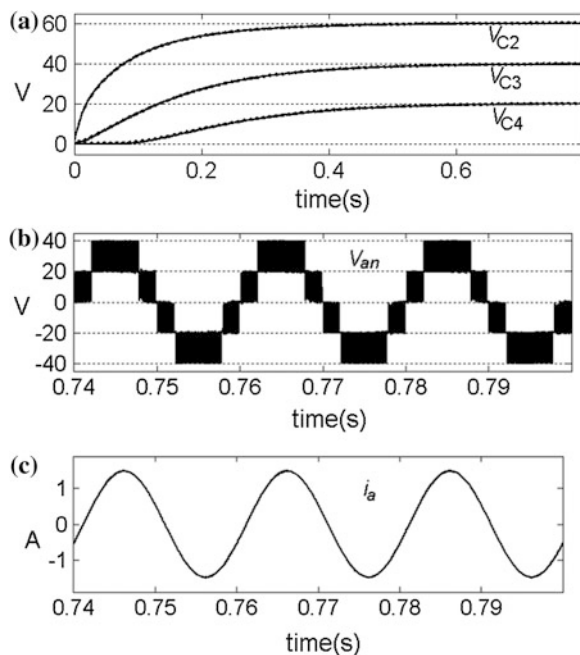
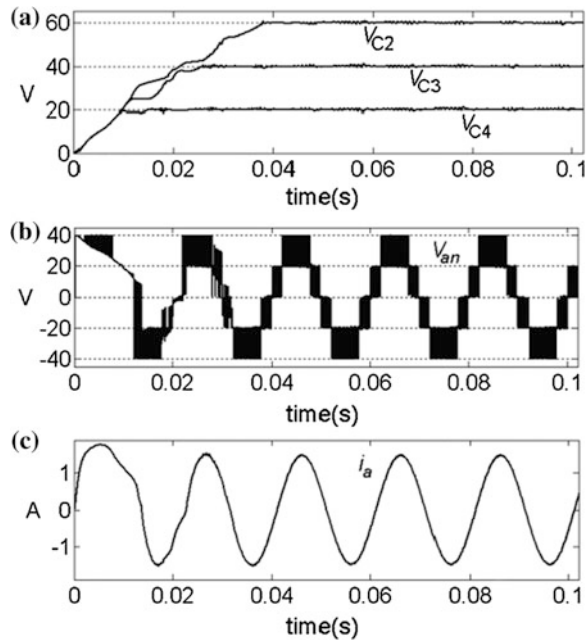


Fig. 2.18 Key results when the single-phase five-level FCMC is controlled using preferential switch state selection scheme. **a** Flying capacitor voltages; **b** FCMC phase-leg switched voltage, and **c** load current in steady state

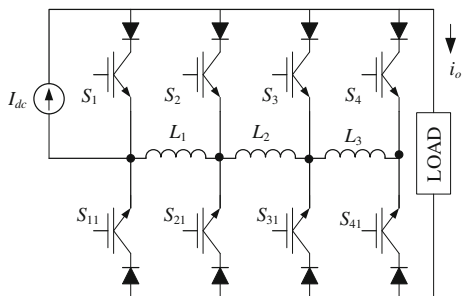


In Fig. 2.18, the simulation results using the preferential switch state selection scheme proposed in [18] are plotted with the same parameters as considered above. Figure 2.18a shows the start-up transient of the flying capacitor voltages with initially uncharged capacitors. It is evident by comparing the capacitor voltage transients of Figs. 2.17 and 2.18 that the rate of capacitors achieving their respective target voltage values is much faster in the latter case. Once the capacitor voltages reach their respective target values, they are tightly regulated around these values and hence, the load voltage and current achieve their desired waveform shapes as shown in Fig. 2.17.

2.2.2.2 Dual CSC Structure of FCMC

It can be observed from above that FCM VSC has a planar structure. Therefore, its CSC configuration can be derived directly by applying duality transformation. The dual structure of single-phase five-level DCMC configuration is shown in Fig. 2.19. The dual elements in phase- a of Fig. 2.16 and in Fig. 2.19 are represented by the same assignments. In phase- a of the five-level FCM VSC configuration of Fig. 2.16, the voltages across the flying capacitors are $V_{f1} = 3V_{dc}/4$, $V_{f2} = V_{dc}/2$ and $V_{f3} = V_{dc}/4$. Similarly, in Fig. 2.19, the current through the respective inductors are $3I_{dc}/4$, $I_{dc}/2$ and $I_{dc}/4$, respectively. This implies that all the inductors are of different current ratings. Hence, this configuration of Fig. 2.19 is named as multi-rating inductor converter. In Fig. 2.19, similar to its VSC counterpart there are four

Fig. 2.19 Single phase multi-rating inductor five level CSC



complementary switch pairs: (S_1, S_{11}) , (S_2, S_{21}) , (S_3, S_{31}) and (S_4, S_{41}) and its switching scheme is listed in Table 2.6 for five levels of load current values. As can be seen, the FCM CSC topology also offers redundant switching combinations. Therefore, in a similar way as in its dual VSC structure, it is possible to synthesize a multilevel current waveform in FCM CSC.

In FCM CSC topology, each semiconductor device blocks the peak line-to-line voltage and conducts I_{dc}/N . However, the inductors carry different current values (e.g., $I_{L1} = 2I_{L2}$). Parallel-connected identical inductors may be used to have a same design rating. With the same switching frequency, and power rating, the FCM CSC requires less energy storage for synthesizing the intermediate levels. This is because the inductors in a FCM CSC are shared by all three phases. However, this topology cannot be easily scaled up for a higher voltage levels.

Table 2.6 Switching scheme of the multi-rating inductor five-level CSC

I_o	Switching scheme							
	S_1	S_2	S_3	S_4	S_{11}	S_{21}	S_{31}	S_{41}
0	1	1	1	1	0	0	0	0
$I_{dc}/4$	0	1	1	1	1	0	0	0
	1	0	1	1	0	1	0	0
	1	1	0	1	0	0	1	0
	1	1	1	0	0	0	0	1
$I_{dc}/2$	0	0	1	1	1	1	0	0
	1	1	0	0	0	0	1	1
	0	1	0	1	1	0	1	0
	0	1	1	0	1	0	0	1
	1	0	1	0	0	1	0	1
	1	0	0	1	0	1	1	0
$3I_{dc}/4$	0	0	0	1	1	1	1	0
	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
I_{dc}	0	0	0	0	1	1	1	1

2.3 Modular Multilevel Converters

Modularity, in general, refers to a technique to develop comparably large systems by combining smaller subsystems. For power converter topologies this means, a cascaded connection of converter cells, so called chain-links, which seems to be an interesting solution to reach high voltage and high quality waveforms [1–4]. However, in order to transfer active power, isolated DC sources are required by means of a transformer and a rectification stage. This fundamental problem has been addressed in [44], opening a new field of possible new solutions. The solution proposed in [37], eliminates the need of separated sources in high power converters by means of an intermediate voltage source or current source, such as a capacitor or inductor, floating with respect to ground potential in the converter circuit. These intermediate sources with passive elements are actively balanced by means of the switching process of the converter. Other circuit configurations including voltage or current sources or their combinations can be tailored in order to make use of the modularity and scalability for high power applications. These solutions require a proper cell or a building block structure. The power electronics building block is an intermediate level towards the modular power converters that incorporate the integration of power devices, passive elements, and other components into functional blocks. Building blocks can be easily added in parallel to increase the current carrying capability or in series in order to handle considerably higher voltages. This section is to provide an overview of the modular multilevel converter topologies from the basic building blocks to the system level modularity, targeting high-power applications and in particular FACTS. As will be discussed further in this section, modular multilevel VSCs and CSCs can be built either straightforward by applying the modular building block cells or by a combination of cells with monolithic multilevel topologies. Therefore, this section summarizes the most recent developments made in this field, covering new promising topologies and operational issues. In addition, emerging trends, challenges, and possible future directions of the multilevel converter technologies are outlined to motivate further work in this field. The following sub-section discusses the first introduced modular topology of multilevel converter introduced in [45].

2.3.1 Chain-Link Multilevel Converters Based on Bipolar Cells

A cascade H-bridge inverter is a series connection of several H-bridges. This topology is the most obvious way of achieving a multilevel waveform. As stated earlier, the H-bridge inverter of Fig. 2.1b can produce voltage waveform with three discrete levels; $+V_{DC}$, 0 and $-V_{DC}$ where V_{DC} is voltage of its DC source. Therefore, a combination of a number of H-bridge inverters should be able to produce more than three level voltage output. Based on this concept the cascade H-bridge inverter

is constructed. A single-phase structure of an m -level cascaded inverter is illustrated in Fig. 2.20. Each Separate DC Source (SDCS) is connected to a single-phase H-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{DC}$, 0, and $-V_{DC}$ by connecting the DC source to the AC output by different combinations of the four switches, S_1 , S_2 , S_3 , and S_4 . To obtain $+V_{DC}$, switches S_1 and S_4 are turned on, whereas $-V_{DC}$ can be obtained by turning on switches S_2 and S_3 . By turning on S_1 and S_2 or S_3 and S_4 , the output voltage is 0. The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by $m = 2s + 1$, where s is the number of separate DC sources. An example of phase voltage waveform (v_{an}) for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Fig. 2.21. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$. Figure 2.21 provides an illustration of this idea of obtaining the total AC voltage produces by the multilevel inverter by adding together five distinct AC voltages of the five H-bridge inverters. Figure 2.21 also illustrates the idea of ‘levels’ in a cascaded H-bridges multilevel inverter. In this figure, one notices that five distinct DC sources can produce a maximum of 11 distinct levels in the output phase voltage of the multilevel inverter which is in justification of the expression $m = 2s + 1$ given above.

One of the earliest applications for the series connection of single-phase full bridge inverter topology was reported for plasma stabilization [46]. Later this approach was extended to include three-phase systems. Recently, the multilevel cascaded inverters have been proposed for such applications as static VAR generation, an interface with renewable energy sources, and for battery-based applications. Peng has demonstrated a prototype multilevel cascaded static VAR generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system [47]. The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the connected electrical system. It was also shown that a cascade inverter can be directly connected in series with the electrical system for static VAR compensation. Cascaded inverters are ideal for connecting renewable energy sources with an AC grid, because of the need for separate DC sources, which is the case in applications such as photovoltaics or fuel cells.

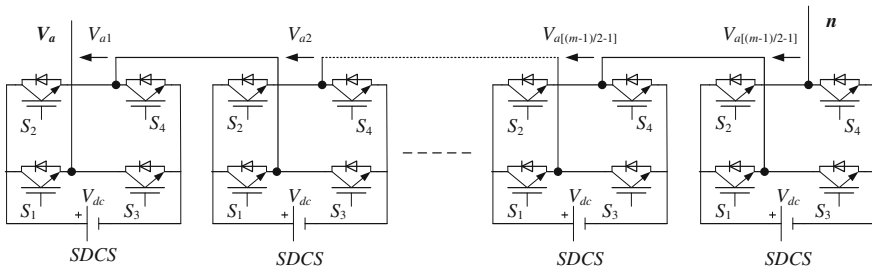


Fig. 2.20 Single phase structure of a multilevel cascaded H-bridge inverter

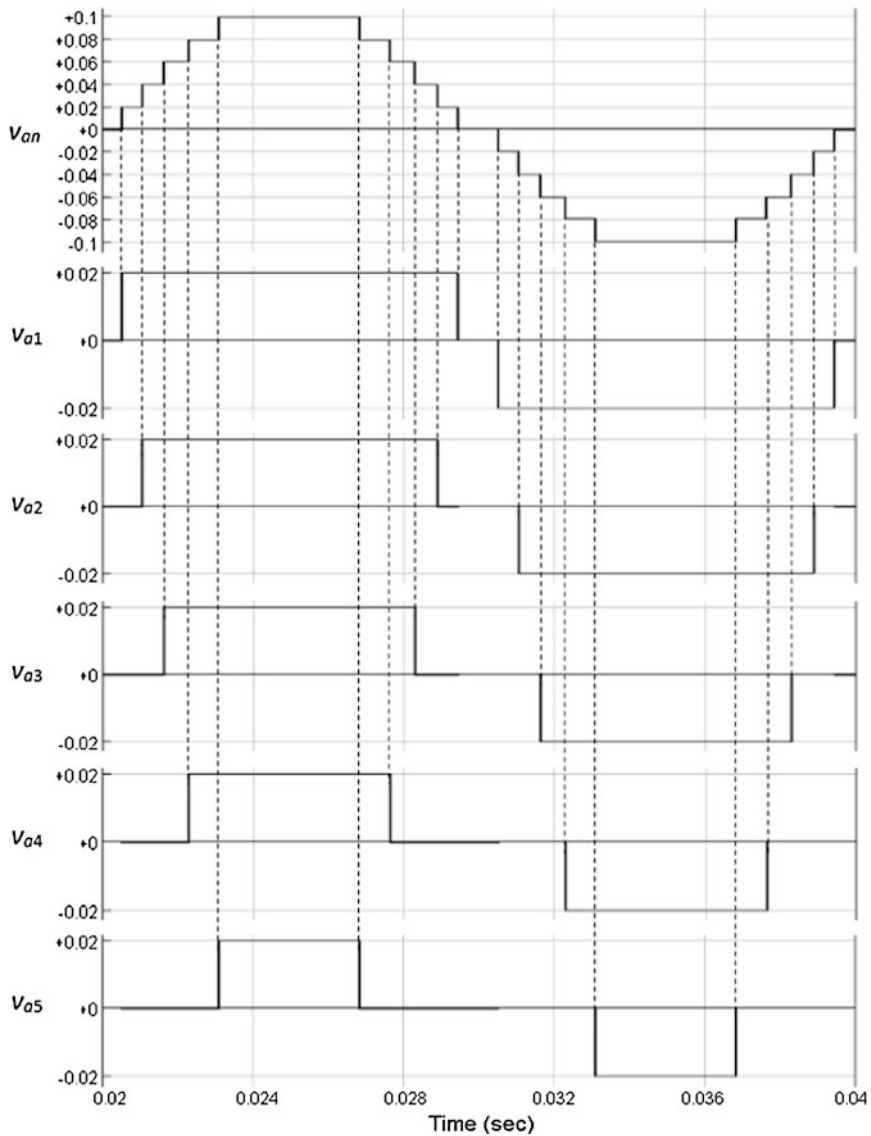


Fig. 2.21 Output phase voltage waveform of an 11-level cascade inverter with 5 separate DC sources

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra-capacitors are well suited to serve as SDCSs [48]. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an AC supply. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses

regenerative braking. Manjrekar has proposed a cascade topology that uses multiple DC levels, which instead of being identical in value are multiples of each other [49]. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for some other levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level. In the industrial community, Robicon Corporation commercialized their medium-voltage drives utilizing the cascaded multilevel topology in 1999. In 1998, GEC ALSTHOM T&D (now ALSTOM T&D) proposed to use the cascaded topology as a main power converter in their STATCOMs that are associated with the TSR and TCR. To date, several papers have discussed the configurations and control strategies for the reactive power compensation systems that utilize cascaded multilevel converters.

The main advantages and disadvantages of multilevel cascaded H-bridge structures are as follows [1–4, 47–50].

Advantages

- The series of H-bridges structure allows a scalable, modularized layout and packaging due to identical structure of each H-bridge. This will enable the manufacturing process to be done more quickly and cheaply.
- Requires the least number of components considering there are no extra clamping diodes or voltage balancing capacitors to achieve the same number of voltage levels.
- Potential of electric shock is reduced due to separate DC sources.

Disadvantages

- Separate DC sources are required for each of the H-bridges.
- The switching modulation needs to be optimized for high performance applications due to a limited combination of switching patterns.
- For reactive power exchange, the power pulsation at twice the output frequency occurring with the DC-link of each H-bridge inverter necessitates over-sizing of the DC-link capacitors.
- Due to number of DC capacitors voltage to be controlled in its FACTS and custom power applications, it has rather complex DC voltage regulation loop.
- Each H-bridge inverter faces unequal current stress.
- Connecting separate DC sources between two converters in a back-to-back arrangement (e.g., in UPFC) is not possible because a short-circuit will be introduced when two back-to-back converters are not switching synchronously.

In a similar way described for cascaded H-bridge converters, other monolithic multilevel converter configuration defined earlier in Sect. 1.2 may also be used a building block. By expanding the building block configuration from the monolithic converter topologies, various types of chain-link modular converters can be synthesized as shown in Fig. 2.22. In the chain-link structures, for the same switch and capacitor units, the higher the number of cells, the higher the voltage blocking

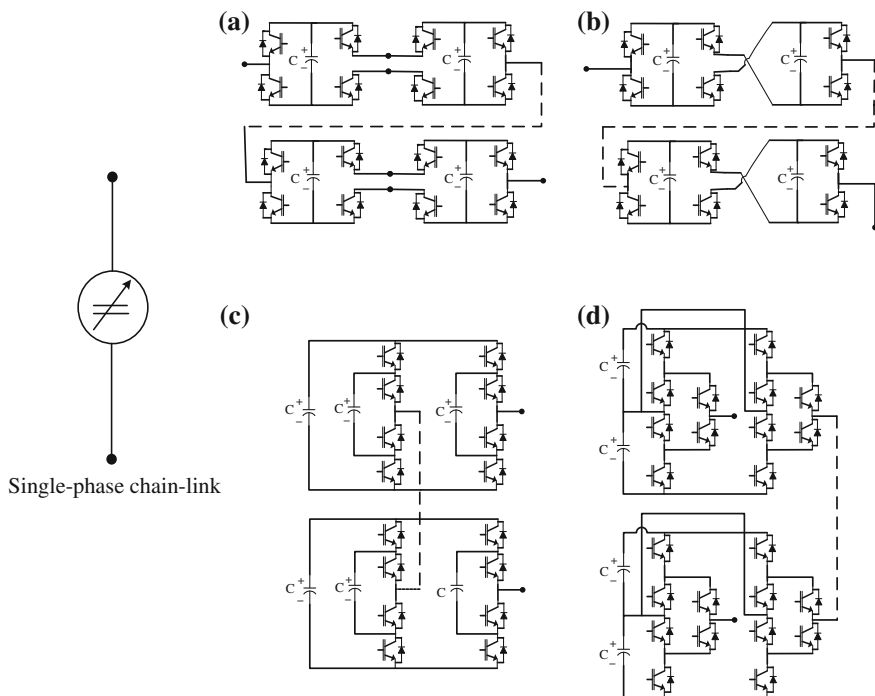


Fig. 2.22 Single-phase chain-link multilevel converter topologies. **a** Series of parallel connected cells. **b** Series of cross connected cells. **c** Stacked commutation cells. **d** Series of NPC commutation cells

capability and the output voltage quality is. The total number of components in the chain-link structure is simply proportional to the number of cells (N). In the chain-link converters, switching frequency of the power devices is reduced by a higher number of cells, while the conduction losses are a function of the number of cells (N) inserted in the conduction path. Therefore, since the chain-link structures bear the same characteristics of their corresponding building blocks, cells with a minimum number of devices are desired to reduce the converter cost and conduction loss in chain-link multilevel converters.

Controlling the floating cell capacitors in the chain-link multilevel converters is one of the main control concerns in such topologies. By changing the switch connection between the intermediate cell capacitors as shown in Fig. 2.22a, the capacitors can be connected in parallel. The parallel connected commutation cells helps the capacitors' voltage ripple reduction. An alternative parallel connection of half-bridge cell capacitors at reduced device current rating is proposed in [51]. The full-bridge cell can be connected in a cross fashion as reported in [52, 53]. The cross connected cell is an alternative symmetrical bipolar cell structure in which by cross connecting more intermediate capacitors in the structure shown in Fig. 2.22b, a higher number of voltage levels can be achieved. This results in reduction of cell

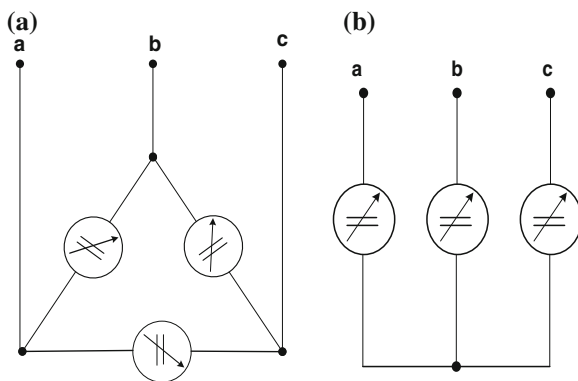
counts and conduction losses while the output quality remains the same as the normal cascaded converters presented in Fig. 2.20. Flying capacitor and neutral point clamped converter can also be utilized as the building block element. By connecting these cells in a nested or series configuration, a single-phase leg structure of the variable VSC can be created as shown in Fig. 2.22c, d. It is worth to mentioning that, the intermediate capacitor voltages should be balanced on the desired DC-voltage value in case of three or more voltage level structure. The chain-link modular multilevel structures in Fig. 2.22, can synthesize a bipolar staircase voltage for high and medium power applications with alternating converter terminal voltages, e.g., STATCOM, matrix converters, etc. For a three-phase system, the output voltage of the three cascaded inverters can be connected in either delta or wye configuration as shown in Fig. 2.23a, b, respectively. Each of these configurations offer various benefits according to the application specifications. The star connection is the most promising as a battery energy storage system (BESS) for positive-sequence active-power control and as a STATCOM for positive-sequence reactive-power control with the lowest converter-cell count. The delta is applicable to a STATCOM for positive- and negative-sequence reactive-power control with $\sqrt{3}$ more current for the same semiconductor as the star connection [54].

The main advantages and disadvantages of the delta connection (Fig. 2.23a) of the chain-link modular multilevel converter topologies for a three-phase systems are as follows:

Advantages

- Modularity of the system is the main advantage of these structures which allows the higher voltage achievement with a minimum mechanical complexity.
- Since each chain-link modular multilevel converter is connected between the lines, a higher current ($\sqrt{3}$ times higher) capability is achieved with the same semiconductor.
- Negative sequence compensation of the delta configuration is achievable by injecting a zero sequence current.

Fig. 2.23 Three-phase chain-link multilevel converter topologies. **a** Delta connection. **b** Star connection



Disadvantages

- Each phase-leg of the delta connection is connected between the line to line network voltages. This increases the required number of series connected cells.
- Current over rating is required for the zero sequence current that exchanges energy between the phases.
- Compensation of unbalance in the network voltages is limited due to restrictions on exchanging energy between the phases during this operational condition.

The main advantages and disadvantages of the star connection (Fig. 2.23b) of the chain-link modular multilevel converter topologies for a three-phase systems are as follows:

Advantages

- Modularity of the system is the main advantage of these structures which allows the higher voltage achievement with a minimum mechanical complexity.
- Since each chain-link modular multilevel converter is connected between the phase network and the neutral, each phase-leg is only subjected to the phase to neutral voltage. This means that theoretically a lower number of series connected cells are required.
- Unbalanced network voltages can be compensated in this structure.

Disadvantages

- For unbalanced loads compensation, a zero sequence voltage must be introduced to exchange energy between the phases. This results in an increased number of series connected cells.
- The required zero sequence voltage increases exponentially when equal amounts of positive and negative sequence compensation are required and this results in a limited compensation capability.

The prominent advantages of modular chain-link multilevel converters in terms of the wider dynamic and greater flexibility, simple mechanical design, maintenance and reliability, low losses make them a suitable choice for different applications such as weak grid support, integration of renewables, industrial steel and mining in order to support heavy loads and flicker mitigation. SVC Light[®] was introduced by ABB in 1997 and improves the efficiency of power transmission systems, increasing the transmission capacity as well as reducing the risk of voltage collapses and blackouts. ABB's latest generation SVC Light is based on a modular, multilevel converter topology to reach even higher transmission efficiency with or without transformer. The new design reduces losses and harmonic emissions and enhances performance, through improved voltage control. Currently, SVC Light[®] offers a power range of 10–250 MVar and is available at different voltage and current rating. Siemens offers the SVC PLUS[®] since 2009 which is the modular multilevel chain-link with the IGBT based full-bridge module. They are also available at different power and voltage ratings. Alstom technology on modular VSC is called MaxSine which is based on power electronic modules.

DC terminals and the AC terminal is connected in the middle of the arms. This topology addresses, low loss, low switching frequency (slightly above the fundamental frequency), voltage scalability due to the simple cascading of identical cells, negligible AC filters due to the synthesized pure sine voltage waveform (for above 20 cells per arm), and mechanical simplicity. Either half- or full-bridge cells can be employed in the converter arms to generate the arm voltage waveforms. In case of the half-bridge cells, each converter arm generates an AC multilevel voltage with a DC offset of the pole-to-ground voltage. This results in a higher converter arm rating (2 times the AC voltage) as they need to provide a DC offset in order to create the output AC voltage. However, when full-bridge cells are used, it is sufficient that each arm generates only the AC voltage with the same amplitude as of the output voltage. Therefore, the number of cells is reduced to half of the one in the half-bridge case while the number of devices in each cell is doubled. A sinusoidal multilevel waveform at the AC terminal is synthesized by devising a proper modulation strategy and creating appropriate insertion indices at each converter arm terminals. One of the other important feature in MMC which can distinguish this topology from the other modular structures, is the lower device current rating due to the AC current sharing between two converter arms and having the circulating current properties. Given the important features of this converter topology, it seems to be an invincible topology for HVDC transmission applications with respect to today's technology. This converter has been developed recently by ABB known as HVDC LightTM [55], by Siemens known as HVDC PLUSTM [56], and known as MaxSine for the Alstom technology. However, various control strategies have been suggested for both MMC and shown the advantages of the high-power MMC-based STATCOM for a full compensation of unbalanced and distorted nonlinear loads [54, 57]. This modular MMC-based STATCOM also introduces a transformerless design. In addition extended version of MMC-based STATCOM was developed in [57] by paralleling a number of MMC to achieve higher efficiency, higher, reliability, lower weight and size, lower switching frequency and lower ratings for the switches. Applying the full-bridge cells instead of the half-bridge cells, the DC and the AC side voltages can be decoupled. Although this requires double the number of switching devices, this is a useful functionality for the renewable sources where the buck or boosting capability of the input voltage is required due to the voltage fluctuation.

Despite all interesting features, this converter suffers from very big a very big capacitor size which is almost ten times greater than the normal monolithic converters. In addition, one of the main challenges in order to control this type of converter is the energy variation balance in each converter arms and different control and capacitor balancing methods have been proposed in literatures [58, 59]. Another critical challenge which corresponds to the high power application requirements is the internal and the external fault tolerance of the converter. Various cell protection schemes and devices have been introduced to deal with internal faults. A device with built-in short circuit failure mode capability or cell bypass switch has been proposed for internal cell faults.

Advantages and disadvantages of the MMC for STATCOM application are as follows:

Advantages

- The system is modular and this allows easy addition of cells for higher phase voltages.
- A DC circulating current can be introduced between the phase legs to facilitate energy exchange under unbalanced conditions for negative sequence compensation. This topology also allows compensation for unbalanced network voltages.
- The line current splits between the two arms of the converter. This means for a constant valve current rating the total output power of the converter is increased.

Disadvantages

- Valve current De-Rating is required due to the DC circulating current added to the required current.
- Each arm of the converter must produce the peak AC output voltage superimposed onto a DC offset. This means the number of cells in the converter is significantly higher than the delta and star chain-link topologies.
- The presence of the DC offset voltage that each arm must create results in a large fundamental frequency component in the arm capacitor voltages. Third harmonic voltage injection does alleviate this issue somewhat, however only by a small fraction (approximately 10 %). The net effect is still an increase in capacitor voltage ripple compared to the delta and star chain-link topologies. This leads to significantly increased amounts of stored energy in the capacitors and hence increased cost for the converter.

To illustrate the MMC operation, a simulation study using MATLAB/Simulink is performed on a three-phase twelve-level MMC. The inverter consists of 12 half-bridge submodules and is connected to the grid and the DC-link voltage is 60 kV. Key MMC waveforms including arm voltage/current and capacitor voltages for 5 MVar inductive (receiving) and capacitive (sending) reactive power modes have been illustrated in Fig. 2.25a, b, respectively. It is evident from Fig. 2.25 that the submodules capacitor voltages attain their target operating values at 5 kV (60 kV/12). As shown, the capacitor ripple in capacitive modes has a higher maximum ripple while in inductive mode capacitors have a higher minimum ripple. This results in an energy requirement of the converter in the inductive mode as the modulation is limited due to the higher minimum ripple. This can be compensated by having a higher DC voltage in each cell capacitor.

2.3.2.2 Modular Multilevel Converter (MMC) with AC Connection

Since, it is not necessary to have DC connection in STATCOM applications, by series connection of the half bridges as shown in Fig. 2.24, a chain-link multilevel converter based on half-bridge cells can be generated. Since the half-bridge has

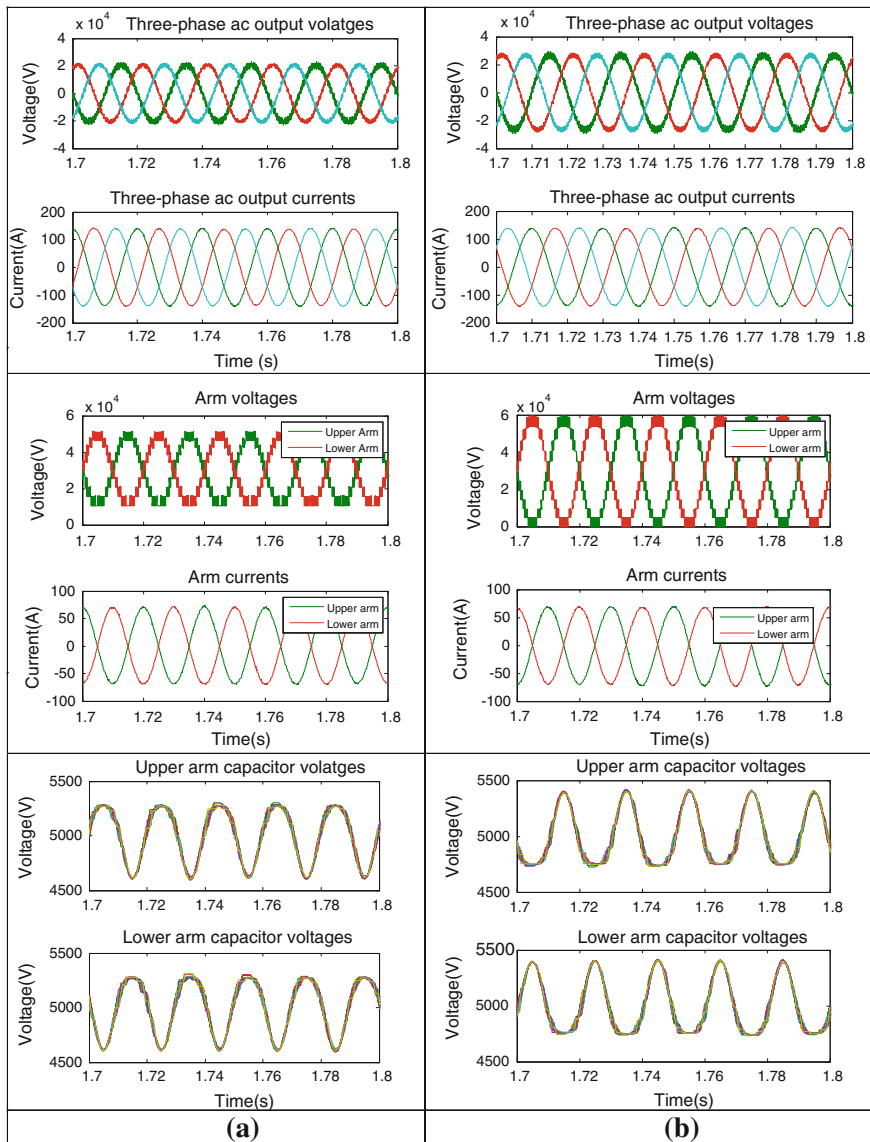


Fig. 2.25 Key MMC waveform with 12 cells in each arm. **a** Inductive mode; **b** capacitive mode

only unipolar output voltage, two sets of series connected half-bridge cells are required for each phase-leg. One set creates positive output voltages while the other creates negative voltages. The corresponding converter schematic is shown in Fig. 2.26. Thus, bipolar multilevel waveform can be generated at the AC output terminal.

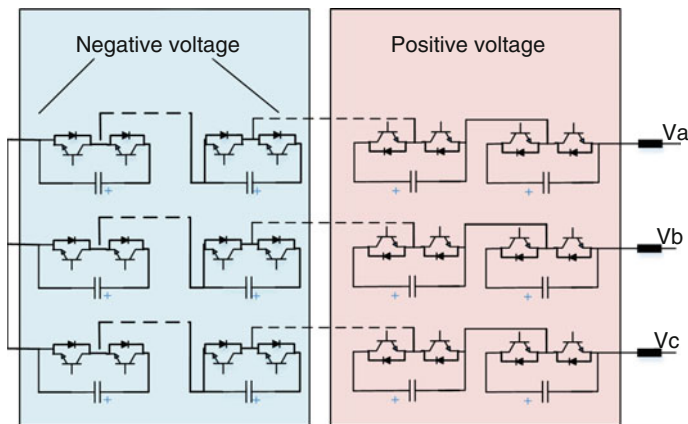


Fig. 2.26 Chain-link multilevel converters with half-bridge cells

Advantage and disadvantages of this topology are as follows:

Advantages

- The system is modular and this allows easy addition of cells for higher phase voltages.
- The system is built based on the half-bridge cells which is very simple and has less mechanics.

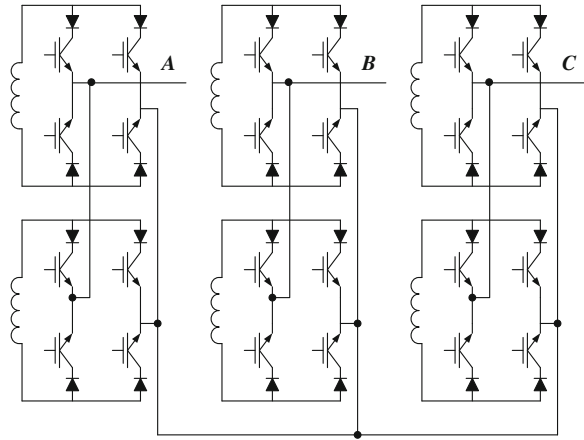
Disadvantages

- A zero sequence voltage should be introduced to exchange energy between the phases when compensating unbalanced loads. This results in an increased number of series connected cells.
- Having two set of half-bridge cells results in a high number of cells in the converter, and hence the stored capacitor energy, is not utilized compared to the chain-link delta star topologies.

2.3.3 Modular Current Source Converters (MCSC)

The modular CSCs are the dual configuration of the modular VSCs and provide a good solution for flexibility with scaling in current. The solution is modular and scales well with standard size building blocks, where the devices and passive components (inductors) have the same rating. The challenge with the MCSC current source-based converter is the ability to scale in voltage and obtaining the isolated direct current sources. Although few researches have focused on the analysis and design of CSC based STATCOM systems, with the advents in high

Fig. 2.27 Dual of series connected CHB-parallel connected CHB current sources



voltage, high power semiconductor technology, such as IGCT and high voltage IGBT technologies, CSC based STATCOM systems at different rate of power can be increasingly used in the near future FACTS applications. The most prominent modular multilevel CSC will be discussed in this section.

2.3.3.1 Modular CSCs Using H-Bridge Cells

The cascaded H-bridge (CHB) current source as a dual to a standard voltage-source based CHB is shown in Fig. 2.27. The topology comprises of single-phase current source cells, either half bridge or full bridge cells, which are the dual of the VSC cell (Fig. 2.4). However, a full-bridge functionality is required to achieve a sinusoidal phase current waveform. As shown, despite of the CHB VSC, cells are connected in parallel to synthesize a stepwise current waveform as the current sources cannot be connected in series. Therefore, this topology is more useful for the application with a high current requirement. Basic operation is analogous to a voltage source based CHB, with the cells being connected per-phase. Using a proper Pulse with modulation strategy such as the phase shifted carrier based method, a multilevel current waveform can be generated at the phase output. As the CHB cells are connected in parallel, each cell is rated for the peak phase-to-neutral alternating voltage, hence, the use of this topology in high voltage applications is challenging. It is noted that the current sharing method (similar to voltage balancing method in VSC) needs to be applied on this topology to ensure the same device current rating. This can be done with the selection algorithm method. For instance, at occasion of switching ON, the cell with lower (higher) current is selected to switch on when the voltage across the chain-link is positive (negative) and vice versa.

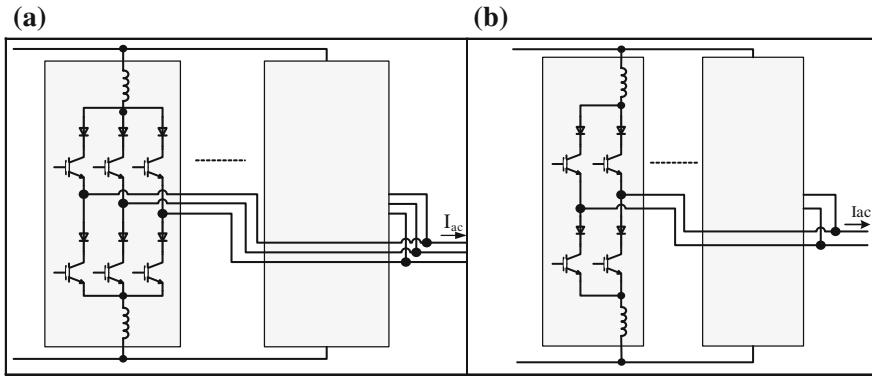


Fig. 2.28 Modular CSCs using cells with a common DC connection, **a** three-phase modular CSC, **b** single-phase modular CSC

2.3.3.2 Modular CSCs Using Cells with Common DC Connection

Because of the nature of current synthesis, a modular multilevel CSC requires current source cells to be connected in parallel. This configuration is the dual of connecting the VSC two or three-phase blocks in series. A three-phase MCSC can be constructed by three single-phase CSCs, or parallel connecting three-phase cells. The conventional modular MCSCs (see Fig. 2.28), that are widely studied in literature [9, 60], consist of parallel-connected full-bridge or three-phase current source cells. The modular CSC topology configuration can also be found by a slight variation to the FCM CSC, described above in Sect. 2.2.2. Figure 2.28a shows a three-phase 5-level example. All inductors conduct the same current level of I_{dc}/N where N is the number of two or three-phases. The DC side of cells is opened, and connected through inductors, which are required to minimize circulating currents between the cells. Same as all modular multilevel structure with the—phase floating energy sources, current balancing strategy is needed to guarantee the device rating. In principle, with a high enough number of cells, each valve can be switched at the fundamental frequency, however the Inductor size is the function of the switching frequency. In order to have a proper design, the optimum switching frequency are chosen to minimize the current ripple. However, using the three-phase CSC block in Fig. 2.28a will result in a lower current ripple compared to the Fig. 2.28b.

2.3.3.3 Current Source M2LC with Half or Full-Bridge Cells

When considering a three-phase current source M2LC, the duality transformations cannot be applied, because a three-phase voltage source M2LC supplying a three-phase load is not a planar structure. One way to construct a three-phase current source M2LC has been discussed in [61], and shown below in Fig. 2.29. This topology copies the higher level circuit structure of the three-phase voltage source

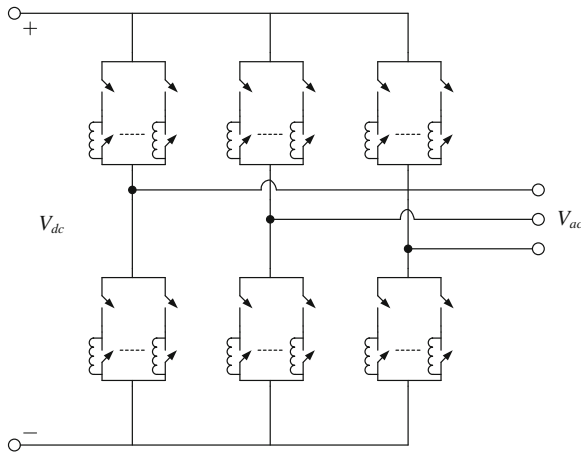


Fig. 2.29 Current source modular multilevel converter–unidirectional cells

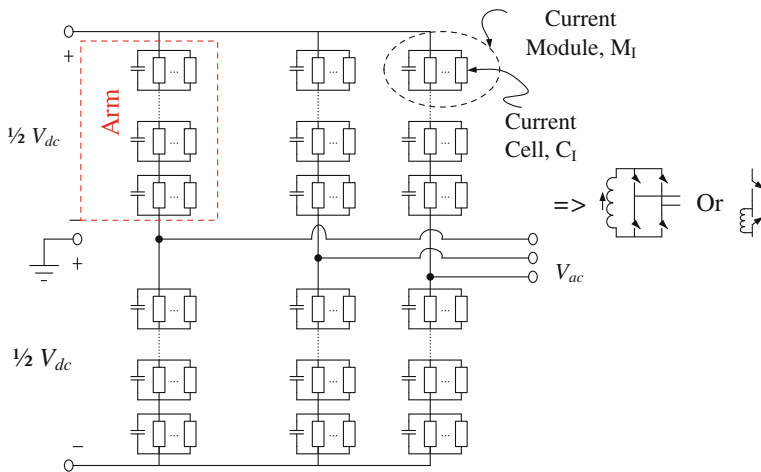


Fig. 2.30 Current source dual of M2LC-configuration to reach a high voltage

M2LC, and thus the operation of this current source M2LC also somewhat copies that of the voltage source M2LC. Each arm in the current source M2LC is a dual circuit of the arm in a voltage source M2LC which has been constructed by parallel connection of either unidirectional (half-bridge), bidirectional (full-bridge), or a mixed. Other types of current source cells may also be used in the current source arm. Each phase consists of two current source arms connecting to the positive and negative poles. When half-bridge cells are used (Fig. 2.29), the current source arm current must be unidirectional, and thus the voltage across each current source arm must be bipolar to ensure zero average arm power.

The current source M2LC can scale in voltage at the arm level. The voltage scaling principle is dual to the current scaling of voltage source M2LC arm. Using

the series-connected current source parallel links as a phase arm, Fig. 2.30 shows a current source MMC topology using half-bridge or full-bridge inductor cells. A capacitor is connected in parallel to each current module to ensure steady-state and dynamic voltage sharing between the series connected current modules. These capacitors are also essential for the series connection of current modules, because all current modules behave as current sources, and their instantaneous currents can never be guaranteed identical in reality. To reach the system voltage level, series-connected current modules are required for each arm. The parallel capacitor voltage should typically have both DC and AC components, which can be actively controlled through the current source parallel links to ensure dynamic voltage sharing. The DC and AC component of the capacitor voltage may be regulated by controlling the DC component and the phase angle of the AC component of the parallel link current, respectively. Having the DC terminals, this converter can be used for either HVDC or FACTS applications. Also, same as the VSC type, using the H-bridge cells can reduce the number of cell in this structure. The main advantages of this topology compared to other modular multilevel CSC are the modularity, scalability to the higher voltage, and the lower voltage rating. Therefore, this topology is more suitable for the high voltage and high current FACTS applications. Due to its scalability, it is possible to remove the transformer for the higher voltage application and thus reduce the extra volume and weight of the system.

2.4 Future Trends in Multilevel Converter Topologies

The evolution of multilevel converters over the last two decades has advanced several commercial applications such as flexible alternating current transmission systems (FACTS). From this technology, as summarized in this chapter, some insight on future trends can be extracted. In addition, despite industrial presence, the technology has not stabilized yet and there are still several challenges for further development of this technology. Some of these trends and challenges are discussed in this section.

The role of the next generation power converter topology becomes significantly important to reduce the total energy consumption by processing the power in electrical transmission systems. The average device switching frequencies are below 300 Hz (for IGBTs and IGCTs) for high power applications. The main reasons for this choice are the device limits, and practical limitations on the cooling system. The switching loss is important in terms of low order harmonics reduction and can be improved by the modulation technique, however, the conduction loss would become dominant, and once the topology is chosen, not much can be done to lower it. Therefore, a trend is to achieve the efficiency of line-commutated thyristor valves converter topologies while gaining valuable insights and overcoming the challenges of the newer topologies.

Reliability and availability at lowered cost is also a key trend in the future development of multilevel converters for high power applications [62].

One important application could be better utilization of the modular building blocks to limit the critical faults in power systems. As discussed earlier in this paper, some multilevel converter topologies have capability to operate under DC fault conditions. The fault detection methods are of vital importance for this ability. As addressed, bipolar cell structures and converter reconfigurations are definitely challenges for further research and development in this field. Another trend to have fault tolerant converters is to move toward the modular current source converters or hybrid VSC/CSC topologies.

Price trends reveals that semiconductors are becoming cheaper while energy is becoming more expensive, and grid codes are becoming more restrictive [63, 64]. Therefore, the use of modular multilevel converters becomes more and more attractive for high power applications, as the long-term operational cost reduction justifies the higher initial costs. The existing and future grid codes and the continued increase of power demand of various applications will be the central focus in modular multilevel converter development. The reduction of the required energy stored in the passive components is highly important. Moreover, the energy consumption in power converters should be minimized [64]. These necessities motivate the trends towards designing building block cells with more functionalities or creating modular converters with paralleled phases.

Currently, the dominating semiconductor technology for high power modular multilevel topologies is the IGBT. This approach has been very successful in modular multilevel topologies due to the low switching frequency, and is expected to exist in the upcoming years in high power application fields. On the other hand, the development of mature wide band gap devices such as silicon carbide (SiC), Gallium Nitride (GaN), and diamond power devices would benefit the establishment of multilevel converters, by drastically reducing the switching losses and minimizing the cooling system requirement [65]. Therefore, it is expected that, in the future, high-voltage SiC devices would affect the building block cells and accordingly modular multilevel topologies for high power applications [66]. This needs to be further evaluated with a proper modeling of the device and considering practical issues in high voltage applications [67].

Modular multilevel converters used for high power applications contain a large number of semiconductors, capacitors and inductors within their structures, which increases the size and weight of these converter topologies [68]. For some applications such as offshore wind, it is vital to have a compact converter topology.

Although transformers provide galvanic isolation and voltage matching in grid connected high power applications, a transformerless topology is still a desirable feature. The elimination of transformers provides a significant reduction in the cost, volume, and weight, system complexity and losses. An alternative solution to further increase the functionality and efficiency of the grid, is to replace the conventional passive transformers by solid-state transformers. This concept also encounters different challenges, such as very high switching loss when using the silicon devices and special considerations required to both core and winding losses, especially for high power applications [69].

References

1. Rodriguez J, Lai JS, Peng FZ (2002) Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Trans Ind Electron* 49(4):724–738
2. Rodriguez J, Franquelo LG, Kouro S, Leon JI, Portillo RC, Prats MAM, Perez MA (2009) Multilevel inverters: an enabling technology for high-power applications. *Proc IEEE* 97(11):1786–1817
3. Abu-Rub H et al (2010) Medium-voltage multilevel converters—state of the art, challenges, and requirements in industrial applications. *IEEE Trans Indust Electron* 57(8):2581–2596
4. Kouro S et al (2010) Recent advances and industrial applications of multilevel converters. *IEEE Trans Indust Electron* 57(8):2553–2580
5. Soto D, Green C (2002) A comparison of high-power converter topologies for the implementation of facts controllers. *IEEE Trans Indust Electron* 49(5):1072–1080
6. Liang J et al (2013) Current source modular multilevel converter for HVDC and FACTS. In: *Proceedings of IEEE 15th European conference on power electronics and applications (EPE)*
7. Shen D, Lehn PW (2002) Modelling, analysis and control of a current source inverter-based statcom. *IEEE Trans Power Delivery* 17(1):248–253
8. Ye Y, Kazerani M, Quintana VH (2005) Current-source converter based statcom: modeling and control. *IEEE Trans Power Delivery* 20(2):795–800
9. Bai Z, Zhang Z (2008) Conformation of multilevel current source converter topologies using the duality principle. *IEEE Trans Power Electron* 23(5):2260–2267
10. Rohner S et al (2010) Modulation, losses, and semiconductor requirements of modular multilevel converters. *Ind Electron IEEE Trans* 57(8):2633–2642
11. Akagi H (2011) Classification, terminology, and application of the modular multilevel cascade converter (MMCC). *Power Electron IEEE Trans* 26(11):3119–3130
12. Ghosh A, Ledwich G (2002) *Power quality enhancement using custom power devices*. Kluwer, Norwell
13. Gyugyi L, Schauder C (1994) US Patent, 5,343,139, 30 August 1994
14. Schauder C et al (1997) Operation of ± 100 MVAR TVA StatCom. *IEEE Trans Power Delivery* 12(4), October 1997
15. Schauder C et al (1998) AEP UPFC project: installation, commissioning and operation of the ± 160 MVA STATCOM (phase I). *IEEE Trans Power Delivery* 13(4), October 1998
16. Peng FZ, Lai JS, McKeever JW, VanCoevering J (1996) A multilevel voltage-source inverter with separate DC sources for static var generation. *IEEE Trans Ind Applicat* 32:1130–1138
17. Kazmierkowski MP, Malesani L (1998) Current control techniques for three-phase voltage-source PWM converters: a survey. *IEEE Trans Ind Electron* 45(5):691–703
18. Shukla A, Ghosh A, Joshi A (2005) Static shunt and series compensation of an smib system using flying capacitor multilevel inverter. *IEEE Trans Power Delivery* 20(4):2613–2622
19. Shukla A, Ghosh A, Joshi A (2007) Hysteresis current control operation of flying capacitor multilevel inverter and its application in shunt compensation of distribution systems. *IEEE Trans Power Delivery* 22(1):396–405
20. Shukla A, Ghosh A, Joshi A (2007) State feedback control of multilevel inverters for dstatcom applications. *IEEE Trans Power Delivery* 22(4):2409–2418
21. Shukla A, Ghosh A, Joshi A (2008) Control schemes for DC capacitor voltages equalization in diode-clamped multilevel inverter based DSTATCOM. *IEEE Trans Power Delivery* 23(2):1139–1149
22. Saedifard M, Bakhshai AR, Jain P (2003) An active power filter implemented with a 3-level NPC converter in conjunction with the classification technique. *Proc IEEE CCECE* 1:503–507
23. Ertl H, Kolar JW, Zach FC (2002) A novel multi-cell DC-ac converter for applications in renewable energy systems. *IEEE Trans Ind Electron* 49(5):1048–1057
24. Flourentzou N, Agelidis V, Demetriades GD (2009) VSC-based HVDC power transmission systems: an overview. *IEEE Trans Power Electron* 24(3):592–602

25. Baker RH, Bannister LH (1975) Electric power converter. US Patent 3,867,643, February 1975
26. Nabae A, Takahashi I, Akagi H (1981) A new neutral-point clamped PWM inverter. *IEEE Trans Ind Applicat* IA-17:518–523
27. Rodriguez J, Bernet S, Steimer PK, Lizama IE (2010) A survey on neutral-point-clamped inverters. *IEEE Trans Ind Electron* 57(7):2219–2230
28. Steimer PK, Apeldoorn O, Ødegård B (2005) Very high power PEBB technology. In: *Proceedings of IEEE EPE*
29. Brückner T, Bernet S (2001) Loss balancing in three-level voltage source inverters applying active NPC switches. In: *Proceedings of IEEE power electronics special conference, Vancouver*, pp 1135–1140
30. Brückner T, Bernet S (2001) Loss balancing in three-level voltage source inverters applying active NPC switches. In: *Proceedings of IEEE-PESC, Vancouver*, pp 1135–1140
31. Marchesoni M, Tenca P (2001) Theoretical and practical limits in multilevel MPC inverters with passive front ends. In: *Proceedings of EPE'01, Graz* pp 27–29, August 2001
32. Shukla A, Shukla A, Joshi A (2012) Control of dc capacitor voltages in diode-clamped multilevel inverter using bidirectional buck–boost choppers. *IET Power Electron* 5 (9):1723–1732
33. Ishida T, Matsuse K, Sugita K, Huang L, Sasagawa K (2000) DC voltage control strategy for a five-level converter. *IEEE Tran Power Electron* 15(3):508–515
34. Shukla A, Shukla A, Joshi A (2010) Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter. *Ind Electron IEEE Trans* 57 (7):2249–2261
35. Yuan X, Barbi I (2000) Fundamentals of a new diode clamping multilevel inverter. *Power Electron IEEE Trans* 15(4):711–718
36. Ye Y, Kazerani M, Quintana VH (2005) Current-source converter based STATCOM: modeling and control. *IEEE Tran Power Del* 20(2):795–800
37. Meynard TA, Foch H (1992) Multi-level conversion: high voltage choppers and voltage-source inverters. In: *IEEE power electronics specialists conference*, pp 397–403
38. Yuan X, Stemmler H, Barbi I (2001) Self balancing of clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under subharmonic PWM modulation. *IEEE Trans Power Electron* 16(2):256–263
39. Wilkinson RH, Meynard TA, Mouton HDT (2006) Natural balance of multicell converters: the general case. *IEEE Trans Power Electron* 21(6):1658–1666
40. Shukla A, Ghosh A, Joshi A (2011) Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM. *Power Electron IEEE Trans* 26(6):1682–1693
41. Shukla A, Ghosh A, Joshi A (2008) Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter. *Power Electron IEEE Trans* 23(2):518–529
42. Meynard TA, Foch H, Thomas P, Caurault J, Jacob R, Nahrstaedt M (2002) Multicell converter: basic concepts and industry applications. *IEEE Trans Ind Electron* 49(5):955–964
43. Fuji K, Schwarger U, Doncker RWD (2005) Comparison of hard-switched multi-level inverter topologies for statcom by loss- implemented simulation and cost estimation. In: *Proceedings IEEE PESC*, pp 340–346
44. Lesnicar A, Marquardt R (2003) An innovative modular multilevel converter topology suitable for a wide power range. In: *Proceedings of IEEE power tech conference, Bologna*, vol 3, 6p
45. Hochwald W, Kleiner TC (1977) Distribution system for ac electrical energy derived from dc energy sources. US Patent No 4,052,657, 4 October 1977
46. Marchesoni M, Mazzucchelli M, Tenconi S (1988) A non conventional power converter for plasma stabilization. In: *IEEE power electronics specialists conference*, vol 1, pp 122–129
47. Peng FZ, Lai JS, McKeever JW, VanCoevering J (1996) A multilevel voltage-source inverter with separate DC sources for static var generation. *IEEE Trans Ind Appl* 32(5):1130–1138

48. Tolbert Leon M, Peng Fang Z, Cunyngham Tim, Chiasson John N (2002) Charge balance control schemes for multilevel converter in hybrid electric vehicles. *IEEE Trans Ind Electron* 49(5):1058–1065
49. Manjrekar MD, Lipo TA (1998) A hybrid multilevel inverter topology for drive applications. In: *IEEE applied power electronics conference*, pp 523–529
50. Malinowski M et al (2010) A survey on cascaded multilevel inverters. *Ind Electron IEEE Trans* 57(7):2197–2206
51. Ilves K, Taffner F, Norrga S, Antonopoulos A, Harnfors L, Nee HP (2013) A submodule implementation for parallel connection of capacitors in modular multilevel converters. In: *Proceedings 15th European conference on power electronics and applications (EPE), Lille*
52. Nami A, Wang L, Dijkhuizen F, Shukla A (2013) Five level cross connected cell for cascaded converters. In: *Proceedings EPE 2013 ECCE Europe, Lille, 3–5 September 2013*
53. Chaudhuri T (2008) Cross connected multilevel voltage source inverter topologies for medium voltage applications. PhD thesis, EPFL
54. Akagi H (2011) Classification, terminology, and application of the modular multilevel cascade converter (MMCC). *IEEE Trans Power Electron* 26(11):3119–3130
55. Jacobson B, Karlsson P, Asplund G, Harnfors L, Jonsson T (2010) VSC-HVDC transmission with cascaded two-level converters. In: *CIGRE*, pp B4–B110
56. Friedrich K (2010) Modern HVDC PLUS application of VSC in modular multilevel converter topology. In *Proceedings of IEEE international symposium on industrial electronics (ISIE)*, pp 3807–3810
57. Mohammadi HP, Bina MT (2011) A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters. *IEEE Trans Power Electron* 26:1534–1545
58. Hagiwara M, Akagi H (2008) PWM control and experiment of modular multilevel converters. In: *IEEE power electronics specialists conference, PESC*, pp 154–161
59. Ångquist L, Antonopoulos A, Siemaszko D, Ilves K, Vasiladiotis M, Nee HP (2011) Open-loop control of modular multilevel converters using estimation of stored energy. *IEEE Trans Ind Appl* 47:2516–2524
60. Antunes FLM, Braga HAC, Barbi I (1999) Application of a generalized current multilevel cell to current-source inverters. *IEEE Trans Ind Electron* 46(1):31–38
61. Liang J, Nami A, Dijkhuizen F, Tenca P, Sastry J (2013) Current source modular multilevel converter for HVDC and FACTS. In: *Proceedings of EPE 2013 ECCE Europe, Lille, 3–5 September 2013*
62. van Wyk JD, Lee FC (2013) On a future for power electronics. *IEEE J Emerg Sel Top Power Electron* 1(2):59–72
63. Boroyevich D, Cvetkovic I, Burgos R, Dong D (2013) Intergrid: a future electronic energy network?. *IEEE J Emerg Sel Top Power Electron* 1(3):127–138
64. Popović-Gerber J, Oliver J, Cordero N, Harder T, Cobos JA, Hayes M, O'Mathuna S, Prem E (2012) Power electronics enabling efficient energy usage: energy savings potential and technological challenges. *IEEE Trans Power Electron* 27(5):2338–2353
65. Pefitsis D, Tolstoy G, Antonopoulos A, Rabkowski J, Lim J, Bakowski M, Ångquist L, Nee H (2012) High-Power modular multilevel converters with SiC JFETs. *IEEE Trans Power Electron* 27(1):28–36
66. Hudgins JL (2013) Power electronic devices in the future. *IEEE J Emerg Sel Top Power Electron* 1(1):11–17
67. Gong X, Josifović I, Ferreira JA (2013) Modeling and reduction of conducted EMI of inverters with SiC JFETs on insulated metal substrate. *IEEE Trans Power Electron* 28(7):3138–3146
68. Blaabjerg F, Ma K (2013) Future on power electronics for wind turbine systems. *IEEE J Emerg Sel Top Power Electron* 1(3):139–152
69. Kassakian JG, Jahns TM (2013) Evolving and emerging applications of power electronics in systems. *IEEE J Emerg Sel Top Power Electron* 1(2):47–58

<http://www.springer.com/978-981-287-280-7>

Static Compensators (STATCOMs) in Power Systems

Shahnia, F.; Rajakaruna, S.; Ghosh, A. (Eds.)

2015, XXI, 735 p. 394 illus., 128 illus. in color.,

Hardcover

ISBN: 978-981-287-280-7