

Chapter 2

Transformer Design and Characterization in CMOS Process

2.1 Background

On-chip inductors have become essential in RF system-on-chip design and integration. As compared with off-chip inductors on the printed circuit board (PCB) or bondwire inductors, the use of on-chip inductors prevents degradation of circuit performance due to the loss and the parasitics from the chip interface. Moreover, high-level integration with on-chip inductors can not only significantly reduce the cost and the form factor but also improve the reliability of the whole wireless systems.

Unfortunately, on-chip inductors suffer from a low quality factor Q , which would result in performance degradation in terms of noise, gain, and power consumption. As a consequence, modern RF CMOS processes provide one or two thick top metal layers far above the lossy substrate to improve the quality factor Q and the self-resonant frequency of the on-chip inductors [1, 2]. In addition, due to its relatively narrowband characteristics, on-chip inductors may not be suitable for wideband applications, such as multiband, multimode, or software-defined radios.

As potential replacement and improvement of on-chip inductors, integrated transformers have recently been considered and widely used in wideband RF and mm-Wave circuits and systems. Their main applications include (1) impedance transformation in the impedance matching network, (2) amplification for voltage or current signal, (3) balun for on-chip single-ended to differential or differential to single-ended signal transformation, and (4) high-order resonant tank to obtain either multiple narrowband or wideband frequency response of amplitude and phase for many circuits, including LNAs, VCOs, frequency dividers, frequency multipliers, etc.

Figure 2.1a shows the schematic symbol of an ideal $N:1$ transformer, where $N = V_1/V_2$ is defined as the turn ratio between the primary coil and the secondary coil. Since an ideal transformer is passive and no energy losses occur during the voltage and current transformation, the current ratio I_2/I_1 equals to $-N$. As a result,

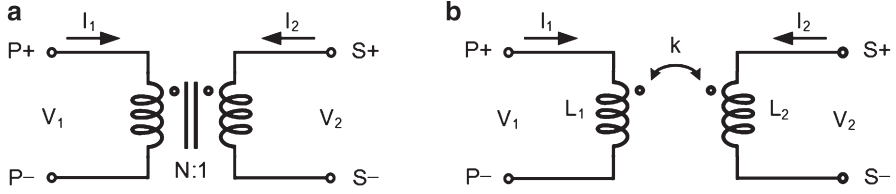


Fig. 2.1 Schematic symbol of (a) an ideal $N : 1$ transformer and (b) a transformer made of two coupled inductors

the impedance seen from the primary coil becomes N^2 times of the loading impedance of the secondary coil.

Figure 2.1b shows a transformer made of two coupled inductors. From the Faraday's law of induction, the induced voltage at either coil equals to the rate of change of the total magnetic flux going through it:

$$V_1 = -\frac{d(\Phi_{11} + \Phi_{21})}{dt} = \left(-\frac{d\Phi_{11}}{dI_1}\right) \cdot \frac{dI_1}{dt} + \left(-\frac{d\Phi_{21}}{dI_2}\right) \cdot \frac{dI_2}{dt} \quad (2.1a)$$

$$V_2 = -\frac{d(\Phi_{22} + \Phi_{12})}{dt} = \left(-\frac{d\Phi_{22}}{dI_2}\right) \cdot \frac{dI_2}{dt} + \left(-\frac{d\Phi_{12}}{dI_1}\right) \cdot \frac{dI_1}{dt} \quad (2.1b)$$

where Φ_{11} (Φ_{22}) is the magnetic fluxes in the primary (secondary) coil generated by the current I_1 (I_2) in itself and Φ_{21} (Φ_{12}) is the magnetic fluxes in the secondary (primary) coil generated by the current I_2 (I_1) in its neighboring coil. By defining the self-inductance as $L_1 = -(\frac{d\Phi_{11}}{dI_1})$, $L_2 = -(\frac{d\Phi_{22}}{dI_2})$, the mutual inductance as $M = -(\frac{d\Phi_{12}}{dI_1}) = -(\frac{d\Phi_{21}}{dI_2})$, and applying Laplace transformation to (2.1a) and (2.1b), V-I equations of the ideal transformer can then be expressed as

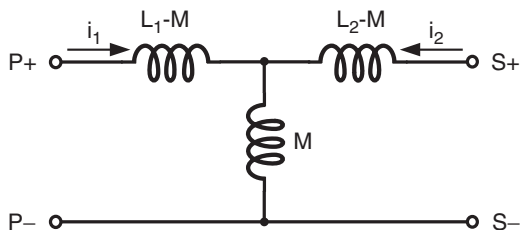
$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} sL_1 & sM \\ sM & sL_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2.2)$$

In the circuit analysis, the T-model as shown in Fig. 2.2 is typically employed to represent the transformer made of coupled inductors as shown in Fig. 2.1b, which can also be easily shown to be equivalent to (2.2). To represent the coupling strength between the two coupled inductors, the magnetic coupling coefficient k defined as the ratio between mutual inductance and self-inductance can be used as below:

$$k \equiv \frac{M}{\sqrt{L_1 L_2}} \quad (2.3)$$

According to the definition, k is an indicator of the coupling strength between the primary and secondary coils. For ideal transformers, there is no leakage of magnetic flux, and the coupling coefficient is unity. However, due to the poor confinement of

Fig. 2.2 T-model of the transformer



magnetic flux in integrated transformers, the coupling coefficient is always substantially smaller than one [3].

Figure 2.3 shows another equivalent circuit model of the transformer that employs an ideal transformer. Here, the ideal transformer with a turn ratio $N = M/L_2 = k\sqrt{L_1/L_2}$ and the inductance k^2L_1 represents the coupling effect between primary and secondary coils, while the inductance $(1-k^2)L_1$ models the leakage flux that does not contribute the magnetic coupling. It is easily proved that the equivalent model as shown in Fig. 2.3 is mathematically the same as the T-model. As shown in the following chapters, the proper choice of the equivalent models can facilitate the circuit calculation.

It is worthwhile to note the meaning of the dots in the transformer symbols in Fig. 2.1. Assuming k is always positive, the dots should be denoted in such a way that when the currents are sent into the dotted terminals from both the primary and secondary coils, the generated magnetic fluxes from both coils should go in the same direction which reinforce each other [4]. Figure 2.4 shows the example to determine the dot location based on this convention.

2.2 Transformer Layout

The common ways to realize integrated transformers are illustrated in Figs. 2.5, 2.6, and 2.7, which offer different tradeoffs on self-inductances, magnetic coupling coefficient, inter-coil and coil-to-substrate capacitances, self-resonant frequencies, and chip area [5]. Here, all the layouts are based on the differential configurations since they are commonly used in VCOs and frequency dividers with balanced differential outputs.

Figure 2.5 shows an interleaved transformer layout. Both the primary and secondary coils are implemented with the same metal layer. As for on-chip inductor design considerations [2], the thick top metal layer is typically used for maximum quality factor Q and high self-resonant frequency because it has much smaller square resistance than other metal layers and far away from the low resistance substrate in CMOS process. When the metal traces need to be crossed over, the lower metal layer can be used as a bridge. Since the interleaved configuration allows large common periphery between the primary and secondary coils, it can

Fig. 2.3 Equivalent circuit model of the transformer

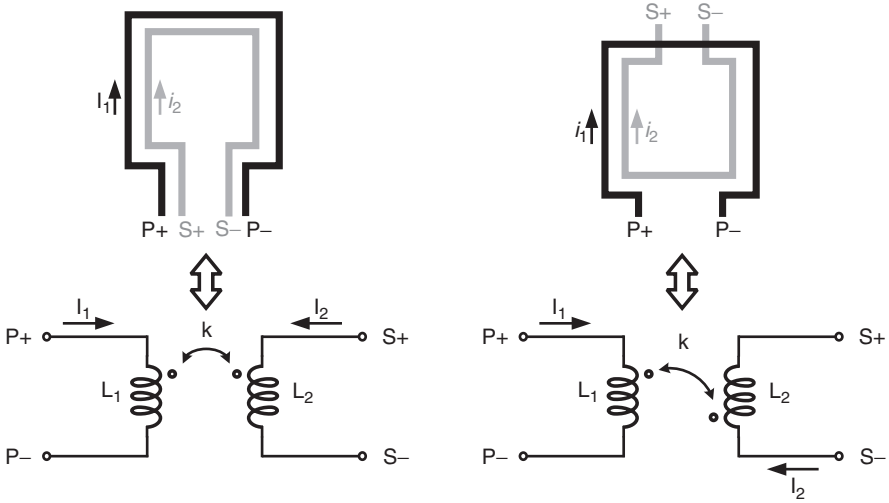
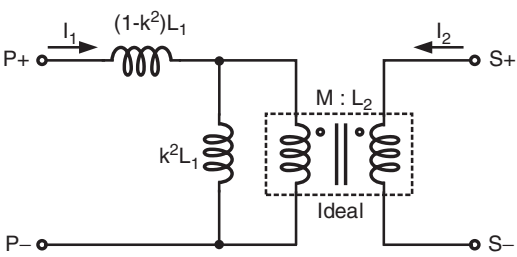


Fig. 2.4 Transformers with different coupling directions and their corresponding schematic symbol using the dot convention

Fig. 2.5 Layout of an interleaved transformer

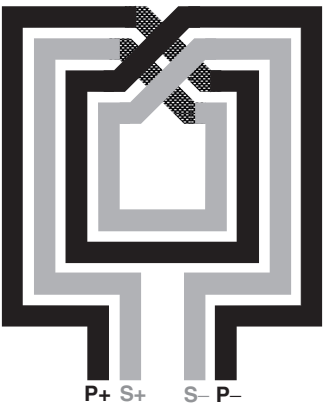


Fig. 2.6 Layout of a tapped transformer

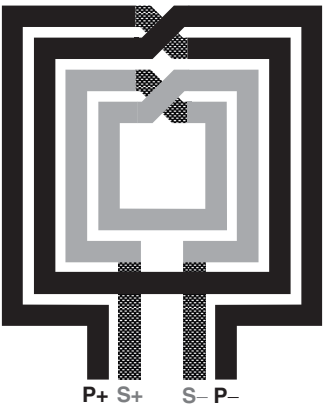


Fig. 2.7 Layout of a stacked transformer: (a) top view and (b) cross-section view

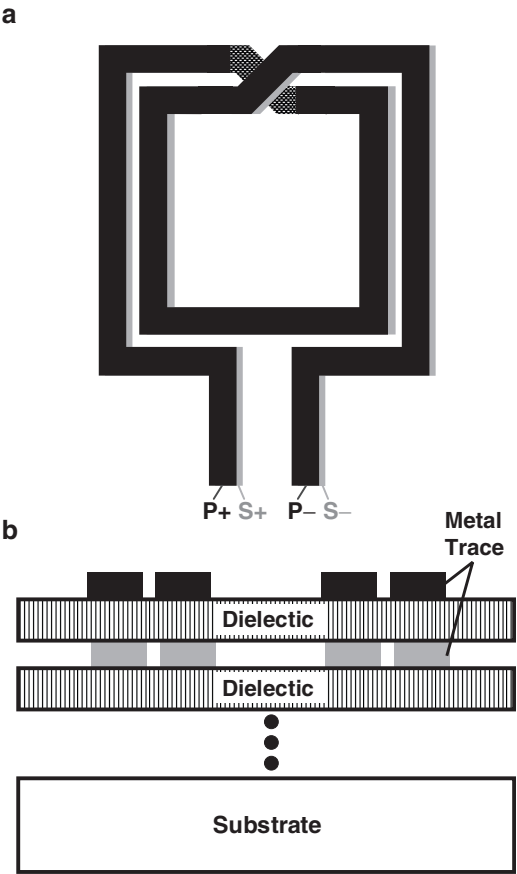


Table 2.1 Comparison of different types of integrated transformer

Transformer structure	k	Self-inductance	Area	Self-resonant frequency
Interleaved	>0.7	Medium	Medium	Medium
Tapped	$0.3\text{--}0.7$	Low	Large	High
Stacked	~ 0.9	High	Small	Low

provide a relatively high coupling coefficient of above 0.7 at the expense of increased inter-coil capacitance and reduced self-inductance since the neighboring metal traces in the same coil are separated by the metal trace from the other coil.

In a taped transformer, both the coils are also implemented in the top metal layer shown in Fig. 2.6. Since the two coils are completely separated, the self-inductance is maximized and the inter-coil capacitance is minimized. However, because only a single turn in the two coils share the common periphery, the coupling coefficient k becomes lower than that of the interleaved configuration. Depending on the space between the two coils, the typical k of the taped transformer can vary from 0.3 to 0.7. Furthermore, the spatial separation of the two coils also results in larger chip area.

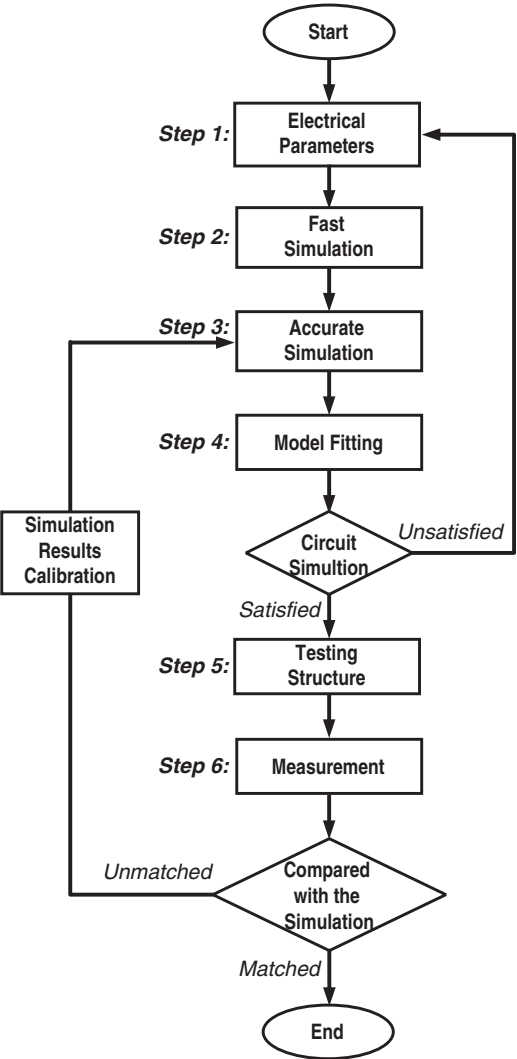
Figure 2.7 shows a stacked transformer layout, in which the primary and secondary coils are implemented in different metal layers. Both vertical and lateral magnetic coupling are utilized to maximize the self-inductance and thus achieve the best area efficiency. Since the dielectric thickness is much smaller than the minimal space between the two neighboring top metal traces, the magnetic coupling is enhanced compared with that of the interleaved configuration. As an example, in a 65-nm CMOS process, the dielectric thickness is smaller than $1\text{ }\mu\text{m}$, while the minimal space of the top metal is around $2\text{ }\mu\text{m}$. Consequently, the coupling coefficient can be close to 0.9 if the metal traces in different layers are perfectly aligned. On the other hand, the inter-coil capacitance increases due to the reduced space between the two coils. In addition, the capacitance from the secondary coil to the substrate also increases since it is implemented in the lower metal layer closer to the substrate. It follows that stacked transformers usually have the lowest self-resonant frequency. The performances of different types of integrated transformers are summarized and compared in Table 2.1.

2.3 Transformer Measurement and Characterization

Basic considerations and guidelines for design, simulation, layout, and characterization of integrated transformers are mostly the same as those for on-chip inductors, which have been well described in many references [2, 3] and will not be repeated here. In the following section, only critical differences unique for integrated transformers are summarized and highlighted.

As illustrated in Fig. 2.8, a typical design and characterization flow of integrated transformers is summarized as below:

Fig. 2.8 Design and characterization flow of integrated transformers



Step 1: Obtain the required electrical parameters of the transformer such as self-inductance, quality factor, and coupling coefficient from either calculation or simulation of the targeted transformer using equivalent circuit models.

Step 2: At the beginning, the physical parameters of the transformer can be quickly estimated and optimized for a given transformer structure by using a fast simulator such as ASITIC [6]. In the optimization, different layout configurations can be considered, from which the physical parameters such as the number of turns, the diameter, metal width, and metal space can be adjusted. Since fast simulators usually overestimate the quality factor Q , the relative trend of the quality factor from different parameter combinations is more useful than its absolute value as a quick reference for optimization.

Step 3: After obtaining the physical parameters from a fast simulation, the transformer can be further simulated by using more accurate electromagnetic (EM) simulator such as the ADS Momentum [7] or HFSS [8]. Usually the simulation results are in the formats of S parameters. To compare with the design goals, the simulated S-parameter data need to be converted into the Z-parameters using the following equations [9]:

$$Z_{11} = Z_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad (2.4a)$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad (2.4b)$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad (2.4c)$$

$$Z_{22} = Z_0 \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad (2.4d)$$

where Z_0 is impedance of the ports used in the simulation. With the Z-parameters, the following equations can be employed to obtain the electrical parameters of the transformer:

$$L_1 = \frac{\text{Im}(Z_{11})}{\omega} \quad \text{and} \quad L_2 = \frac{\text{Im}(Z_{22})}{\omega} \quad (2.5a)$$

$$Q_1 = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \quad \text{and} \quad Q_2 = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})} \quad (2.5b)$$

$$k = \frac{\text{Im}(Z_{21})}{\sqrt{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \quad (2.5c)$$

where $\omega = 2\pi f$. At this stage, the physical parameters can be further fine-tuned to obtain the optimized design that can best satisfy the requirements.

Step 4: After the physical parameters of the transformer are fixed, the lumped model as shown in Fig. 2.9 can be used for circuit simulation. This lumped model is based on the wideband inductor model from [10], which merges the π models from [11] and [12] and the substrate-coupled model from [13]. Here, the self-inductance and the ohmic loss are modeled by components L_1/L_2 and r_1/r_2 , while the parasitic capacitance and the resistive loss of the substrate are modeled by $C_{\text{ox}1}/C_{\text{ox}2}$, $C_{\text{sub}1}/C_{\text{sub}2}$, and $R_{\text{sub}1}/R_{\text{sub}2}$. The magnetic coupling and capacitive coupling between the two coils are modeled by k and C_c , respectively, and the capacitive coupling between the metal traces in the same coil is modeled by C_{m1}/C_{m2} . The substrate-coupled network made of $L_{\text{ed}1}/L_{\text{ed}2}$ and $R_{\text{ed}1}/R_{\text{ed}2}$ models the substrate losses due to the eddy current which is increased with frequency. The model parameters are extracted from and fitted to the simulated S-parameter data by using optimizer and fitting tools. Simulations can be used to ensure that the frequency response of the

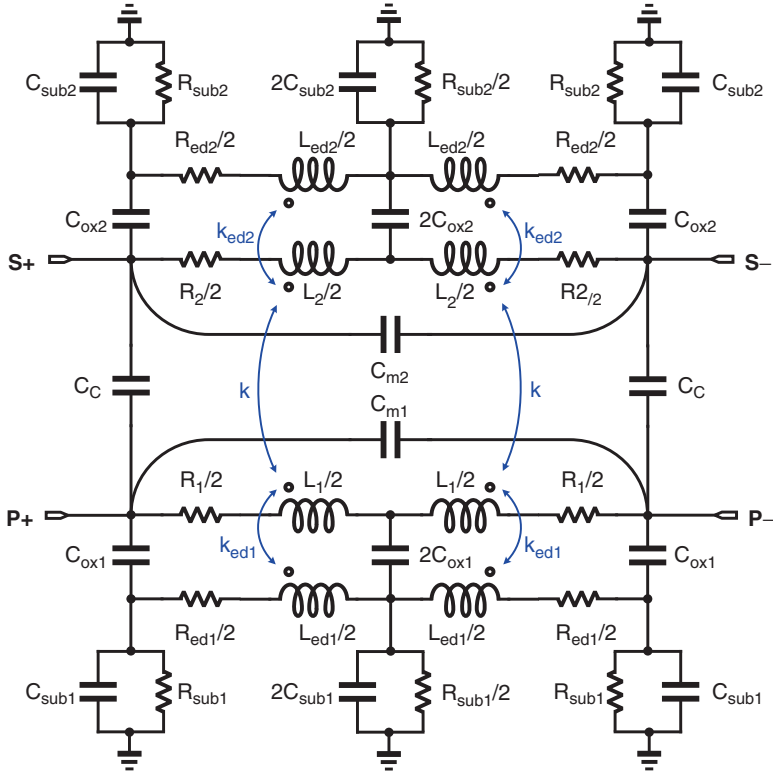


Fig. 2.9 A wideband transformer model for parameter extraction and circuit simulation

model can match well the EM simulation results over a wide frequency range. The transformer model can then be directly used in the time-domain or frequency-domain transistor-level simulation, which enables complete evaluation of the circuit performance. In practice, several iterations with the whole procedure repeated may be necessary to fine-tune the physical and electrical parameters of the transformers until the circuit specifications are satisfactorily met.

Step 5: The transformer testing structure as shown in Fig. 2.10a and its de-embedded structures as shown in Figs. 2.11a and 2.12a can be laid out and fabricated for measurement, characterization, and comparison with the simulation results. The de-embedded open and short structures are employed for de-embedding purpose to eliminate the impacts from the testing PADs and the parasitic metal traces connecting between the transformer core and the testing PADs. For simplicity, the single-ended testing structures with one port of the primary and secondary coils being directly connected to the ground plane are considered here. If a 4-port network analyzer is available, the fully differential testing structures can be constructed in a similar way. The de-embedding principles and procedures in Step 6 can also be applied to the differential testing structures.

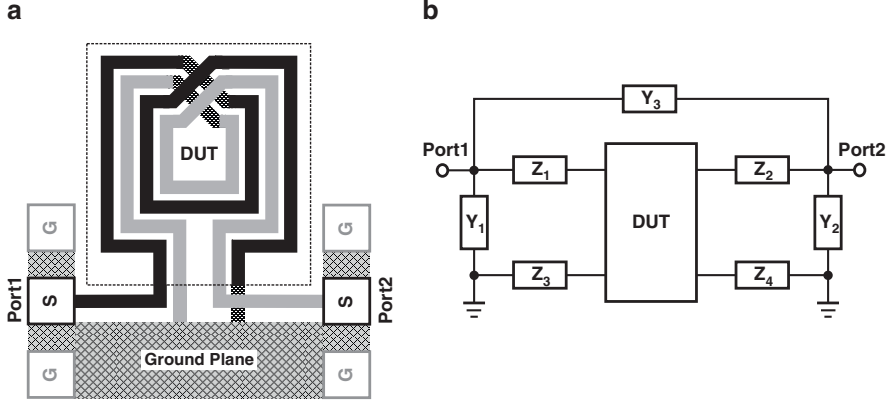


Fig. 2.10 (a) Layout and (b) equivalent circuit of the transformer testing structure

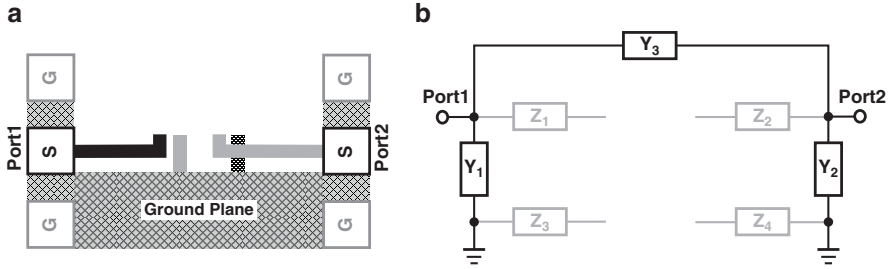


Fig. 2.11 (a) Layout and (b) equivalent circuit of the open de-embedded structure

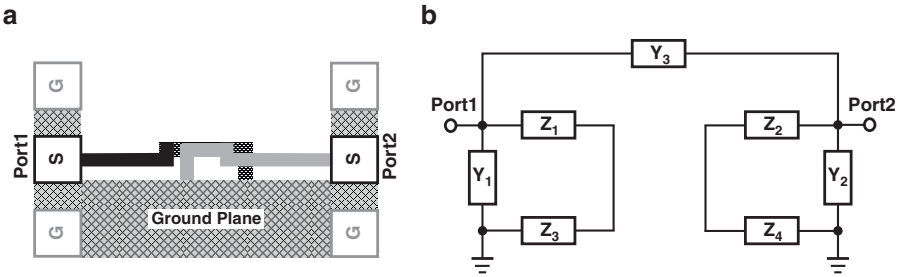


Fig. 2.12 (a) Layout and (b) equivalent circuit of the short de-embedded structure

Step 6: Using a 2-port network analyzer, the S-parameter of the transformer testing structure (S_{raw}) in Fig. 2.10a and the de-embedded structures (S_{open} and S_{short}) in Figs. 2.11a and 2.12a can be obtained by on-chip probing. The S-parameters (S_{raw} , S_{open} , and S_{short}) can be further converted to the Y-parameters (Y_{raw} , Y_{open} , and Y_{short}) by using the following equations [9]:

$$Y_{11} = \frac{1}{Z_0} \cdot \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (2.6a)$$

$$Y_{12} = \frac{1}{Z_0} \cdot \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (2.6b)$$

$$Y_{21} = \frac{1}{Z_0} \cdot \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (2.6c)$$

$$Y_{22} = \frac{1}{Z_0} \cdot \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (2.6d)$$

Using the Y-parameters, the following de-embedding procedures can be applied to obtain the corresponding electrical parameters of the transformer:

1. Extraction of the parasitic parameters Z_1 to Z_4 . According to the equivalent circuits for the open/short de-embedded structures as shown in Figs. 2.11b and 2.12b, the parasitic parameters Z_1 to Z_4 can be extracted by subtracting Y_{open} from Y_{short} to obtain Y_{DE1} first:

$$Y_{\text{DE1}} = Y_{\text{short}} - Y_{\text{open}} \quad (2.7)$$

and then converting Y_{DE1} to Z_{DE1} . So Z_{DE1} only contains the information of parasitic parameters Z_1 to Z_4 .

2. Open de-embedding for measurement data of the transformer testing structure. According to the equivalent circuits for the transformer testing structure and the open de-embedded structures as shown in Figs. 2.10b and 2.11b, the effect of parasitic parameters Y_1 to Y_3 can be removed by subtracting Y_{open} from Y_{raw} :

$$Y_{\text{DE2}} = Y_{\text{raw}} - Y_{\text{open}} \quad (2.8)$$

3. Short de-embedding for measurement data of the transformer testing structure. After converting Y_{DE2} to Z_{DE2} , the effect of parasitic parameters Z_1 to Z_4 can be removed by subtracting Z_{DE1} from Z_{DE2} :

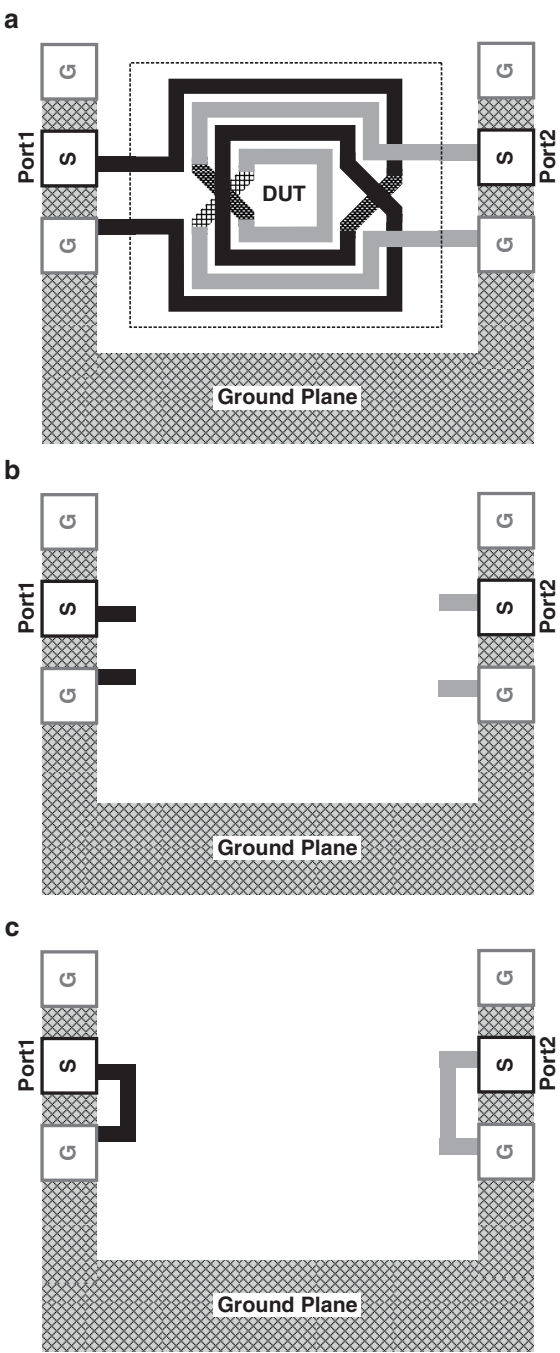
$$Z_{\text{DUT}} = Z_{\text{DE2}} - Z_{\text{DE1}} \quad (2.9)$$

Here, Z_{DUT} represents the impedance of the transformer core after de-embedding. By applying (2.5a–2.5c), the measured self-inductance, quality factor, and coupling coefficient for the transformer core can be obtained.

Step 7: Finally, the measured electrical parameters are compared with the EM simulation results. If the results are not satisfactory, the transformer design would need to be modified by going back to Step 3, starting from the EM simulation of the modified design. The differences between the simulation and measurement results of the transformer can also be utilized to correlate the difference in the measured circuit performance for further optimization.

In the transformer layout in Fig. 2.10a, the primary and secondary ports are located on the same side. If the two ports of the transformer need to be placed on the different sides, the layouts of the testing structures also need to be changed to those as shown in Fig. 2.13.

Fig. 2.13 Layout of testing structures for the transformer with two ports on different sides: (a) the transformer testing structure, (b) the open de-embedded structure, and (c) the short de-embedded structure



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