

# Chapter 2

## MEMS Technologies for Energy Harvesting

**Manuel Domínguez-Pumar, Joan Pons-Nin  
and Juan A. Chávez-Domínguez**

### 2.1 Introduction

The technology of Microelectromechanical Systems, or MEMS, is generally defined as the miniaturization of mechanical and electromechanical structures that are fabricated using standard processes from the integrated circuit industry and other compatible processes usually aimed at ‘sculpting’ 3D structures. MEMS can in particular include moveable parts such as cantilevers, beams, membranes, plates, etc. They may present interactions with biological, chemical and thermal phenomena, including interaction with fluids. At the same time MEMS devices usually interact with fields and forces that are not electromagnetic, such as mechanical forces, piezoelectric and thermoelectric forces, among others. This has promoted MEMS technology to be an excellent tool for the miniaturization of energy harvesters.

Common physical dimensions of MEMS can range from below 1  $\mu\text{m}$  (in this case they are usually called Nanoelectromechanical), up to the mm scale. It is remarkable that generally the MEMS equivalent of a sensor/actuator macrosystem outperforms the latter. Among other factors, the repeatability and high reliability of MEMS batch fabrication processes can clearly contribute to this improvement, while at the same time even reducing the unit cost. Furthermore, the recent merging between MEMS and CMOS technology has opened new platforms on which both the microelectromechanical parts and the sensing/actuation circuits can be found within the same silicon die.

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M. Domínguez-Pumar (✉) · J. Pons-Nin  
MNT-DEE, Technical University of Catalonia, Barcelona, Spain  
e-mail: manuel.dominguez@upc.edu

J. Pons-Nin  
e-mail: joan.pons@upc.edu

J.A. Chávez-Domínguez  
GSS-DEE, Technical University of Catalonia, Barcelona, Spain  
e-mail: juan.antonio.chavez@upc.edu

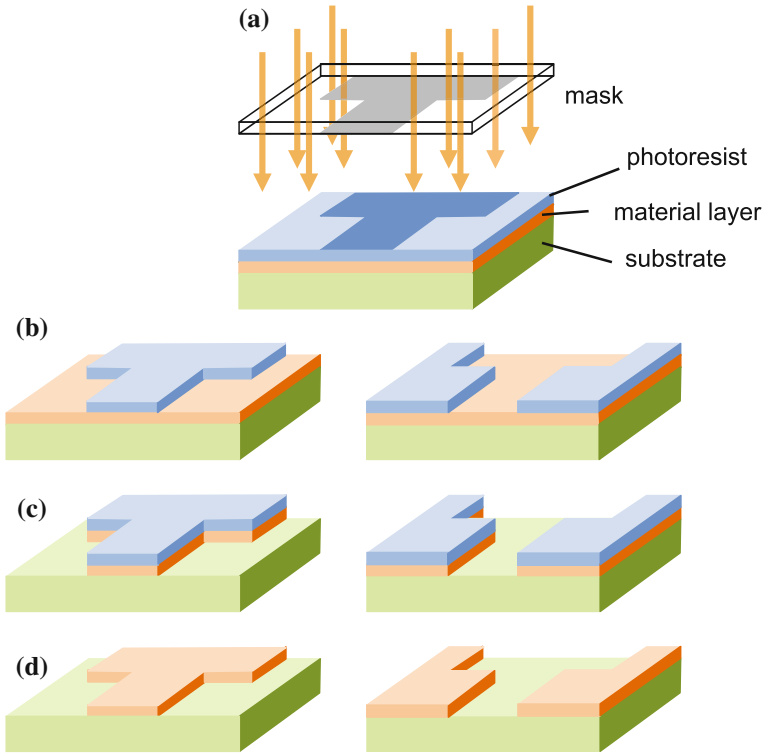
This chapter is divided into three main parts. Section 2.2 introduces the most common fabrication processes used in MEMS technology. Special attention is paid to the processes that are specific to MEMS such as anisotropic etching. Section 2.3 introduces the main design procedures that have been used in MEMS to generate nonlinear actuation and sensing in energy harvesters. In particular the creation of bistable potentials, impact energy transfer and nonlinear springs is addressed. Recent examples found in the literature are presented and linked with the fabrication of the devices. Finally, due to its growing relevance, an introduction to piezoelectricity is given in Sect. 2.5. Some examples also found in the literature of energy harvesters designed using piezoelectric actuation and sensing are also introduced.

## 2.2 MEMS Fabrication Processes

This section provides a brief guide to the fabrication processes used in MEMS technology. As MEMS fabrication developed out of integrated circuits (IC) fabrication, we first focus on the main differences between MEMS and IC technologies. A description of the deposition and etching techniques most frequently used for MEMS follows. Special emphasis is made on those techniques that are MEMS-specific, such as anisotropic etching, wafer bonding, and, in particular, deep reactive-ion etching. The next focus is on MEMS fabrication strategies, including surface micromachining, bulk micromachining and silicon on insulator (SOI) based techniques. Finally, an example is provided of a commercial process aimed at the fabrication of piezoelectric MEMS devices that can be suitable for energy harvesting applications, among others.

### 2.2.1 IC Versus MEMS Fabrication

IC and MEMS fabrication possess a common series of process steps (e.g. photolithography, etch, oxidation, diffusion, LPCVD or sputter deposition) and materials (e.g. silicon, polysilicon, silicon nitride, silicon oxide or metals). In fact, IC and MEMS fabrication technologies can be seen as a complex sequence of deposition, material growth, lithography and etching processes. The objective of lithography is to translate a geometrical pattern onto a given material layer. The basic steps of standard contact lithography are shown in Fig. 2.1, where the layer to pattern is on the substrate. First, a thick layer of photoresistive polymer (photoresist) is deposited on top of the layer to be patterned. Next, the photoresist is exposed to light through a mask with opaque areas corresponding to the desired pattern. Due to such illumination, the solubility of the photoresist to developers becomes very different between shadowed and illuminated areas, Fig. 2.1a. The photoresist is then developed to obtain the desired pattern, which may be that of the mask (positive photoresist) or its complement (negative photoresist), Fig. 2.1b. The pattern in the photoresist is then transferred to the target



**Fig. 2.1** Photolithography-etch process with either positive (*left*) or negative (*right*) photoresist: **a** exposure to light through the mask, **b** photoresist develop, **c** layer etch, **d** photoresist removal

layer using selective etching techniques, Fig. 2.1c. Finally, the remaining photoresist is chemically stripped, Fig. 2.1d.

MEMS technology, on the other hand, has unique requirements and a growing set of applications that makes it clearly diverge from IC fabrication [1, 2]. The first obvious distinction is that MEMS can make use of thicker deposited or grown layers and deeper etchings. It may well be the case that even the whole substrate is to be etched in some parts of the wafer. Second, MEMS fabrication involves a wider variety of materials, including quartz, ceramics, polymers, glass, piezoelectric and magnetic materials, etc. As a consequence, processes such as electroplating, wafer bonding, molding, anisotropic wet etching or deep reactive-ion etching, are more common, or specific, to MEMS fabrication. Third, some devices must be processed on both sides of the wafer, thus adding front-backside alignment as a technological necessary requirement for certain devices. A fourth difference is that MEMS devices include moveable mechanical parts such as beams and membranes that must be released. Additionally, the mechanical properties must be carefully controlled to avoid release distortion due to phenomena such as residual stress or stiction. Obviously controlling the mechanical properties of layers requires considerable effort. Putting all this

together, a remarkable characteristic of MEMS technology is the existence of multiple and very diverse MEMS fabrication processes. This is especially true in the area of energy harvesting, where many different processes are designed in order to obtain tailored mechanical properties of the devices. This fact represents in itself a large divergence from what is, generally, the more common situation in IC technology.

### **2.2.2 Addition Processes for MEMS**

Addition of materials onto a wafer is basic in MEMS. Process steps such as doping, thermal oxidation and epitaxy are inherited from IC technology. For instance, diffusion and ion implantation techniques are used in MEMS, but not in the same fashion as in IC technology. In the latter case, the objective is to have a very strict control on the electrical properties of the devices. In the MEMS case, though, the goal can be simply to convert a resistive layer into quite a good electrical conductor.

Thermal oxidation is a simple process used to grow good-quality thin films of silicon oxide on silicon substrates. The substrate is immersed into an oxygen-rich environment, which can be wet/liquid or dry/vapour. High temperatures, from 800 to 1100 °C, speed up the chemical oxidation of the substrate. However, as the thickness of the oxide layer increases, the substrate surface becomes harder to reach for the oxygen molecules. This effect causes nonlinear reduction of growth rate for thicknesses greater than 100–200 nm.

Other addition, or deposition, processes also come from IC technology, but due to the above-mentioned expansion to new applications the variety of specific MEMS processes is growing continuously. The next sections will focus on the physical and chemical deposition processes widely used for MEMS.

#### **Physical Deposition**

Physical deposition implies the direct transfer of a material, from a certain source, on the wafer surface. Examples are evaporation, sputtering and casting. Evaporation and sputtering are often used to deposit metals such as copper, gold and aluminium, among others. Evaporation is also used to deposit polymers. Casting is a common method to deposit polymers and glass. The thickness of deposited layers can range from a few hundreds of nanometres to microns. These processes are made at low temperatures, and may therefore be compatible with previous process steps executed on the wafer. On the other hand, the quality of the layers (e.g. density of defects, resistivity, etc.) is not as good as when deposited by chemical methods.

- In **Evaporation** the source material and the wafer are placed inside a vacuum chamber. There, the source material is heated until it boils and evaporates. Being in vacuum, the evaporated molecules freely travel and condensate on all surfaces inside the chamber, including the wafer. A method to heat the source material consists of placing it in a tungsten chest and then applying a high current. A high-

energy electron beam or a laser targeting the source material are other common heating methods that serve to speed up the process.

- **Sputtering** is also performed inside a vacuum chamber. The chamber contains the source material, called target, the destination wafer and gas plasma at low pressure. RF power is applied to generate gas ions and accelerate them towards the target. This causes extraction, or sputtering, of target atoms. Sputtered atoms travel and condense on all surfaces inside the chamber. Sputtering is performed at lower temperatures than evaporation.
- In **Casting** the source material is first dissolved in a liquid solvent. Then the solution is dropped on the wafer either by piping or spraying techniques. Next, the wafer is spun to spread the solution uniformly over the entire surface (spin coating). A material layer, with thickness that can range from the nanoscale to tens of microns, is obtained once the solvent has evaporated. Due to their solubility in organic solvents, casting is a common practice for the deposition of polymers, including photoresists used in photolithography.

## Chemical Deposition

In this case, the source material is obtained from a chemical reaction taking place close to the wafer. Favourable conditions to excite and control the reaction, such as temperature, pressure, electric field or presence of plasma, are provided by specific equipment, which also provides means to remove the byproducts of the reaction.

- **Chemical Vapour Deposition (CVD)** is achieved by placing the wafer inside a reactor. A chemical reaction between two or more gas species produces the source material, which condenses on all surfaces inside the reactor, wafer included. CVD yields thin layers with almost-uniform thickness and good coverage, even on stepped topographies. A variety of materials, including polysilicon, silicon nitride, silicon oxide, phosphosilicate glass (PSG), ceramics and plastics, can be deposited. Some materials are unpopular because of reactor contamination or due to the hazardous byproducts they generate.

Low Pressure CVD (LPCVD) is performed at high temperature (from 500 to 800 °C). It yields fair material properties and layers with uniform thickness, but slow deposition rates. As an example, polysilicon deposition is achieved by decomposition of silane gas ( $\text{SiH}_4$ ) into solid silicon and hydrogen gas under temperatures around 600 °C. Plasma Enhanced CVD (PECVD) is performed at lower temperatures because plasma adds extra energy to the gas mixture, but the layers have inferior quality compared with LPCVD layers. PECVD is often used for fast deposition of low-quality silicon oxide.

- **Electroplating** is a generic technique with many industrial applications. In MEMS, it is mainly used to deposit metals such as nickel and gold. The surfaces on which we wish to deposit the corresponding metal are previously coated with a conductive material, if they are not conductive themselves. Then the wafer is immersed into a liquid electrolyte solution. By applying a voltage between the wafer and an electrode also immersed in the solution, a reduction–oxidation reaction is excited. As a result, wafer surfaces are coated with the source material. In this way, nearly

uniform metal layers with thickness ranging from microns to tens of microns can be deposited.

Some appropriate chemical mixtures allow the reaction to take place without applying any external voltage, or without placing contacts or electrodes within a liquid. In this case, known as electroless plating, the reaction is excited by the electrochemical potential between the solution and one or more materials on the wafer. However, the reaction behaves spontaneously and results such as deposition rate and layer thickness are difficult to control.

## Wafer Bonding

The objective of wafer bonding is to obtain a permanent contact of two wafers. This process can also be performed at die level or at device level. Wafer bonding allows addition of materials obtained from different processes, but is also highly useful for other processing and post-processing purposes, such as planarization, wafer sealing in vacuum, packaging or MEMS-IC integration.

Wafer bonding can be performed in many ways, chemical or physical, depending on materials to join and compatibility with other fabrication processes. In general, three subsequent steps are applied: (1) wafer preprocessing (cleaning and pretreatment of the surfaces to contact and, if needed, addition of intermediate layers), (2) wafer alignment and contact (it usually yields weak adhesion), (3) annealing and bond consolidation (by temperature, pressure, electric field, intermediate layer hardening, etc.).

Let us distinguish among direct and indirect bonding processes

- **Direct bonding** is performed for wafer to wafer contact. The process is activated and enhanced by a temperature or an electric field. For example, silicon-to-silicon bonding is achieved with annealing temperatures around 800 °C, a value often not compatible with other processes. Plasma enhanced bonding allows to decrease the temperature to 400 °C or less. In anodic bonding, the wafers are stacked and placed between two electrodes, where voltage is applied. This low-temperature process is mostly used for glass-to-silicon and glass-to-metal bonding. In thermocompression, pressure force and temperature are applied simultaneously to the stacked wafers until solid diffusion occurs. This process is used for metal-to-metal bonding.
- In **indirect bonding**, an intermediate material is placed between the wafers. This material provides long-time adhesion properties and reduces the relevance of the properties of the surfaces to contact (e.g. defects or topography). In adhesive bonding, polymers such as BCB (benzocyclobuten) or SU-8 (a negative photoresist) are used. Annealing is performed at relatively low temperature, with no voltage required. Since the wafers are not in direct contact, bonding of many different materials is enabled. In glass soldering, a glass layer with low melting point is used as an intermediate material. In eutectic bonding, the intermediate material is a metal alloy. This alloy goes directly from solid to liquid state at temperatures far below the melting points of the metals involved. This way, good-quality aluminium-to-silicon and gold-to-silicon bonding is achieved.

### 2.2.3 Etching Processes for MEMS

Etching processes are crucial in MEMS fabrication. Selectivity of etchant species against protection (masking) materials, substrates and the target material is a major issue, but etch rate, etch uniformity and temperature are also key characteristics. Let us first distinguish between wet and dry etching processes.

#### Wet Etching

Wet Etching is relatively simple and cheap. It allows to attack a material by immersing the wafer into a liquid etchant. The etchant chemically reacts with the material in unprotected areas. Wet etching can be isotropic or anisotropic.

- **Isotropic wet etching** is a classical technique performed to remove a wide range of materials, including semiconductors, dielectrics, metals or polymers. When used for patterning purposes, isotropic etching causes undercutting: the chemical reaction attacks the walls under the protection mask and produces a lateral etch effect, Fig. 2.2a. The amount of undercutting is the same distance as etch depth, thus it affects pattern transfer precision.
- **Anisotropic wet etching.** Solubility properties of crystalline materials may vary with crystal orientation. In silicon, potassium hydroxide (KOH) and ethylene diamine pyrocatechol (EDP) have different etch rates along the three crystallographic planes. For example, KOH yields etch rate selectivity of 300:1 or higher between the  $\langle 100 \rangle$  and  $\langle 111 \rangle$  planes. This means that etching can be virtually stopped on certain planes, and therefore substrates can be “sculpted” to produce a variety of structures. As an example, a trench is built in Fig. 2.2b.

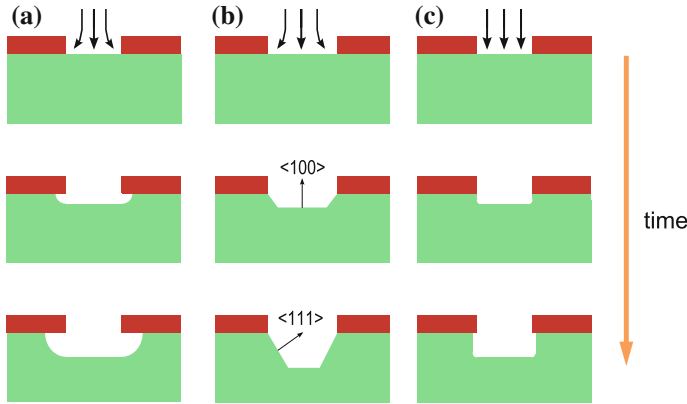
The alignment of the mask against the crystal planes, the etchant used and the process time are key factors. Additionally, precise temperature control and gas reflux systems are required to keep the etchant concentration constant during the process, and therefore the etch rate. Wet etchant and related byproducts are hazardous substances that may cause handling or environmental safety problems.

Anisotropic wet etching produces characteristic geometrical forms, since planes are not vertical to the surface when etching holes or trenches, as seen in Fig. 2.2b. This implies large silicon consumption, loss of precision in pattern transfer and limits what structures are possible.

#### Dry Etching

In dry etching, the wafers are placed inside chambers that contain either gas or plasma reacting with the target material. In general, dry etching yields better etch performance than wet etching, but at noticeably higher costs due to the more sophisticated equipment used.

- **Isotropic gas etching** utilizes a gas with high etch selectivity against the mask protection material. As an example, xenon difluoride ( $\text{XeF}_2$ ) has etch selectivity of silicon versus silicon oxide up to 10,000:1, whereas selectivity versus silicon nitride is around 100:1.

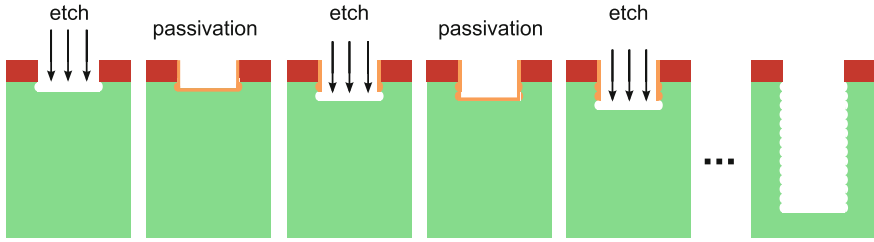


**Fig. 2.2** Typical trench profiles obtained in silicon with different etch processes: **a** isotropic etching, **b** wet anisotropic etching—two crystallographic axes shown—, **c** anisotropic dry etching

- **Plasma etching** is performed inside a specific reaction chamber that contains chemically active gas species at low pressure and applies an electric field to the gas. The electric field creates electrically charged gas radicals, which chemically react with the wafer material. In addition, the electric field may cause a physical etch effect: the charged radicals accelerate until they hit and sputter the wafer material. The physical etch component is anisotropic, whereas the chemical component is isotropic and material selective.
- **Reactive Ion Etching (RIE)** is a special kind of plasma etching. In RIE, RF power is applied to increase the physical component of the etching, therefore it can be more anisotropic than traditional plasma etching. Moreover, the chemical-isotropic and physical-anisotropic mechanisms can be balanced to obtain etched features with rounded to nearly vertical sidewalls. However, the process has many parameters to adjust and this implies long-time development until the desired balance is achieved. In practice, RIE is limited in etch depth (e.g. tens of microns for silicon) and etch rate (e.g. typical values around  $1 \mu\text{m}/\text{min}$  for silicon). The next section focuses on Deep RIE, a special class of RIE that has gained enormous popularity in modern MEMS fabrication.

### Deep Reactive-Ion Etching

Deep Reactive-Ion Etching (DRIE) is a highly anisotropic process aimed at creating deep holes and trenches in silicon, with high aspect ratios and nearly vertical side walls. It was first developed by the German company Robert Bosch GmbH [3, 4]. The process is performed at room temperature. DRIE strongly improves etch performance against traditional anisotropic dry and wet etching techniques: silicon etch depths up to  $750 \mu\text{m}$  at rates up to  $25 \mu\text{m}/\text{min}$  are typically achieved. Etching uniformity at wafer scale is also improved.



**Fig. 2.3** Successive etching and passivation steps of a DRIE process

The DRIE process performs RIE in small depth increments by alternating two different gas mixtures in the reactor

1. The first mixture (e.g.  $\text{SF}_6$  for silicon) provides standard RIE etching of the substrate, or another thick layer, through a window opened in a mask material (e.g. photoresist, silicon oxide, silicon nitride and metal, among others). This results in nearly vertical etching of the substrate.
2. The second mixture (e.g.  $\text{C}_4\text{F}_8$ ) deposits a passivation layer. This layer dissolves very slowly in the chemical part of the subsequent RIE etch. The RIE directional ions attack the passivation layer at the bottom of the etched area. Then this bottom layer is sputtered off and the substrate becomes exposed to the chemical etch.

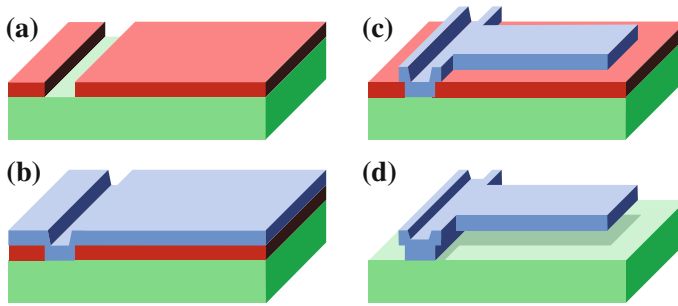
An etch-passivation cycle only lasts for seconds. It is repeated many times, resulting in a large number of small etch steps only taking place at the bottom of quasi-vertical sidewalls, Fig. 2.3. However, the sidewalls have slightly undulated shapes, with typical amplitudes from tens to a few hundreds of nanometres. Cycle times can be adjusted for a trade-off between smoother walls and higher etch rates [5].

Specific DRIE recipes have been developed for materials other than silicon, including glass, silica, quartz, InP and polymers. DRIE of glass substrates is performed applying high RF power, but this implies that mask materials must be carefully chosen. Chemically amplified photoresists and polysilicon are typically used as mask materials in DRIE of glass. Metal masks are used in DRIE of polymers, but this is expensive due to the additional deposition and lithography steps they require.

## 2.2.4 MEMS Fabrication Strategies

### Surface Micromachining

MEMS surface micromachining aims at building moveable structures by deposition and patterning of different layers on top of the substrate. The moveable parts of the devices are made of what are called structural materials. These materials are deposited on top of what are called sacrificial layers, previously deposited or grown to hold the structural parts. The sacrificial layers will be removed later during the



**Fig. 2.4** MEMS cantilever fabrication using surface micromachining

fabrication process. The removal of the sacrificial layers is known as the release process.

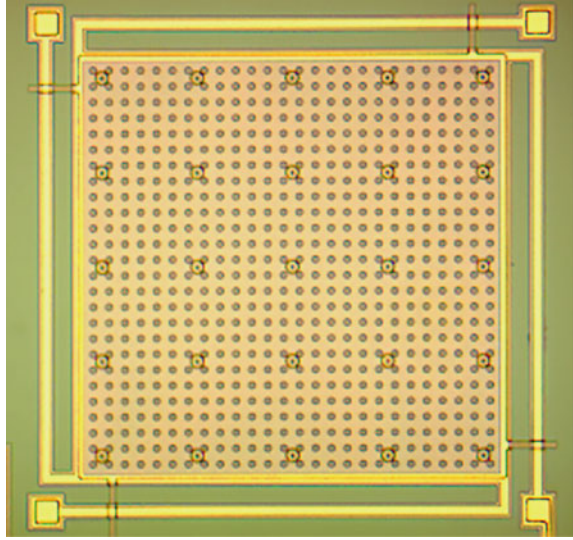
As an example, Fig. 2.4 summarizes a series of steps performed to build up a cantilever structure. To begin, the sacrificial layer (i.e. silicon dioxide) is deposited and patterned through a photolithography-etch process, Fig. 2.4a. The uncovered area will be used to attach (anchor) the device to the substrate. The structural layer (e.g. polysilicon) is then deposited on top of the wafer, Fig. 2.4b. Next, the structural layer is patterned to define the device, Fig. 2.4c. Finally, the sacrificial layer is etched. As shown in Fig. 2.4d, this creates a void, equal to the thickness of the sacrificial layer, below the beam.

MEMS surface micromachining has evolved directly from IC fabrication, but some strong differences arise. For instance, in surface micromachining only up to 7–8 masks and minimum feature sizes around  $0.5\text{--}1\text{ }\mu\text{m}$  are typically used; this decreases mask costs. However, in surface micromachining, layers are thicker than the thin films used in IC fabrication. This adds specific challenges to deposition and etch processes, including topography-related issues. As after 7–8 successive layer deposition and etch steps, the vertical dimensions of structures can be anything ranging from zero to tens of microns.

Another difference is that MEMS fabrication must take special care to control the mechanical properties, such as density, stress and Young's modulus, of structures to release. These properties are highly sensitive to the temperatures applied during fabrication. For example, successive heating and cooling can generate residual stress between two stacked layers due to the different thermal expansion coefficients of the materials. If one of such layers is removed, the released structure would not be flat and exhibit either tensile or compressive stress deformation, thus affecting the expected mechanical performance.

Finally, during the release process the surface tension of wet etchant can force contact between fixed and moveable parts of a device and cause stiction failure: the adhesion forces generated in the contact are strong enough to deform and permanently attract these parts. Dry etching, critical point drying (CPD) during the final phase of wet etching, increasing the surface roughness or coating the layer with low surface energy materials are techniques used to prevent stiction. For devices with large areas

**Fig. 2.5** *Top view of an electrostatic MEMS, taken from [6], fabricated with surface micromachining. A  $360 \times 360 \mu\text{m}^2$  polysilicon plate is held by four arms in “L” anchored to the substrate at the other ends. The plate is suspended over the substrate through a  $2 \mu\text{m}$  air gap and a  $0.65 \mu\text{m}$  silicon nitride layer*



to release, as the one shown in Fig. 2.5, it is common practice to etch regular grids of holes in the structural layer. This enables efficient diffusion of wet etchant during the etch of the sacrificial layer below.

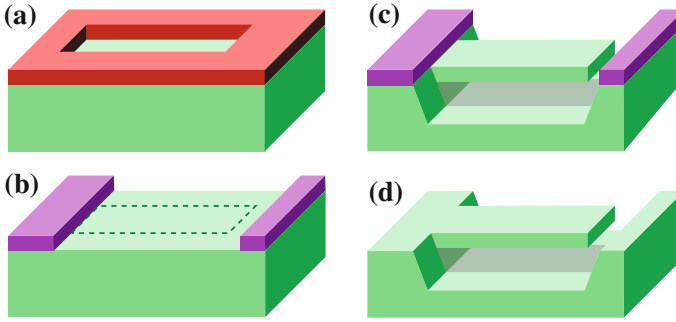
Since surface micromachining is relatively close to IC fabrication, it constitutes the most frequent basis to develop monolithic microsystems, where electronic (e.g. CMOS) and mechanical components are fabricated on the same substrate. The properties of the substrate are less important in surface micromachining than in other MEMS fabrication strategies, such as bulk or SOI micromachining. In this case, surface micromachining enables the use of substrate materials other than silicon, such as glass, quartz, plastics or organic polymers.

On the other hand, surface micromachining is not suitable to fabricate structures with large moveable parts, to use layers thicker than  $2\text{--}5 \mu\text{m}$ , or to build features with the high aspect ratios that some MEMS applications demand. Additionally, some geometrical structures are not possible to achieve, giving opportunities to other fabrication strategies, such as bulk and SOI micromachining.

### Bulk and SOI Micromachining

Unlike surface micromachining, bulk micromachining aims to create MEMS structures within the substrate. It is based on selective deep etching of materials such as silicon or glass. Bulk micromachining fabrication processes that combine anisotropic and isotropic wet etching have been widely used to obtain a variety of mechanical structures in silicon.

Figure 2.6 illustrates the fabrication of a silicon cantilever. A mask material (e.g. silicon dioxide) is first deposited on top of a silicon wafer. Then it is patterned by a lithography-etch process, Fig. 2.6a. A subsequent boron diffusion is performed in



**Fig. 2.6** MEMS cantilever fabrication in a silicon substrate using bulk micromachining

the uncovered substrate area. The  $p^+$  doped area becomes resistant against wet etch species.

Once the initial mask removed, a second protection layer (e.g. polyimide photoresist) is deposited and patterned, see Fig. 2.6b, where the dashed line encloses the boron diffusion. Next, anisotropic wet etching is applied to chemically attack the uncovered surface. Due to different etch selectivity along crystallographic planes and to the resistance of the  $p^+$  area, the substrate trench and the suspended structure shown in Fig. 2.6c are obtained. The last step is the removal of the protection layer, Fig. 2.6d.

Bulk micromachining techniques based on wet anisotropic etch of silicon are widely used in MEMS. However, these techniques have some issues. Notably, the cost in silicon is high, since large wafer areas are usually etched to obtain a unique device. A second issue are the process limits for which geometrical structures can be done and which are not achievable. Third, wet etching is unreliable to achieve structures with sizes below the micron scale.

In recent years, MEMS processes that use silicon on insulator (SOI) wafers in place of conventional silicon wafers have gained great popularity [1]. A SOI wafer is a stack of silicon, insulator and silicon layers. The MEMS structures are mainly fabricated in the top silicon layer, usually known as the device, or active, layer. This is good-quality crystalline silicon with well-known electrical and mechanical properties. In SOI wafers for MEMS the typical thickness of the device layer is tens of microns, well above the  $1\text{ }\mu\text{m}$  or less of SOI wafers used in IC fabrication. The buried insulating layer is typically silicon oxide, with thickness of microns or below. The bottom silicon layer, with typical thickness of hundreds of microns, is known as the handle substrate.

SOI-based MEMS processes allow one combine both bulk and surface micromachining techniques to obtain a rich set of structures. For example, the buried insulator can provide built-in stop for dry and wet etching processes performed in the device layer, but it can also be used to stop deep etch processes performed in the handle substrate. This way, features such as through-wafer holes, front or backside cavities of controlled depth, structure release from both sides of the wafers, full-wafer

thickness suspended structures, etc. can easily be achieved. Surface micromachining techniques can be also used, mostly on the device layer. A commercial SOI-based MEMS process is described in Sect. 2.2.4.

### Multi-project Wafer Processes

Some MEMS foundries offer multi-project wafer (MPW) processes. These are robust closed fabrication processes that provide well-known and reliable results. Additionally, MPW processes can be inexpensive, since wafers can be shared among several users. Their use facilitate users to focus on the device design, avoiding challenges associated with process development. MPW processes offer CAD tools such as device templates, design rules for layout checking and electrical and mechanical parameters for simulation. In general, MPW processes have not been targeted for commercial production, but used for research and prototyping. In recent years, some foundries have started providing specialized MPW services for low-volume production customers trying to reduce their design cost and time to market.

The first MPW process offered was a surface micromachining process developed by Howe and Muller [7, 8], with three polysilicon structural layers. Today, a number of MPW processes that use surface, bulk and SOI micromachining, electroplating and CMOS integration at wafer level are available. Some examples include

- MEMSCAP's MUMPS (Multi-User MEMS Processes) [9] offers PolyMUMPS, SOIMUMPS, MetalMUMPS and PiezoMUMPS. PolyMUMPS includes surface micromachining with three polysilicon structural layers and two silicon oxide sacrificial layers. SOIMUMPS combines SOI bulk and surface silicon micromachining. MetalMUMPS combines electroplating, surface and bulk micromachining, with nickel and polysilicon as structural materials. Finally, PiezoMUMPS adds a piezoelectric layer to a process similar to SOIMUMPS.
- Sandía SUMMiT (Sandia Ultra-planar, Multi-level MEMS Technology) V [10] is a surface micromachining process similar to PolyMUMPS, but with five structural layers and including planarization.
- InvenSense's NF Shuttle process [11] offers MEMS-CMOS integration. MEMS SOI devices and CMOS circuitry are fabricated on separated wafers. Then the wafers are bonded together using low-temperature eutectic bonding.
- Teledyne-DALSA's High Voltage CMOS/DMOS Technology with MEMS Post-Processing [12]. This process combines high-voltage CMOS circuitry and simple MEMS structures, with metal as the structural material.
- Lionix's TriPleX MPW and Fluidic MPW processes [13] are specifically targeted to devices for either integrated optics or microfluidic applications.

### The PiezoMUMPS Process

The PiezoMUMPS process [14] was introduced by MEMSCAP in 2013 as a response to the growing interest in piezoelectric MEMS. This low cost and low temperature process evolved from the previous SOIMUMPS. It uses the same SOI wafers and inherits some well-known bulk and surface micromachining features. The SOI wafer is a stack of, from bottom to top, a silicon substrate layer ( $400 \pm 5 \mu\text{m}$ ), a buried

silicon oxide layer ( $1 \pm 0.05 \mu\text{m}$ ) and the SOI device layer ( $10 \pm 1 \mu\text{m}$ ). A thin oxide layer is present on the bottom surface.

The process includes deposition and patterning of an aluminium nitride (AlN) piezoelectric film on top of the SOI device layer. It also includes deposition and patterning of additional metal and silicon oxide layers. Five mask levels are used. The minimum feature size for the SOI layer is  $2 \mu\text{m}$ , making structures with aspect ratios up to 5:1 possible.

In order to illustrate the process flow, let us apply it to obtain the unimorph piezoelectric cantilever shown in Fig. 2.7, a structure rather similar to resonators used in energy harvesting applications.

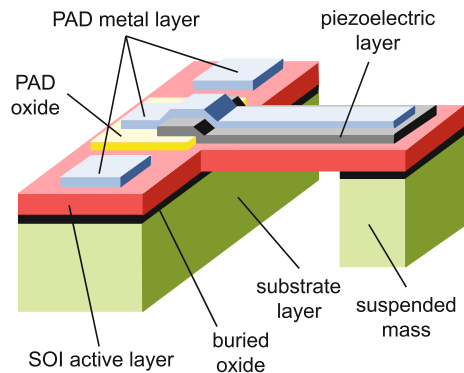
The process starts with LPCVD deposition of PSG on top of the SOI layer, Fig. 2.8a, followed by thermal annealing in argon atmosphere,  $1050^\circ\text{C}$  for 1 h. Due to the corresponding phosphorous diffusion, the surface of the SOI device layer becomes highly conductive ( $15\text{--}25 \Omega/\text{sq}$ ). After that, the PSG layer is completely removed by wet etching. Next, a  $0.2 \mu\text{m}$  layer of thermal oxide is grown on top surface. Through a photolithography-etch process using positive photoresist and RIE, the oxide is patterned accordingly to the PADOXIDE mask, Fig. 2.8b.

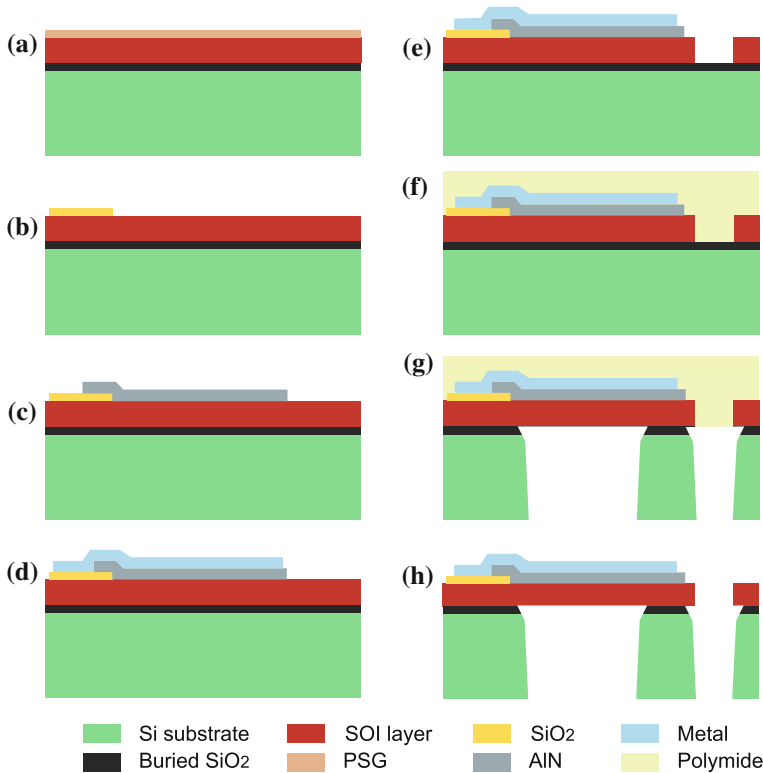
The first material deposited is a  $0.5 \mu\text{m}$  thick AlN piezoelectric layer. A reactive sputtering process is used for this purpose. Then, using photolithography with positive photoresist and wet etching, the PZFILM mask pattern is transferred to the AlN layer. That is followed by a photoresist strip, Fig. 2.8c.

Next, a metal stack composed of 20 nm of Chrome and  $1 \mu\text{m}$  of Aluminium is deposited and patterned using the following lift-off process: the wafer is coated with negative photoresist and exposed to light through the PADMETAL mask, then the photoresist is developed and the metal layer is deposited over the entire surface by evaporation; finally, the photoresist is dissolved to leave behind metal only in the uncovered (developed) areas, Fig. 2.8d. This process allows one define  $3 \mu\text{m}$  minimum metal features and spaces with  $3 \mu\text{m}$  tolerance alignment.

The  $10 \mu\text{m}$  SOI device layer is patterned using positive photoresist and the SOI mask. The pattern is transferred to silicon using a specific DRIE process, based on inductively coupled plasma (ICP) technology, that prevents undercutting of the

**Fig. 2.7** Unimorph piezoelectric cantilever structure with a full-wafer thickness mass suspended at the free end. The two outer metal PADs provide electrical contacts to the SOI active layer, while the one in the middle contacts the piezoelectric film



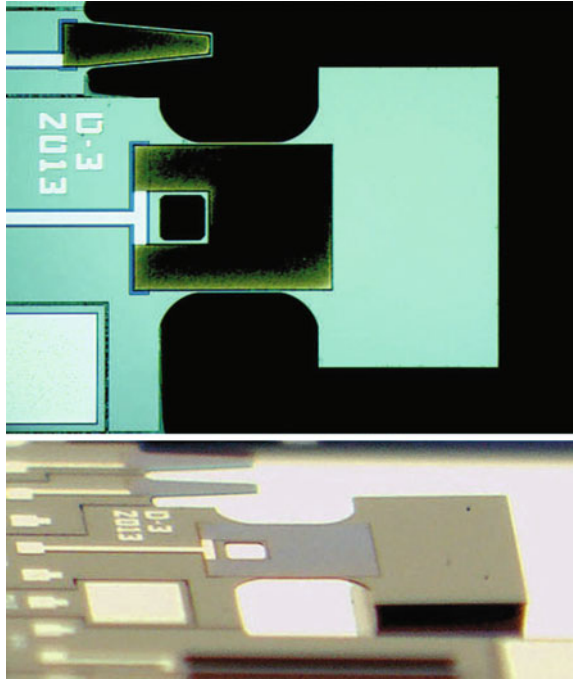


**Fig. 2.8** PiezoMUMPS fabrication process steps: **a** silicon doping, **b** thermal oxide deposition and patterning (PADOXIDE), **c** piezoelectric layer deposition and patterning (PZFILM), **d** metal layer lift-off (PADMETAL), **e** silicon device layer patterning (SOI), **f** polyme coating, **g** substrate layer patterning (TRENCH), **h** structure release

silicon when the etch reaches the buried oxide layer. After etching, the photoresist is stripped, Fig. 2.8e. Since the surface of the device layer is heavily doped, the separated metal features deposited on this layer will be electrically contacted unless they are also separated by a trench feature defined by the SOI mask.

Next, a thick polymide coating is applied onto the front surface of the wafer, Fig. 2.8f. This coating holds the wafer together through the next process steps. The wafer is then reversed and negative photoresist is deposited on the bottom surface. Next, the photoresist is patterned accordingly to the TRENCH mask. A RIE process is then used to remove the bottom oxide in the uncovered areas. Subsequent DRIE is performed to etch the TRENCH mask patterns through the substrate, until the buried oxide is reached. When the etch is completed, the remaining photoresist is stripped. Finally, wet etching is used to remove the oxide layer in the uncovered areas. As a result, the substrate layer is patterned accordingly to the TRENCH mask, Fig. 2.8g.

**Fig. 2.9** *Top and lateral view of a piezoelectric MEMS resonator fabricated in the PiezoMUMPS batch reported in [15]. Cantilever dimensions are  $1100\text{ }\mu\text{m}$  long and  $500\text{ }\mu\text{m}$  wide. The mass suspended at the free end has an area of  $600\text{ }\mu\text{m} \times 1000\text{ }\mu\text{m}$  and full-wafer thickness ( $410\text{ }\mu\text{m}$ ). The first mechanical resonance mode is at  $1.22\text{ kHz}$*



Finally, the front side protection coating is removed using a dry etch process. This releases the mechanical structures in the SOI active layer located over through-substrate holes, Fig. 2.8h. Figure 2.9 shows two photographs of a low-frequency MEMS resonator fabricated with PiezoMUMPS technology.

### 2.3 Nonlinear Mechanisms Used in Energy Harvesting with MEMS

The first approach made to energy harvesting was based on the use of linear resonators. The main disadvantage of linear devices is that they present a small bandwidth and therefore are only able to retrieve energy from a part of the mechanical excitations spectrum. To solve this issue, the use of resonators exploiting nonlinear mechanisms has been proposed as a way to, in some cases, dramatically enhance the performance of these devices. In this section, we introduce the main design techniques used in MEMS devices to implement nonlinear mechanisms such as bistable potentials, nonlinear springs and impact energy transfer.

### 2.3.1 Bistable Potentials

#### Bistable Potentials Obtained with Permanent Magnets

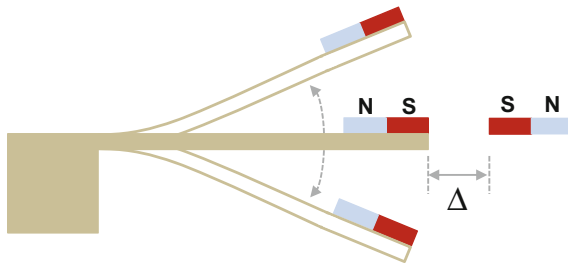
One of the methods used in the literature to produce bistable potentials is achieved by suitably placing a permanent magnet on top of a cantilever and another one fixed to the structure frame. By placing both magnets so that in the rest position they face each other with the same polarity, a bistable potential is easily generated. In [16] a MEMS device is presented on which the bistable potential is achieved by placing the permanent magnet at the tip of a BESOI (bulk etched SOI) cantilever, opposite another permanent magnet such that the polarity of both magnets is opposed at the nearest point, see Fig. 2.10. This configuration of magnets provides a repulsive force such that the rest position of the cantilever is no longer stable.

Regarding the fabrication, the authors use a BESOI technology with a bulk 450  $\mu\text{m}$  thick, 2  $\mu\text{m}$  of buried oxide, a 15  $\mu\text{m}$  crystalline silicon active layer and several deposited layers with oxide, polysilicon and metal. The cantilevers are 2000  $\mu\text{m}$  long with different widths in the range below 800  $\mu\text{m}$ . The permanent magnet deposited at the tip of the cantilever has a cylindrical shape and is made of NdFeB. Generally, the whole structure is manually assembled or microassembled, [17], since the fabrication process of the magnets is not compatible with the MEMS fabrication. This difficult placement can result in either non-repeatability or high production cost.

The obtained bistable potential is assumed to be that of a nonlinear pendulum governed by a double well nonlinearity

$$U(x) = kx^2 + (ax^2 + b\Delta^2)^{-3/2} + c\Delta^2 \quad (2.1)$$

where  $\Delta$  is the distance between the south poles of both, see Fig. 2.10, and parameters  $a, b$  and  $c$  depend on the specific geometry of the cantilever and its mechanical properties. Taking into account this kind of potential, the equation governing the dynamics of the inverted pendulum with the bistable potential is [18]



**Fig. 2.10** Schematics of the structure proposed in [16]: a cantilever with a fixed magnet at the tip, facing another magnet with south pole polarities facing each other. The rest position of the cantilever is no longer stable and whole structure is bistable

$$m\ddot{x} = \frac{dU(x)}{dx} - \gamma\dot{x} - K_v V(t) + \sigma\xi(t) \quad (2.2)$$

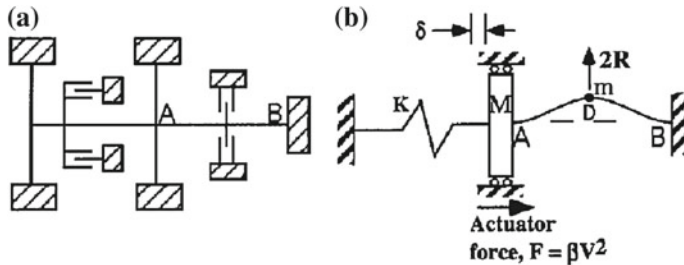
where the  $\gamma\dot{x}$  term represents mechanical damping,  $-K_v V(t)$  represents the energy transfer to the electrical domain and  $\sigma\xi(t)$  corresponds to the external vibration force driving the pendulum.

The main disadvantage cited against this type of structure is the presence of moving magnets, since they can generate fluctuations in the magnetic field which can affect other parts of the circuit, [19]. Furthermore, another disadvantage is the placement itself of the permanent magnets on the MEMS structures, which is usually made microassembled by hand. Electroplating [20], though, has been proposed as an alternative means to produce MEMS compatible permanent magnets, without manual assembly [21, 22].

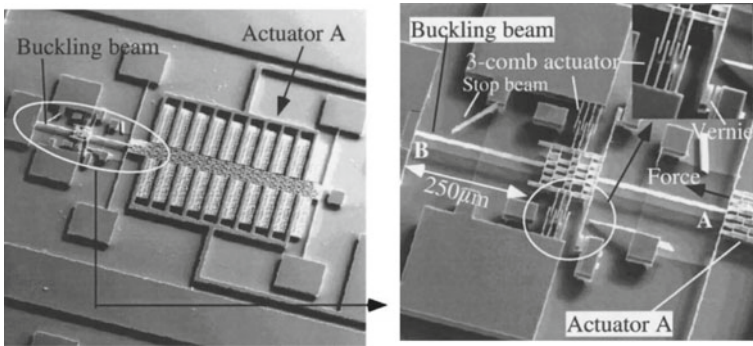
### Bistable Potentials Obtained by Buckling or Snap-through Instability

Buckling has also been used in energy harvesters to obtain a bistable potential. As it has been very well explained in [23], a bistable system is created by simply holding a business card between fingers and bowing it. A force normal to the surface of the card can make it snap from one stable position to the other. In order to obtain this kind of behaviour in MEMS structures, the axial load necessary for this buckling behaviour may come from residual stress of the fabrication process, or from the actuation with comb drives conveniently placed in the device to transmit an axial load to the corresponding beam [24]. Other mechanisms have also been established to create bistable mechanical structures such as: a clamp mechanism with an actuator to switch between stable states [25], or two curved parallel beams clamped in the centre [23] not relying on residual stress to obtain the buckling behaviour.

In [24] a tunable bistable mechanism is presented where an actuator generates a tunable axial compressive force on a beam, which is also subjected to a transversal force (see Fig. 2.11). The actuator is used to establish the necessary compressive force on the buckling beam to obtain the bistable potential. The beam is located between points A and B in the schematics of Fig. 2.11a. The actuator force, proportional to the square of the voltage applied on the comb drive (Fig. 2.11b), is shared between



**Fig. 2.11** Schematics of the structure proposed in [24]: **a** principle of actuation for a tunable bistable mechanism; **b** model of the structure

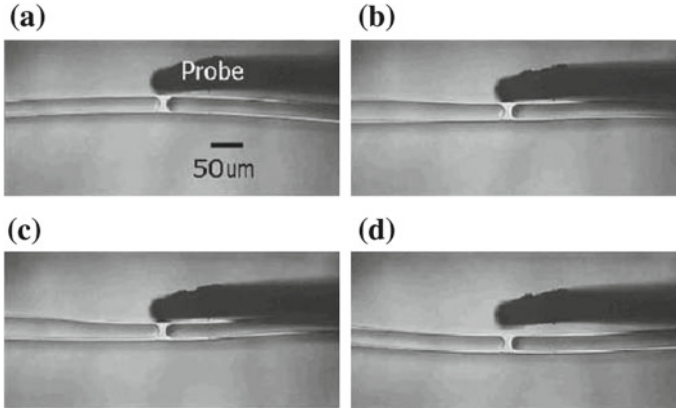


**Fig. 2.12** *Left:* overall photograph of the actuator and the bistable buckling beam of [24]. *Right:* detail of the beam and up and bottom comb drives

its own springs (located to the left in Fig. 2.11a) and the buckling beam. The force transverse to the beam is generated by two comb drives vertically arranged between points A and B in Fig. 2.11a). A photograph of the device can be observed in Fig. 2.12. The main actuator spans an area of  $1 \times 1 \text{ mm}^2$ , has 800 comb drives and is supported by six beams, held by anchors. It has been designed to generate only compressive stress on the buckling beam. The fact that this compressive force is exerted by the comb drives of the main actuator is what makes this device tunable, since the bistable potential can be modified as a function of the voltage applied to the main actuator.

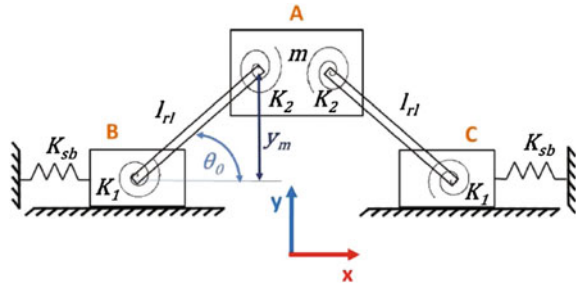
In [23] the authors present another bistable device that does not rely on prestress of the beam to produce buckling. They use two curved centrally clamped parallel beams to generate the bistable potential, see Fig. 2.13. A similar approach is taken in [26] on which preshaped buckled beams are designed [27]. In general, the physics of curved arches requires additional analysis in order to predict the nonlinear effects, due to the curvature of the structures and the snap-through instability [28, 29].

In [19] a bistable potential is obtained by a different structure on which a central mass is connected with two slightly slanted rigid fixed links through flexural pivots. In this way, two symmetrical stable positions can be achieved and therefore the structure presents a bistable potential. The equivalent mechanical model for the potential energy can be observed in Fig. 2.14. The slant angle, namely  $\theta_0$  plays an important role in the definition of the elastic potential of the structure, since it is used to generate the bistable potential (for  $\theta_0 = 0$  the potential is monostable), while at the same time it will generate an asymmetry in the elastic potential. The reason for this is that the slant angle makes the snap easier from one of the states than from the other. The potential energy of the mechanical structure is difficult to analyze and the authors use FEM simulations to obtain the elastic potential. However, in the final proposed structure, double fixed links are connected in a H configuration with a central mass. The whole thickness of the BESOI wafer ( $467 \mu\text{m}$ ) is used in the implementation of the arms. This is done in order to improve the mechanical stability of the design, specifically avoiding the appearance of unwanted vibration modes. The slant angle



**Fig. 2.13** Bistable mechanism of double curved beams, [23], **a** initial stable position, **b** applied force deflects the double beams, **c** more force generates more deflection, **d** beams at the second stable position

**Fig. 2.14** Pseudo-Rigid body model of the first microstructure proposed in [19]

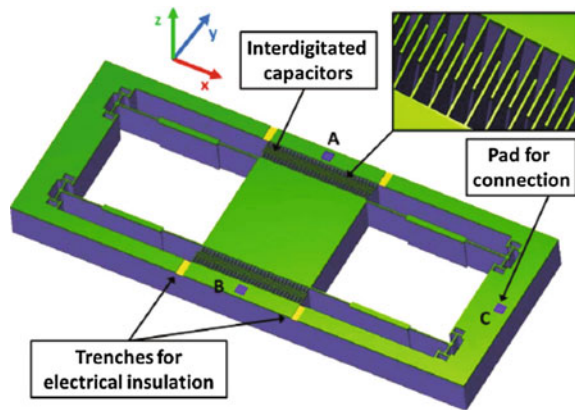


is finally chosen to be  $0.5^\circ$ . The sensing electrodes, consisting of a comb drive, are placed perpendicular to the direction of the fixed links and extract the mechanical energy harvested by the mechanical structure, see Fig. 2.15.

### 2.3.2 Nonlinear Springs

The use of nonlinear springs has been proposed to increase the effective bandwidth in energy harvesters. Nonlinearity in the spring stress–strain relationship can generate either a hardening, [30, 31], or a softening behaviour, [32, 33]. In the first case, the resonant frequency increases when the oscillation amplitude increases, while in the second case the resonant frequency decreases with increasing oscillation amplitude. In general both phenomena can occur in a device, but depending on some condition (applied voltage, dimensions of the structure, etc.) one of them dominates the other, [34]. Nonlinearity in springs appears for large deflections. For example, in the

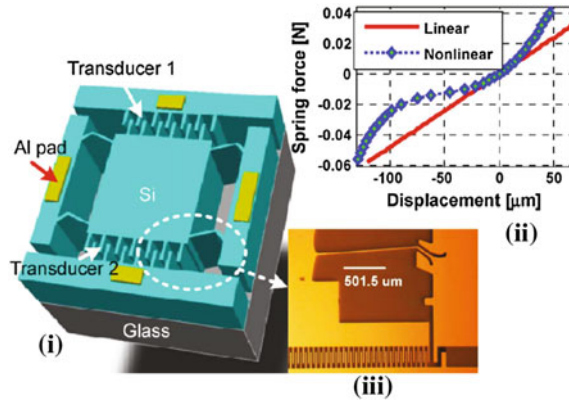
**Fig. 2.15** Model of the final structure proposed in [19]. Pads “A”, “B” and “C” are for the electrical connection of the comb capacitors



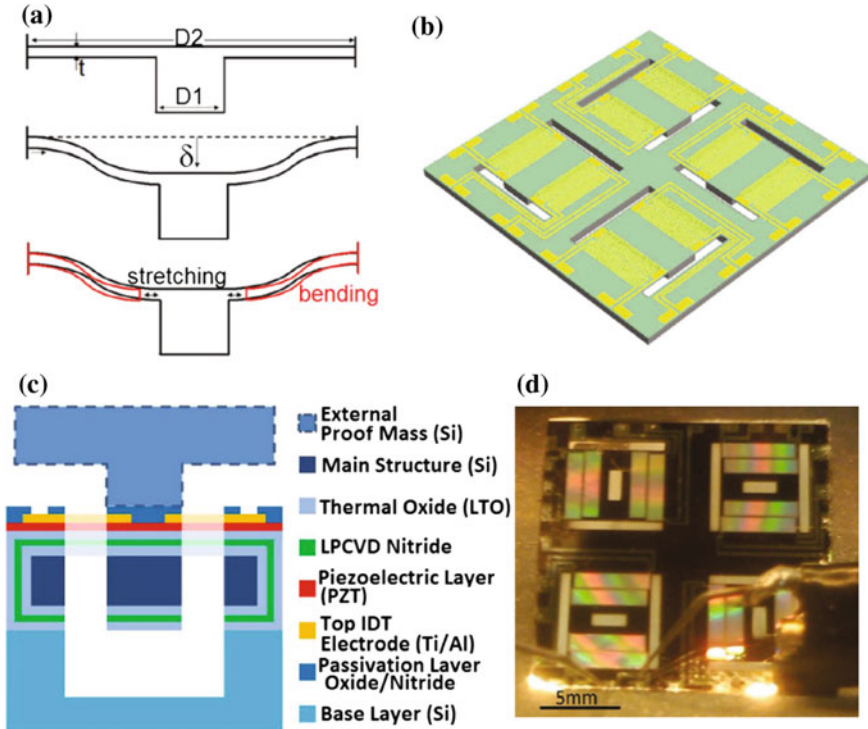
case of thin fixed-fixed beams, or tethers, it appears when the displacement of the proof mass is comparable or larger than the thickness of the springs, resulting in an increase of the strain energy due to stretching of the neutral surface, [34–36]. This is obviously an unwanted phenomenon in linear devices whereas it is a desired feature in some applications, such as energy harvesting, in which nonlinearity is sought as a means to increase bandwidth.

The authors in [32] present a wafer thick resonator that has nonlinear springs for enhancing energy harvesting. The fabrication process consists mainly of a full-wafer-thickness dry etch that serves to delimit the inertial mass and the supporting nonlinear springs. This wafer will be anodically bonded to a Pyrex glass wafer that has been previously wet etched so that the inertial mass is free to move. Special care has been taken by placing dummy protective structures close to springs and capacitor fingers. This is to limit inward sloping sidewalls in places where the etch opening is of the order of the etch depth or larger. In this design the spring restoring force is approximated by a seventh order polynomial. Figure 2.16 shows a model of the proposed structure, a photograph of the nonlinear spring and also the relation between the force versus displacement in the nonlinear spring obtained by FEM simulations. As can be observed in Fig. 2.16ii the softening behaviour is obtained only in one direction (negative displacement).

The authors in [37] propose to use a clamped–clamped configuration for the supporting thin beams of a proof mass. Each beam is clamped between the proof mass and the supporting structure. In this way, the displacement of the proof mass generates stretching. The only existence of bending would require lateral motion and, since the proof mass is in the centre of a clamped–clamped beam, this is not possible. This effect is illustrated in Fig. 2.17a. The fabrication process includes several steps comprised of both surface and bulk micromachining. The structural layer of the beams is composed of LPCVD silicon nitride and low temperature silicon oxide. The active layer consists of Ti/Al interdigitated electrodes, a PZT thin film and a layer of  $\text{ZrO}_2$ . A PECVD passivation layer is finally added to protect the active layer and compensate the residual stress. After the structure has been fabricated external

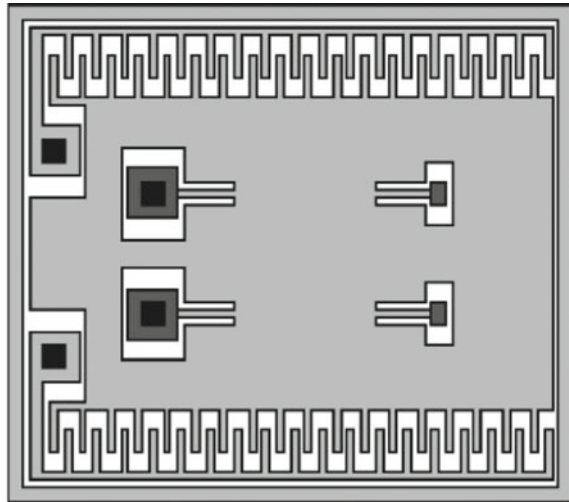


**Fig. 2.16** i Geometry of the device using nonlinear springs proposed in [33], ii spring force as a function of displacement of the nonlinear spring calculated by FEM, iii photograph of one the nonlinear springs in the device



**Fig. 2.17** Device proposed in [37]: a displacement of the proof mass generates nonlinear bending and stretching strain in the supporting beams, b general overview of the device with four beams supporting the main structure of the bulk silicon wafer. An external mass will be attached to the upper surface of the beams afterwards, c cross section of the structure, d photograph of the final device

**Fig. 2.18** Schematic of the device proposed in [38]. Dark grey rectangles are mass-spring anchorages and black squares represent electrical pads. The displacement of the proof mass is in plane between comb drives



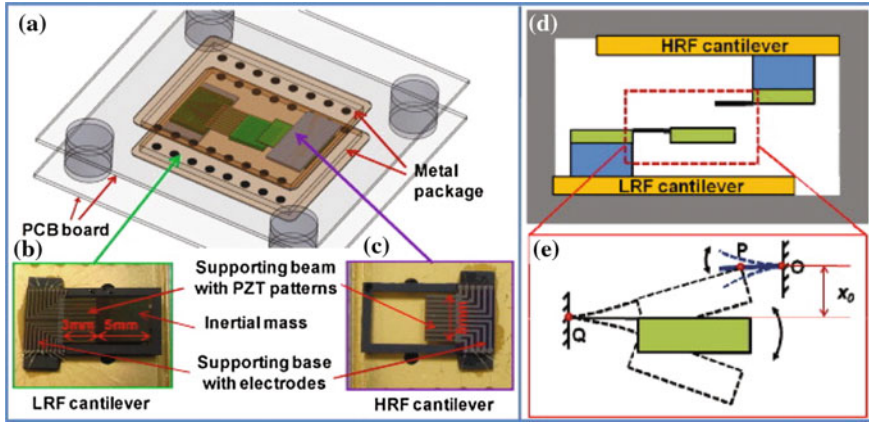
masses are attached to the upper surface of the beams to achieve a higher nonlinearity of the structure.

The authors in [38] propose an electrostatic harvester using a large mass subjected by nonlinear springs to increase the effective bandwidth. A schematic of the device can be seen in Fig. 2.18 on which two comb drives are at the top and bottom, while the inertial mass is anchored in four points (dark grey areas in the middle of the inertial mass). The device has been fabricated with a commercial SOI process from Tronics Inc. The nonlinear regime is obtained at large displacements of the inertial mass. The authors have fitted with a seventh order polynomial the nonlinear terms of the spring.

### 2.3.3 Nonlinear Energy Transfer by Impact

The first proposed use of impact in energy harvesting application can be traced back to [39]. Impact actuation can be seen as an example of pulsed actuations, i.e. an actuation on which the velocity of the device is almost instantly changed. This type of excitation has been used to obtain self-sustained oscillations in MEMS resonators, [40–42].

An example of energy transfer by impact applied to energy harvesting can be found in [43, 44] where the authors propose the use of two cantilevers, one with a low resonant frequency (LRF) and another with a higher resonant frequency (HRF) that may impact each other. The structure of the proposed device can be observed in Fig. 2.19. The LRF cantilever has a silicon inertial mass and has to be stopped by the HRF cantilever. For this purpose, a specific packaging has been designed. The LRF cantilever excites the second one, the HRF cantilever. This results in a



**Fig. 2.19** Device proposed in [43]: **a** Schematic of the overall system, **b** LRF cantilever, **c** HRF cantilever, **d** schematic of the arrangement of both cantilevers inside the packaging, **e** illustration of the impact between cantilevers

FUC, Frequency Up-Conversion, on which the energy is transferred from the LRF cantilever to the HRF.

The simplified equations of motion are

$$\begin{aligned}
 (m_0 + m_1)\ddot{z} + (c_0 + c_1)\dot{z} + (k_0 + k_1)z - k_1x_0 &= -(m_0 + m_1)\ddot{y}, & (z \geq x_0) \\
 m_0\ddot{z} + c_0\dot{z} + k_0z &= -m_0\ddot{y}, & (z < x_0)
 \end{aligned}
 \tag{2.3}$$

The excitation cantilever, LRF, has as a proof mass  $m_0$ , a damping coefficient  $c_0$  and a spring constant  $k_0$ . At a distance  $x_0$  the second cantilever is placed with a mass  $m_1$ , a damping coefficient  $c_1$  and a spring constant  $k_1$ . Both cantilevers interact when the displacement of the first one is greater than the distance between both resonators,  $z \geq x_0$ .

The fabrication process of the piezoelectric cantilever, [45], is started from a SOI wafer with a  $5\text{ }\mu\text{m}$  thick silicon active layer, a buried oxide of  $1\text{ }\mu\text{m}$  and the bulk of the wafer,  $400\text{ }\mu\text{m}$ . On top of the active Si layer, multiple layer depositions are made (the first one of Pt/Ti for the bottom electrode, second one of  $3\text{ }\mu\text{m}$  of (100)-oriented PZT, and a third metal deposition composed of Ti/Pt/Ti for the configuration of the top electrode). The metal depositions are made using sputtering and the PZT is deposited with a sol-gel process. The etching of the multilayer is made with an Ar-ion beam for the metals and the PZT layer is wet etched. The whole structure is passivated with a  $\text{SiO}_2$  layer deposited by sputtering. Holes are made on the oxide layer to place contacts. The bulk of the SOI wafer is later etched from the backside to release the moveable parts while preserving the inertial mass.

For this application, special care must be taken with the packaging because it must provide the correct separation between the cantilevers while at the same time one of them is placed upside-down, see Fig. 2.19.

## 2.4 Transduction Principles

The objective of this section is to present the specific requirements of electrostatic and electromagnetic transduction when used in energy harvesters. In particular the electrostatic transduction, in some devices, requires the presence of electrets. Electrets are dielectric materials on which permanent charge has been introduced. The movement of the electrets due to external vibrations can trigger currents in some parts of the device from which energy can be retrieved. Piezoelectric transduction will be treated later in a separate section.

### 2.4.1 *Electrostatic Transduction*

In electrostatic harvesters, the vibration energy is recovered by means of electrostatic force, which acts as a damping mechanical force. These kinds of devices require an initially precharged surface, so that the movement of a seismic mass generates a current flow in some part of a circuit. In order to provide this initial charge, several alternatives have been proposed such as insulated floating electrodes, [46], electrets [47, 48] and also electret-less circuits that require an external starting voltage or current, [49]. Electrets have been extensively used although they may require unconventional steps in the fabrication process.

On the other hand, some papers in the literature present electrostatic energy harvesters avoiding the presence of electrets or even external circuits necessary for precharging the structure. This kind of papers focus on the exploited mechanical nonlinearity or other features and use standard power sources to harvest. In this subsection, we will focus on electrets and we will present some examples of energy harvesters that make use of them.

Electrets are dielectrics on which a quasi-permanent charge has been injected, [50]. The lifetime of these charges can be very large. As an example, experiments on which a charge density has remained unchanged for 35 years are reported in [51]. Electrets present this charge, and therefore a stable built-in voltage, due to some previous ion injection, poling or application of a voltage. Among the materials most commonly used for electrets we find inorganic layers made of  $\text{SiO}_2$ , a combination of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  layers, [52], and also organic compounds based on polymers. Among the polymers compatible with MEMS processes we may find the amorphous perfluorinated polymer CYTOP (Asahi Glass Col., Ltd), [53–56]. This polymer can provide up to four times more charge density than Teflon.

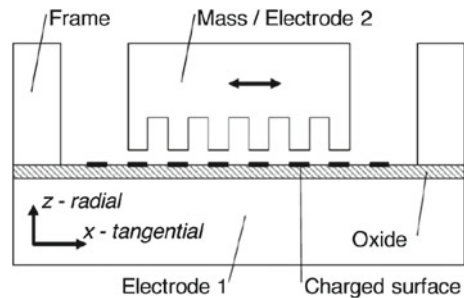
There are numerous methods used for poling electrets such as: corona charging, ion implantation, contact charging, thermal poling, UV irradiation, soft X-ray irradiation and electron-beam irradiation. Charges have also been successfully injected into electrets with very inexpensive equipment such as ionic hair-dryers, [56]. Corona charging generates principally surface charge whereas electron beam and thermal poling produce volume, surface charges and polarization. Thermal annealing may follow the corona charging to increase charge stability by driving charges to the bulk of the material. Long term, both  $\text{SiO}_2$  and CYTOP present good charge stability, [55], which is an essential property.

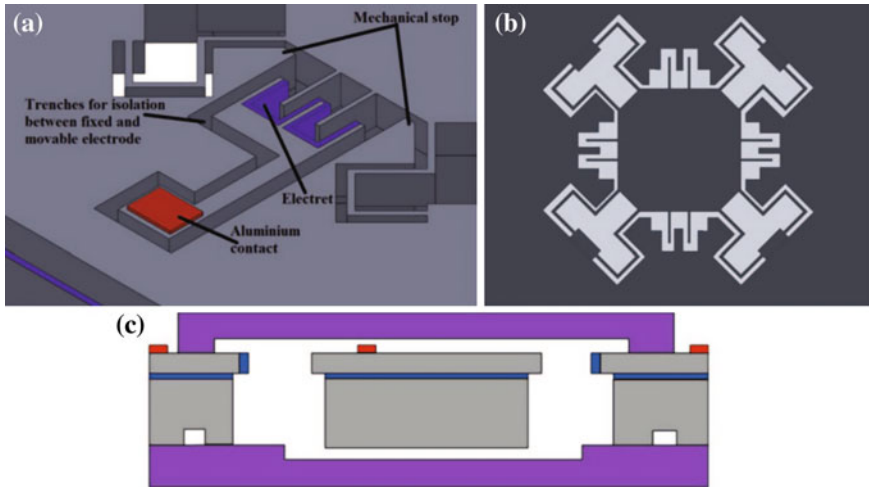
The more conventional approach for using electrets includes planar electrets, [57], although they can also be deposited on vertical walls, [56, 58]. Vertical electrets are more difficult to produce as, for example, the corona method or ion implantation cannot be used. On the other hand, vertical electrets are compatible with standard electrostatic comb drive actuation.

Examples of recent energy harvesters using electrets can be found in [56, 57, 59]. The authors in [57] propose an electrostatic energy harvester using an electret inside the active gap. Figure 2.20 shows a schematic of the device. The electret has been patterned in stripes on the bottom wafer while the proof mass, which is conductive, moves inside the potential generated by the electret. If a load is connected between electrodes 1 and 2, a current will flow and power will be transferred. Since the displacement of the mass can surpass a single electret stripe, frequency up-conversion may occur. This is because a single period in the proof mass movement can generate several electret stripe crossings and therefore several periods in the generated current.

The authors in [56] propose a 3D electrostatic energy harvester using sidewall electrets. The device allows one retrieve vibration energy in any direction due to the specific design that fixes an angle of  $45^\circ$  between the suspending beams and the comb drive electrodes with electrets, see Fig. 2.21. The pull-in contact between electrodes is avoided by the presence of the mechanical stoppers shown in Fig. 2.21a. The electrets have been vertically placed on the surface of the fixed electrode fingers and are made of  $\text{SiO}_2$ . The authors have charged the electrets using an hair-dryer that is commercially called “ionic hair-dryer” since it generates ions to compensate for the charge generated in hairs by combing. Electret charging with this method

**Fig. 2.20** Cross section of the device proposed in [57]. The motion of the proof mass is indicated by the arrow. The proof mass is conductive





**Fig. 2.21** **a** Detail of the device proposed in [56], **b** schematic of the overall device, **c** cross section of the device (suspending beams not shown)

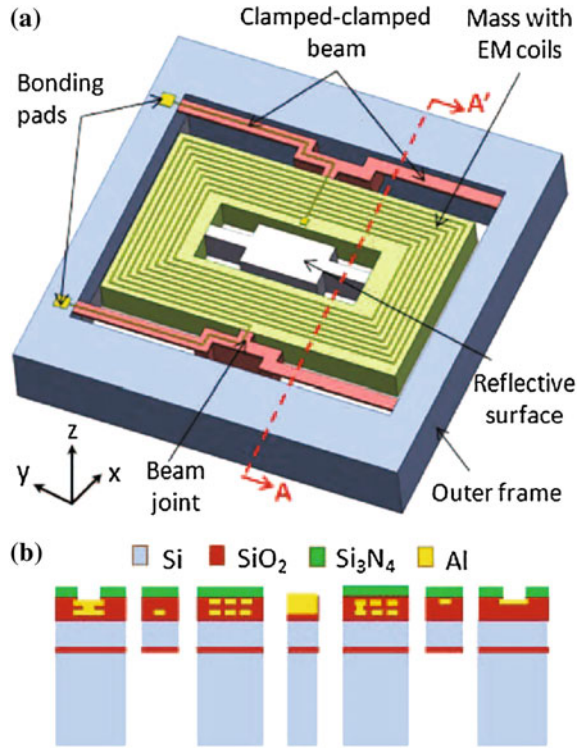
strongly depends on the exposure angle. Nevertheless, the authors are able to charge these vertically placed electrets by exposing them to the air flow for more time.

### 2.4.2 Electromagnetic Transduction

In this kind of transduction, the energy is recovered in coils present in the device as a function of the variation of a magnetic field. The variation of the magnetic field will be due to some vibration mode activated in the structure by the external acceleration from which energy must be recovered.

The authors in [60] propose a device for electromagnetic energy harvesting. This device uses a SOI wafer for which the thickness of the active layer and the bulk of the wafer are  $5\text{ }\mu\text{m}$  and  $400\text{ }\mu\text{m}$ , respectively. The design has two thin clamped-clamped beams connected to a large mass by beam joints, see Fig. 2.22. A cross section of the device can be observed in the same figure. The device presents a two fold objective to increase performance of the device: nonlinear force-deflection characteristic, an amplitude-stiffened Duffing-spring and multi-frequency harvesting mechanisms using different resonant modes of the structure (out of plane  $70.7\text{ Hz}$ , torsion  $85.78\text{ Hz}$  and twist modes  $147.92\text{ Hz}$ ). The electromagnetic harvesting is accomplished by placing a cylindrical magnet on top of the device that generates a magnetic field perpendicular to the surface of the device. The large mass integrates the EM coils that will be used to retrieve the electromagnetic energy. All three modes can generate large beam deflection and stretching strain, generating therefore a nonlinear response of the device.

**Fig. 2.22** Schematic of the electromagnetic harvester presented in [60]. A cross section of the device is shown at the *bottom* of the figure. The thickness of the silicon active layer, used for the clamped–clamped beams is  $5\ \mu\text{m}$  and the thickness of the bulk of the wafer is  $400\ \mu\text{m}$



The expression showing the equivalent force applied in the centre of the clamped–clamped beam of the device is

$$F = \left(\frac{\pi^4}{6}\right) \left[\frac{Ewh^3}{l^3}\right] x + \left(\frac{\pi^4}{8}\right) \left[\frac{Ewh}{l^3}\right] x^3 \quad (2.4)$$

where  $E$  is the Young's modulus,  $w$ ,  $h$  and  $l$  are the width, thickness and length of the beam. The first term is due to the bending strain and produces a linear spring constant, whereas the second term, related to the stretching strain, produces the cubic term. Observing this expression the nonlinear term will be significant for displacements larger than the thickness of the beam [60].

## 2.5 MEMS Devices Based on the Piezoelectric Transduction Mechanism

This section describes the structures, materials and main properties of MEMS based on the piezoelectric transduction mechanism. The piezoelectric properties of materials and a description of the most common piezoelectric materials are included. Sub-

sequently, cantilever beam structure with a tip mass is described due to its wide use in MEMS energy harvesters. The unimorph and bimorph cantilever structures are presented and discussed. Bimorph piezoelectric cantilevers allow higher output power while unimorph piezoelectric cantilevers are more manufacturable. Furthermore, the top-bottom electrodes, TPE, and interdigitated, IDE, and electrodes configurations for unimorph cantilevers are also reviewed. These electrode configurations are used when 31 or 33 modes of piezoelectric materials are required. Finally, an application example of a MEMS-based bimorph energy harvester is illustrated.

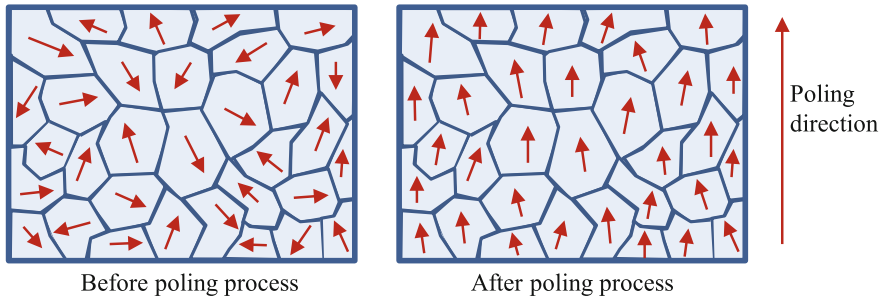
Piezoelectric transduction is an advantageous mechanism to convert vibration-to-electric energy for small scales as stated by Marin et al. [61] and Cook et al. [62]. Marin studied the relationship between the effective material volume ( $v$ ) and the output power for different mechanisms. The output power for the piezoelectric mechanism is proportional to  $v^{3/4}$ , while that for the electromagnetic mechanism is proportional to  $v^2$ . At volumes smaller than  $0.5 \text{ cm}^3$  the electromagnetic transformation factor reduces abruptly [61]. The piezoelectric mechanism has the highest energy conversion efficiency [63, 64] and is the most appropriate technology for the scale of MEMS devices [65, 66].

### 2.5.1 Piezoelectricity

The piezoelectric effect was reported by Jacques and Pierre Curie in 1880 [67, 68]. They found that some kind of crystals subjected to mechanical strain became electrically polarized. Furthermore, they found that the relationship between the degree of polarization and the applied strain is proportional. The inverse piezoelectric effect, these materials deform when a voltage is applied, was predicted by Lippmann [69] and confirmed experimentally by the brothers Curie.

Piezoelectric materials present anisotropic behaviour. Consequently, the properties of the material depend upon the direction of the strain and the direction of the polarization and in particular, on the position of the electrodes. It is important to note that the piezoelectric engineered materials, unlike natural materials, are subjected to a process called poling to impart the piezoelectric behaviour. The dipoles of the cells of a macroscopic crystalline structure are originally randomly oriented and the piezoelectric effect is negligible when the material is subjected to a mechanical stress. The poling process consists of applying a very high electric field that permanently orients the dipoles in the direction of the field, Fig. 2.23.

It is important to avoid the depolarization of the piezoelectric material. There are two ways to de-pole a piezoelectric material: (i) applying a very high electric field opposite to the field applied during the poling process, and (ii) heating the material above its Curie temperature.



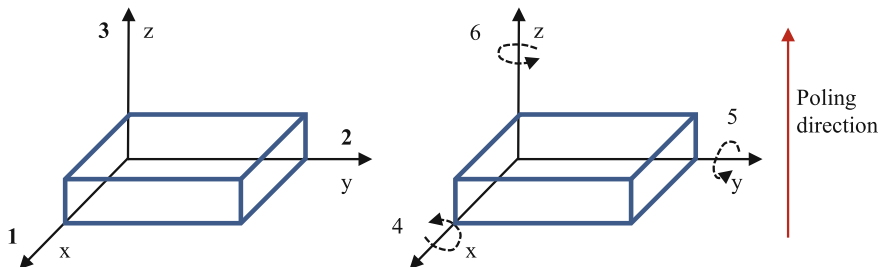
**Fig. 2.23** The poling process induces piezoelectric properties in the material. Before the poling process the dipoles are randomly aligned (*left*). After poling process the dipoles tend to be pointed to poling direction (*right*)

### 2.5.2 Properties of Piezoelectric Materials

The compliance, coupling and permittivity properties for a piezoelectric material are second-order tensors due to the anisotropic behaviour of these materials. As a result, constants defined to characterize the piezoelectric materials have two subscripts, one related to the applied force, stress, and the other related to the change in length, the strain. The specific coordinate system used to indicate the directions of the stress and the strain are shown in Fig. 2.24. Conventionally, the poling direction is the  $z$ -axis (or 3), except in quartz where it is  $x$ -axis (or 1).

As can be seen, the  $x$ ,  $y$  and  $z$  axes are represented by the subscripts 1, 2 and 3, respectively. The subscripts 4, 5 and 6 are used to represent the rotation about these axes.

The constants commonly used to characterize piezoelectric materials are: (i) the piezoelectric strain/charge constant,  $d$ , (ii) the piezoelectric stress/voltage constant,  $g$ , (iii) the electromechanical coupling coefficient,  $k$ , and (iii) the permittivity,  $\epsilon$ .



**Fig. 2.24** Specific notation for coordinates used in piezoelectric constants and quantities. The  $z$ -axis coincides with the poling direction. The numbers 1, 2 and 3 represent the Cartesian coordinates (*left*) and the numbers 4, 5 and 6 represents the shear about Cartesian coordinates (*right*)

The anisotropic piezoelectric mechanical and electrical quantities are linked using double subscripts (i.e.  $k_{ij}$ ). The subscripts designate the axis parallel to the direction of the excitation and the axis parallel to the direction of the response [70].

The strain/charge constants,  $d_{ij}$ , express the relationship between the strain developed along or around an axis and the applied electric field parallel to an axis when all external stresses are constant [71]

$$d_{ij} = \frac{\text{strain developed along } j - \text{axis}}{\text{applied electric field parallel to } i - \text{axis}} \quad \left( \frac{m}{V} \right) \quad (2.5)$$

The strain/charge constant can also be defined as the relationship between the short-circuit charge per unit area flowing between connected electrodes that are perpendicular to an axis and the stress applied along or around an axis when all other external stresses are constant [71]

$$d_{ij} = \frac{\text{short - circuit charge flow perpendicular to } i - \text{axis}}{\text{applied stress along } j - \text{axis}} \quad \left( \frac{C}{N} \right) \quad (2.6)$$

The stress/voltage constant,  $g_{ij}$ , is the relationship between the open circuit electric field developed along an axis and the stress applied along or around an axis when all other external stresses are constant [71]

$$g_{ij} = \frac{\text{open circuit field along } i - \text{axis}}{\text{stress applied along } j - \text{axis}} \quad \left( \frac{Vm}{N} \right) \quad (2.7)$$

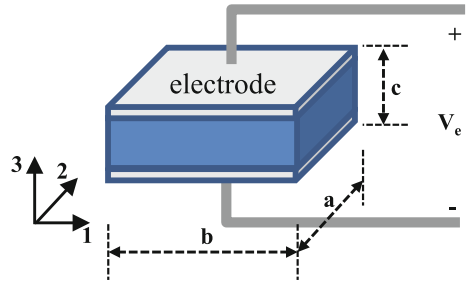
The stress/voltage constant can also be defined as the relationship between the strain developed along an axis and the electric charge density applied to electrodes that are normal to an axis [71]

$$g_{ij} = \frac{\text{strain developed along } j - \text{axis}}{\text{applied charge density normal to } j - \text{axis}} \quad \left( \frac{m^2}{C} \right) \quad (2.8)$$

The electromechanical coupling coefficients,  $k_{ij}$ , are the energy ratios describing the conversion from mechanical energy to electrical energy or vice versa [64]. The ratio of energy stored, mechanical or electrical, to energy, mechanical or electrical, applied can be calculated by squaring the electromechanical coupling factor,  $k^2$ . The first subscript,  $i$ , indicates the direction of the electrical field and the second designates the direction of the mechanical strain. These coefficients have no dimensions. Equation 2.9 shows the relationship between the mechanical input energy in the  $j$ -axis,  $W_j^m$ , and the electrical energy stored in the  $i$ -axis,  $W_i^e$ .

$$k_{ij}^2 = \frac{W_i^e}{W_j^m} \quad (\text{dimensionless}) \quad (2.9)$$

**Fig. 2.25** Piezoelectric material with two electrodes on its opposite sides.  $V_e$  is the voltage across the electrodes and  $a$ ,  $b$  and  $c$  are the dimensions of the piezoelectric element



The most common piezoelectric constants and coefficients used in energy harvesting systems are listed below using the dimensions and the reference system shown in Fig. 2.25.

- $d_{31}$ : This constant represents the relationship between the charge developed,  $Q$ , flowing between the shorted electrodes,  $V_e = 0$  V, that are orthogonal to the poling axis ( $3 - z$ ), and a force,  $F$ , applied along the axis 1. Therefore, the charge developed  $Q$  can be calculated as [72]:

$$Q(V_e = 0 \text{ V}) = d_{31} F \frac{b}{c} \quad (2.10)$$

- $d_{33}$ : This constant represents the relationship between the charge developed,  $Q$ , flowing between shorted electrodes that are orthogonal to the poling axis ( $3 - z$ ), and a force,  $F$ , applied in the direction of the polarization axis ( $3 - z$ ). Therefore,  $Q$  can be calculated as [72]:

$$Q(V_e = 0 \text{ V}) = d_{33} F \quad (2.11)$$

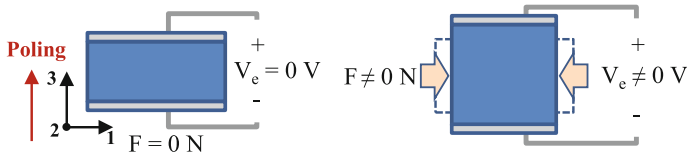
- $g_{31}$ : This constant expresses the relationship between the induced electric field is along the poling axis ( $3 - z$ ) and the force applied in the direction orthogonal to the polarization axis ( $1 - x$ ), Fig. 2.26. Therefore, the induced voltage can be calculated as [72]

$$V_e(Q = 0 \text{ C}) = g_{31} \frac{F}{a} \quad (2.12)$$

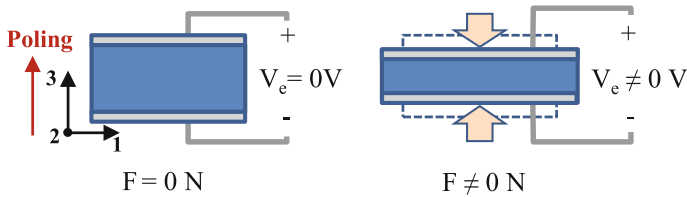
- $g_{33}$ : This constant expresses the relationship between the induced electric field along the poling axis ( $3 - z$ ) and the force applied in the direction of the polarization axis ( $3 - z$ ), Fig. 2.27. Therefore, voltage induced can be calculated as [72]

$$V_e(Q = 0 \text{ C}) = g_{33} F \frac{c}{ab} \quad (2.13)$$

Therefore, the spatial orientation of the materials is very important. It must be taken into account when a system is modelled, analyzed or simulated.



**Fig. 2.26** The 31 mode operation for piezoelectric materials. No voltage is induced when no force is applied (*left*) and voltage is induced when force is applied (*right*)



**Fig. 2.27** The 33 mode operation for piezoelectric materials. Effect when no force is applied (*left*) and voltage is induced when force is applied along the poling axis (*right*)

### 2.5.3 Piezoelectric Materials

Piezoelectric materials are used in a range of applications such as pressure sensing, data storage, mechanical actuation, ultrasonic wave generation and energy harvesting. Owing to this wide range of applications, a large number of materials have been developed. The following classification includes the most available forms of piezoelectric materials [73, 74]:

- Crystals: Quartz ( $\text{SiO}_2$ ), Berlinitz ( $\text{AlPO}_4$ ), Gallium Orthophosphate  $\text{GaPO}_4$ , Turmaline, etc.
- Polycrystalline ceramics: Barium titanate ( $\text{BaTiO}_3$ ), Lead Zirconate Titanate (PZT) [75]. These materials are characterized by its perovskite tungsten-bronze structure.
- Thin film non-ferroelectric materials: Sputtered zinc oxide (ZnO), Aluminium Nitride (AlN) [76].
- Polymeric materials: Polyvinylidene fluoride (PVDF) [77].
- Screen printable thick-films based upon piezoceramic powders [78] and composites such as polyvinylidene-trifluoroethylene-PZT (PVDF-TrFE) [79]
- Organic crystals: single-crystal diisopropylammonium chloride (DIPAC) and diisopropylammonium bromide (DIPAB) [80, 81]

MEMS devices require thin and thick film technologies since the layers of the materials must be below  $100\text{ }\mu\text{m}$ . Thin-film technologies, physical or chemical deposition, are used to fabricate films with thickness lower than  $5\text{ }\mu\text{m}$ . Thick layers with thickness up to  $100\text{ }\mu\text{m}$  can be fabricated using the screen printing method. Maas et al., [82], describe PZT printing onto silicon, the powdered PZT is mixed with borosilicate glass powder and an organic vehicle to make a paste, it is the ink. The

**Table 2.1** Coefficients of common piezoelectric materials [64, 84–86]

Property	PZT-5H	PZT-5A	BaTiO <sub>3</sub>	PVDmF	AlN	GaN	ZnO
$d_{33}$ ( $10^{-12}$ C N <sup>-1</sup> )	593	374	149	−33	5	3.7	12.4
$d_{31}$ ( $10^{-12}$ C N <sup>-1</sup> )	−274	−171	78	23	−2	−1.9	−5
$g_{33}$ ( $10^{-3}$ V m N <sup>-1</sup> )	19.7	24.8	14.1	330	−	−	−
$g_{31}$ ( $10^{-3}$ V m N <sup>-1</sup> )	−9.1	−11.4	5	216	−	−	−
$k_{33}$ (dimensionless)	0.75	0.71	0.48	0.15	0.23	−	0.48
$k_{31}$ (dimensionless)	0.39	0.31	0.21	0.12	−	−	0.182

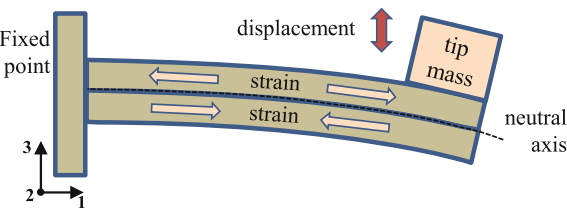
layer is printed, dried to remove the solvent and finally fired. The aluminium nitride, AlN, has recently been included on the list of materials used in energy harvesting. Schaijk et al. justify the selection of AlN as piezoelectric material as it is easier to process than PZT [83]. The piezoelectric constants of PZT are better than AlN but the main advantage of AlN is its compatibility with CMOS processing. This is because it is foreseeable that in the near future, new investigations will result in better performance devices based on AlN. Finally, the piezoelectric constants for common materials used in MEMS devices are shown in Table 2.1.

**2.5.4 Piezoelectric Energy Harvester**

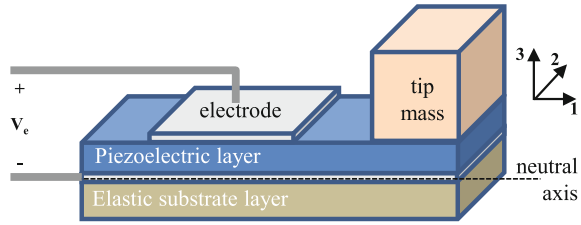
Energy harvesting MEMS devices based on piezoelectric materials generally have a cantilever beam structure as shown in Fig. 2.28. The beam is clamped at one end and the mechanical vibrations are generated principally along the third axis through bending. As can be seen, the vertical movement of the mass induces a strain along the x-axis (or 1). Accordingly, if a 31 mode piezoelectric material is deposited on the beam, then a voltage would be induced between the two sides of this material when it is exposed to vibration sources.

The structure shown at Fig. 2.28 creates equal and opposite strains on the beam. Therefore, it is not possible to use a beam based only on a piezoelectric material as the total voltage or current generated would be null. To be effective as a generator a piezoelectric layer is fixed to a non-piezoelectric elastic layer, Fig. 2.29. Thereby the

**Fig. 2.28** Cantilever beam structure with a tip mass subjected to bending. The strain developed above the neutral axis is opposite to the strain developed below the neutral axis



**Fig. 2.29** The unimorph structure based on a piezoelectric layer and a inactive substrate. The generated voltage,  $V_e$ , depends only on the strain on the piezoelectric layer

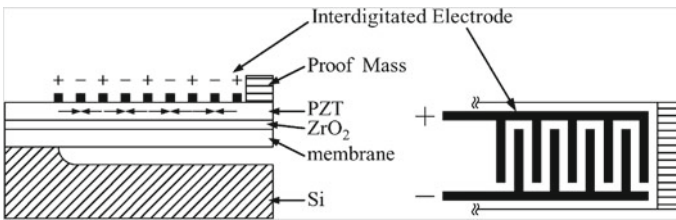


neutral axis, the line in which the beam does not change in length, is not in the centre of the piezoelectric layer. This structure is named unimorph because it is composed of a unique piezoelectric active layer.

The 33 mode of piezoelectric materials is often more favourable than 31 mode, see Table 2.1. This would be a reason to use this mode but the structure shown at Fig. 2.29 is not feasible as the direction of the induced electric field in 33 mode is parallel to the stress direction. The interdigitated electrode, IDE, configuration presented by Jeon et al. at [66] and Park et al. at [87] enables one employ the 33 mode and discards the bottom electrode layer, Fig. 2.30.

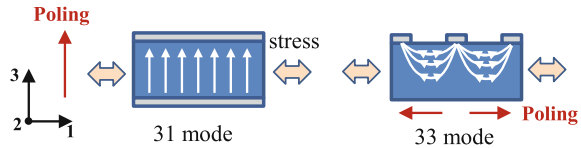
IDE configuration has the additional advantage of allowing a designer adjust the electrode spacing and, consequently, output voltage since the open circuit voltage is proportional to the distance between electrodes, see Eq. 2.13. A comparison between the structures proposed using the 31 and 33 modes is shown in Fig. 2.31.

Therefore, the electrode lengths and shapes are important parameters that affect the output voltage due to the nonuniformity of the strain along the beam [88]. Kim et al. have fabricated and compared piezoelectric energy harvesters based on  $d_{31}$  and  $d_{33}$  modes [89]. These authors have demonstrated that the output power of the  $d_{33}$  mode depends strongly on the dimensions of IDE.



**Fig. 2.30** Structure of the unimorph cantilevered beam with interdigitated electrode proposed by Jeon et al. [66]

**Fig. 2.31** Relationship between applied stress and induced field, white arrows, for 31 and 33 modes



## Bimorph Cantilever Structure

The structure of a bimorph piezoelectric energy harvester based on a cantilever beam is shown in Fig. 2.32. Two piezoelectric layers are fixed to a non-piezoelectric elastic layer. The electrodes can be connected in series or in a parallel configuration. The main advantage of a bimorph structure is that there is a lower loss in the mechanical support materials since only the piezoelectric layer is strained.

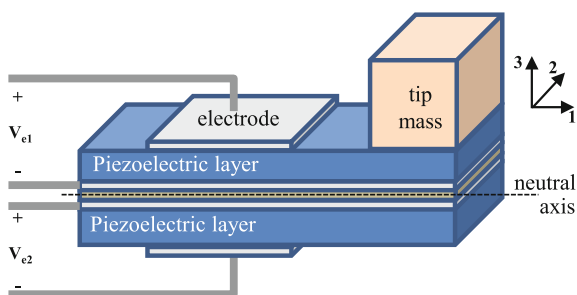
Currently, the optimization of energy harvesters is one of the most important challenges due the low energy extracted. In order to analyze and optimize designs, several models of the piezoelectric energy harvesters have been proposed. Lumped-parameter models allow simple expressions but with limited accuracy. Models based on distributed-parameters offer higher accuracy, increasing the complexity of the expressions. Erturk et al. at [90] present a detailed electromechanical modelling of piezoelectric energy harvesters.

## Application Example

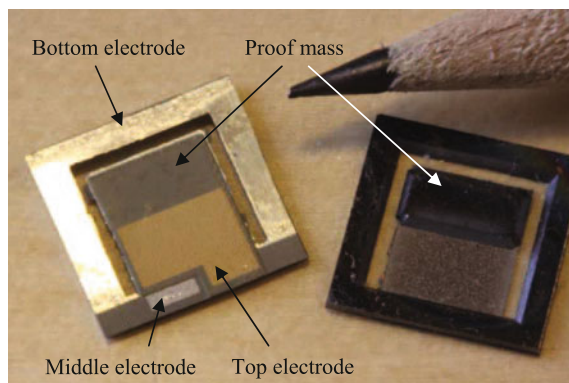
A MEMS vibration energy harvester based on a PZT/PZT thick film bimorph with an integrated silicon tip mass is described in [91], Fig. 2.33.

The authors propose a new fabrication process that improves the quality of the thick film. The PZT layers are screen printed, treated with a high pressure process and finally sintered (high-temperature heating without melting the material). The

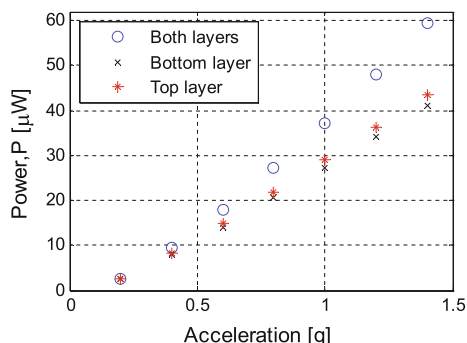
**Fig. 2.32** Structure of a bimorph piezoelectric energy harvester



**Fig. 2.33** Front and back of a MEMS-based PZT/PZT thick film bimorph vibration energy harvester fabricated by R. Xu et al [91]



**Fig. 2.34** RMS power output as a function of the input acceleration [91]



characterization of the power output as a function of the acceleration is shown in Fig. 2.34. The output power reaches 37.1,  $\mu\text{W}$  when the energy harvester is subjected to an acceleration of 1 g. It is important to denote that the power output due to the bottom layer and the power due to the top layer are very similar.

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