

Chapter 2

Copper-Based TSV: Interposer

Sebastian Killge, Volker Neumann, and Johann W. Barthä

2.1 Introduction

Through-silicon via (TSV) fabrication consists mainly of the following steps: etching, deposition of insulator, deposition of barrier and seed layers, and electrochemical plating. Depending on the application, the TSV structures differ in size, aspect ratio, density, materials, and technology. Each application has its own requirements which affect the whole processing scheme. The most important parameters for TSV fabrication are aspect ratio and contact density. Their values are specific to each application.

In this chapter, we present a specific process flow for a TSV—interposer realizing through holes down to a diameter of 10 μm . The fabrication of interconnect is carried out as a through-hole connection. In contrast to the blind hole via integration schemes, the TSVs are etched through to an etch-stop layer. Thus, no grinding, polishing, or etch back processes have to be applied later as it is required in blind hole via integration schemes. Since the fabrication aims at interposer fabrication, no active devices and thus, no restrictions in the thermal budget have to be considered. The complete process flow consists of the following steps and is schematically pictured in Fig. 2.1:

1. The fabrication process is started with a blank silicon wafer. A substrate thickness of 200 μm is chosen as a trade-off between an attainable aspect ratio for deep silicon etch and via fill. Also, a removable stop layer is deposited for

S. Killge (✉) • V. Neumann • J.W. Barthä
Technische Universität Dresden, Institute of Semiconductors and Microsystems - IHM,
01062 Dresden, Germany
e-mail: sebastian.killge@tu-dresden.de; volker.neumann@tu-dresden.de;
johann.bartha@tu-dresden.de

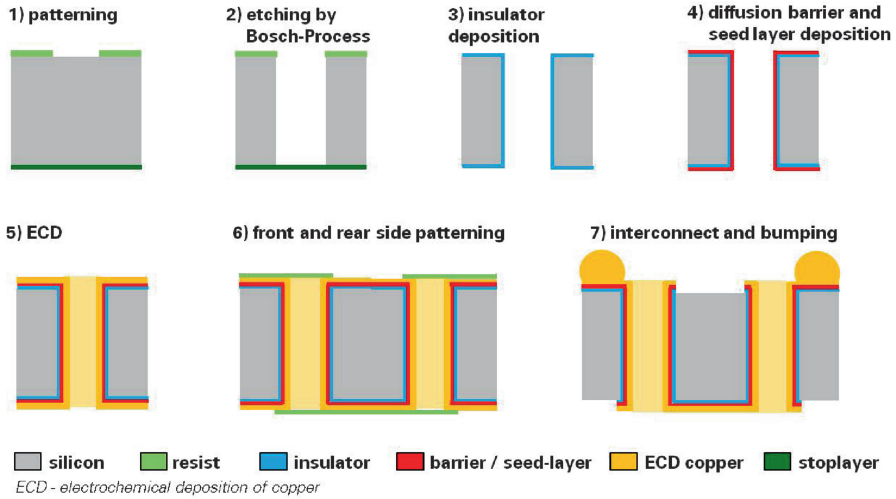


Fig. 2.1 TSV process scheme for thinned wafer with a thermal oxide layer as rear side etch-resist

the subsequent deep reactive ion etch process¹ and a full lithography step is performed to create a photoresist masking layer for the subsequent deep reactive ion etch process.

2. The TSVs are formed by means of deep reactive ion etching. The photoresist and the polymeric sidewall passivation layers created during DRIE processing are stripped wet-chemically. The stop layer is removed by an additional wet-etch process. Furthermore residual polymer is removed and the sidewalls are smoothed by reactive ion etching in an oxygen-nitrogen trifluoride plasma.
3. To prevent leakage between different interconnects, an insulating silicon dioxide layer is grown by thermal processing. Moreover, this process also functions as an annealing process to minimize stress in the crystal lattice caused by the etching process.
4. The diffusion barrier layer and a ruthenium (Ru) seed layer are deposited in situ by atomic layer deposition (ALD).
5. The TSVs are either filled or just enhanced with copper in an electrochemical plating process.
6. Front and back side lithography is used to generate the metallization layer mask for the subsequent patterning processes.
7. The copper layer is structured in a wet etching process and the redistribution lines on the front and back side of the wafer are created by pattern plating. The seed and the barrier layers are removed afterwards in a plasma etch process. In a waferbumping process, SnAg or PbSn solder bumps are fabricated by electrochemical deposition (ECD) and reflow.

¹ The properties of different stop layers are investigated in Sect. 2.2 of this chapter.

2.2 Deep Reactive Ion Etching

Deep reactive ion etching (DRIE) is widely used to generate MEMS structure, capacitors for deep-trench DRAM, and for fabrication of TSVs. It is an extension of the RIE process, which is a highly anisotropic etch process that is used to generate straight (90°) etch profiles, steep trenches or holes (generally with high aspect ratios) in a substrate. In general, DRIE can be either isotropic or anisotropic. There are two methods available to control isotropy in DRIE: cryogenic and Bosch. In cryogenic DRIE, the wafer is cooled to -110°C ($+163\text{ K}$) to slow down the chemical reaction leading to isotropic etching and generate a sidewall passivation [1]. The second and well-established option is the Bosch DRIE process. It was developed in 1994 at Robert Bosch GmbH [DE 4241045 C1] [2]. This etching process is performed by cycling between a deposition (C_4F_8) and an etching (SF_6) step and is also known as time multiplexed or pulsed etching. It consists of:

1. Application of a chemically inert passivation layer by plasma induced deposition of a polymer layer using C_4F_8 as feed gas.
2. Anisotropic removal followed by isotropic Si chemical etch; SF_6 is generally used for etching of Si.

As shown in Fig. 2.2 initially, the polymeric passivation layer covers the resist, the entire structure, and sidewalls and prevents further chemical attack. In the following etching step first the ionic fraction of the plasma assists to remove the passivation on vertical surface (trench bottom) after that the trench bottom is etched isotropically. The isotropic etching is performed for a few seconds, usually with a fluorine based gas (SF_6).

This is followed by a deposition step lasting a few seconds, in which the pattern is again covered with a uniform polymeric layer. Then the etching cycle is repeated. Due to the direction of the accelerated ions, the polymeric layer is removed much faster on vertical surfaces than on horizontal surfaces. For the rest of the etching cycle, further etchants start etching the surface vertically, simultaneously the chemically inert polymer layer keeps the sidewalls from further etching and hence the lateral etching or isotropic etching component is substantially reduced. These etching/deposition steps are repeated several times to achieve the required etch depth. The plasma is generated by an inductive plasma source, while the ion bombardment on the substrate is controlled by a capacitively coupled RF power applied to the susceptor plate. Each step contains a significant number of parameters controlling the process properties like gas flows, the power of the inductively coupled plasma or the platen source, time, etc. The optimized etching profiles with slightly positively tapered angles are generated by careful balancing between the two steps.

The advantage of the passivation layer is that the width of a trench can be confined to a certain extent. Otherwise, without the passivation step, the isotropic

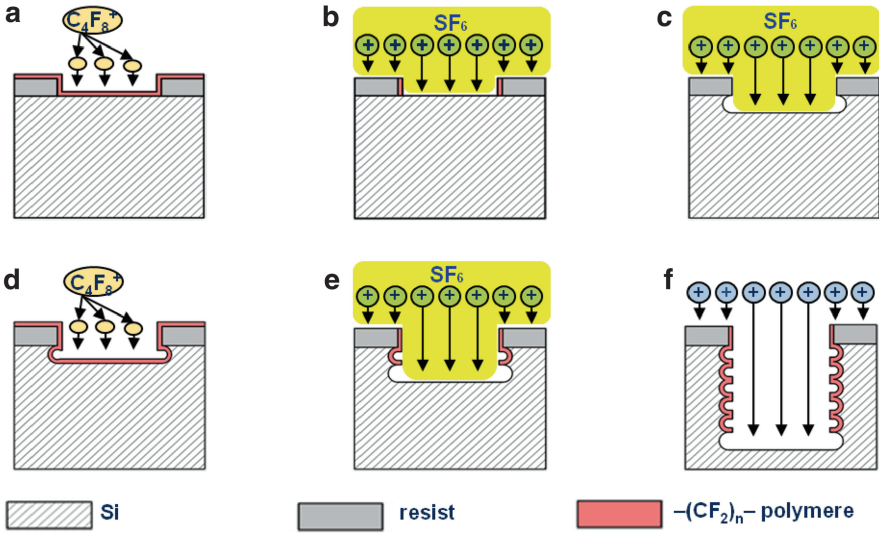
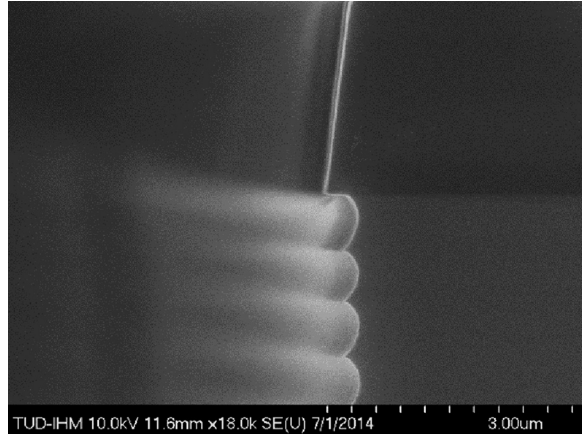


Fig. 2.2 Bosch process scheme. (a) Deposit a conformal C_4F_8 passivating layer; (b) directed removal of the passivation layer by ions; (c) isotropic etching with SF_6 ; (d) deposit a conformal C_4F_8 passivating layer; (e) pass. removal and isotropic etching; (f) alternating steps (b)–(e)

Fig. 2.3 Bosch scallops created by alternating isotropic passivation and anisotropic opening of the trenches bottom



etching can lead to very high lateral etching, resulting in very broad open structures. Nevertheless this effect can be used for diameter enlargement of the structures in the upper region near the opening.

The cyclic approach using isotropic chemical etching alternating with isotropic passivation and anisotropic opening of the trenches bottom creates a characteristic sidewall shape with a waved profile. These waves are also referred to as *scallops* (Fig. 2.3). The challenge in DRIE is to generate TSVs with a low surface roughness (scallops), a low tilt of the vias, and easily removable CF-polymers residues.

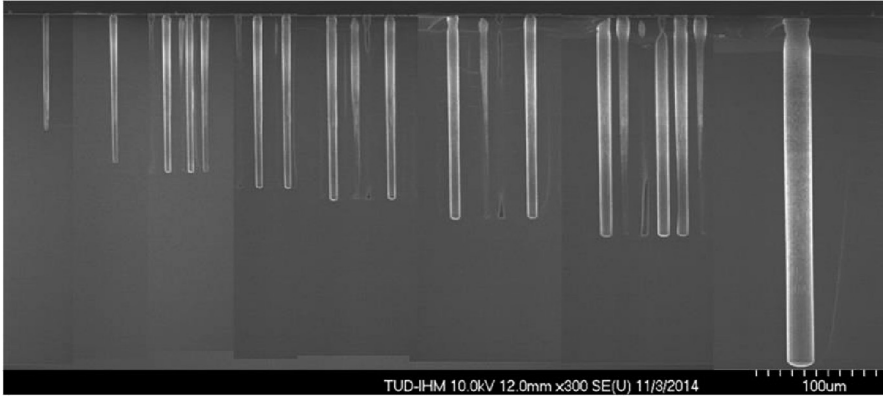


Fig. 2.4 SEM pictures of the etch rate depending on the dimensions of a feature varying for 5–40 μm TSV fabrication in one etching process

Overall, the sidewall roughness is very critical and should be as low as possible to minimize its impact on the subsequent deposition steps. Indeed, high surface roughness causes a much greater area to be coated, and therefore the coverage of the following layers has to be increased. In addition, residues of CF-polymer may attach to the TSV sidewalls. Another important point is that the etch rate depends on the structure diameter. Thus, it is not possible to etch structures with different diameters or opening surfaces to the same depth.

Dependence of etching on aspect ratio is sometimes called *RIE lag* as it describes the impact of feature dimensions on each rate [3]. This is especially important when features of different dimensions are etched simultaneously. Because of *RIE lag*, smaller structures will be etched slower than larger structures. Figure 2.4 shows the varying etching rate for 5–40 μm TSV fabrication in one etching process.

At the Institute of Semiconductor and Microsystems (TU Dresden), an STS Pegasus machine is used. This is a high-rate-etching machine that is very well suited for fabrication of deep TSVs. The control of the alternating etching and deposition step is the basis to improve the result. As mentioned before, each step consists of a huge range of parameters to control the etching result. To obtain a high uniformity of the etch depth all over the wafer, it is necessary to obtain a highly uniform plasma density which can be controlled with specific fields around the plasma bulk.

Figure 2.5 shows results for optimized process on the STS Pegasus. It is possible to generate TSVs with tapered profiles up to an aspect ratio of 30:1 with low surface roughness. Those TSVs are manufactured with two etching processes. At first, the via is etched to the desired depth. This first process step creates a so-called undercut which is a negative profile in the first 5 μm etching depth. The undercut has to be removed by a second process, because the negative profile makes it difficult to deposit continuous electrical insulator, diffusion barrier and seed layers. The TSVs of the optimized process (Fig. 2.5) have a lower surface roughness at the bottom and in the middle. In the TSVs from the initial test, pillar formation was found.

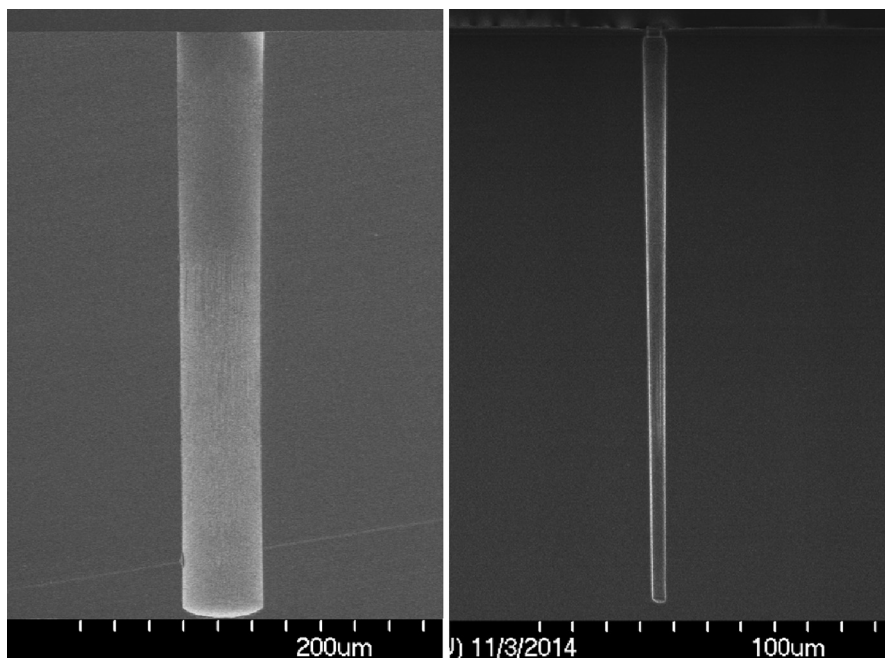


Fig. 2.5 SEM pictures of the etching results at STS Pegasus DRIE. *Left:* 40 μm diameter; 400 μm deep, AR 10:1. *Right:* 6 μm diameter; 187 μm deep, AR 30:1

The pillar formation is a defect in the TSV sidewalls where the CF-polymer passivation of the TSV sidewalls is burst in the etching cycle and a parasitic etching behind the sidewalls appears.

In the optimized process the pillar formation could be reduced to a minimum. The optimized parameters guarantee a sidewall surface roughness of 20–100 nm at maximum. The integration scheme for the fabrication of the TSV interposer using 200 μm thin wafers enables the creation of through-hole VIAs without additional wafer thinning. Therefore, the etching process must be reliably stopped on the wafer back side without impact on the TSV geometry or the sidewall roughness. Since the temperature control at the wafer relies on He-back side cooling (thin He-gas buffer between wafer susceptor and wafer) the TSV-hole etching must stop on a thin membrane as stop layer.

Applying a photoresist as stop layer is one of the simplest ways to realize this. Spin-coating and bake-out process of the stop layer are carried out prior to the lithography step, which is performed to create the masking layer on the front side of the wafer. However, commonly used photoresists are insulating and the cleaning of the trench bottom after the passivation step requires ion bombardment approaching perpendicular to the surface. An insulating layer will charge up the surface positively and deflect the ions creating a thinning of the sidewall passivation close to the trench bottom and by this a widening of the structures referred to as “notching” (shown in Fig. 2.6).

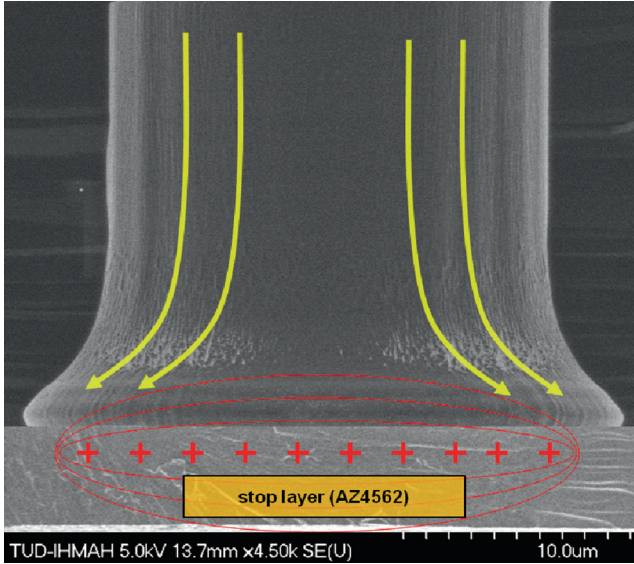


Fig. 2.6 Notching created by released ion bombardment and back side stop layer charging on trench bottom

So notching is an effect of lateral etching which occurs in high-density plasma etching when approaching a stop layer [4]. The phenomenon is caused by two co-occurring events:

1. The extinction of etching due to the appearance of the non-etchable stop layer causes a gain in radial concentration.
2. The charge accumulation in an insulating stop layer material. The latter is accompanied by an electric field, which then deflects all further impinging ions onto the sidewall of the TSV.

One approach to minimize the notching effect is the application of conductive stop layers [5]. The material commonly used is aluminum [6], which has been the standard material for metallization layers in CMOS fabrication for many years [7]. This greatly simplifies the application since the deposition and etch processes are easily available. In general, film thicknesses of few microns are chosen in order to ensure a sufficient mechanical stability [6, 8].

Besides the prevention of sidewall notching during DRIE, a most important requirement of the etch-stop layer is the ease with which the material is removed subsequent to the TSV formation. In our case an aluminum film thickness of only 50 nm is deposited, and mechanical stability is provided by applying an additional photoresist layer of 5 μm thickness onto the aluminum layer (Fig. 2.7).

As mentioned above, the bad adhesion of polymer layers on the surface has a negative influence on the subsequent films, thus increasing the likelihood of delamination. Furthermore, pillar formations are found that are partly due to

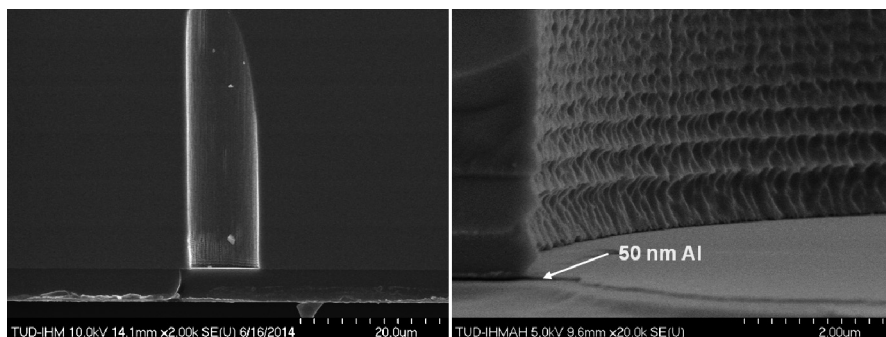


Fig. 2.7 SEM of etched TSV (20 μm diameter, 200 μm length) at the bottom of the etch-stop layer after DRIE, detailing minimal notching on 50 nm of Al-stop layer

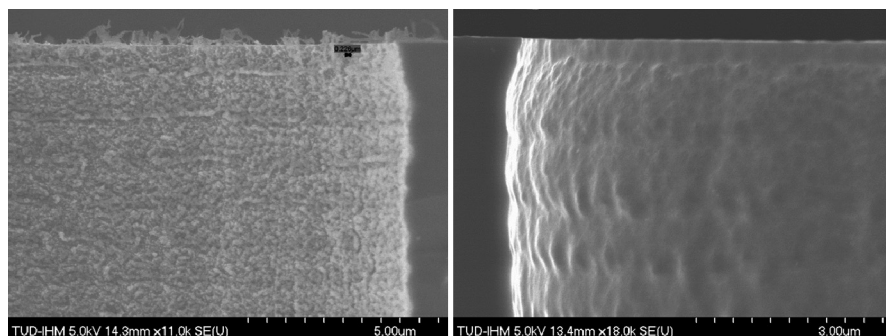


Fig. 2.8 SEM pictures before and after plasma-enhanced smoothing, using oxygen (O_2), argon (Ar), and nitrogen trifluoride (NF_3) (max. 20 nm surface roughness at TSV sidewall, 20 μm diameter, 200 μm length)

polymer residues. Their bad adhesion to the via walls often results in delamination of subsequently deposited layers as well. The optimized process reduces the CF-polymer residues. Proper cleaning procedures are necessary and can be employed in two ways: dry plasma or wet chemical cleaning. For the wet chemical step the use of 1-methyl-2-pyrrolidone (NMP) or nonafluoro-4-ethoxy-butane (F7200) is being investigated. In a dry plasma-enhanced cleaning the residual polymer is removed and the sidewalls are smoothed by reactive ion etching in an oxygen-nitrogen trifluoride plasma (Fig. 2.8). The optimized parameters of the wet chemical and dry plasma cleaning steps guarantee a sidewall surface roughness of only 20–100 nm at maximum.

The next step after the generation of the TSV is an enlargement of its diameter in the upper region near the opening. The TSVs are thus manufactured with two subsequent etching processes. At first, the via is etched to the desired depth. This first process step creates a so-called undercut which is like a negative profile in the first 5 μm etching depth. The undercut has to be removed by a second process,

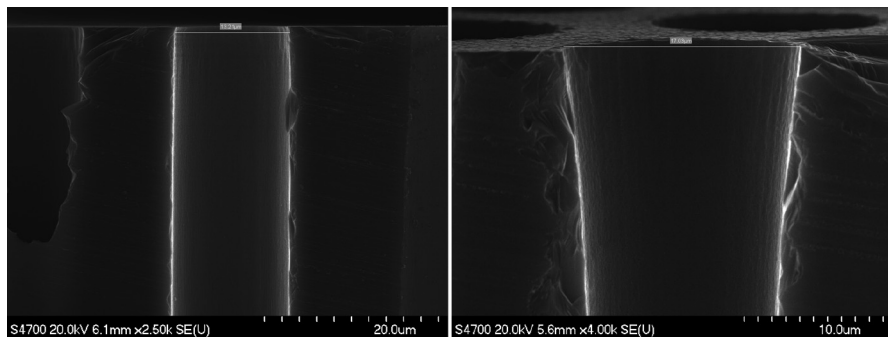


Fig. 2.9 Removal of the undercut and profile enlargement for tapered TSV by an additional etching step. *Left:* before removal of the undercut. *Right:* after the additional etching for tapered profiles

because the negative profile makes it difficult to deposit a continuous electrical insulator, diffusion barrier and seed layer by conventional deposition techniques. On the one hand, tapered profiles reduce the contact density on the chip. On the other hand, positive profiles make it easier to get good sidewall coverage with subsequent deposition steps (Fig. 2.9). The removal of the undercut is an important prerequisite for good deposition conditions in the PE-CVD, PVD metallization, and ECD steps.

In summary of TSV etching, we can state that by etching to a conductive stop layer, it is possible to fabricate interposer TSV using $200\mu\text{m}$ thin wafers. This allows the creation of TSV structures with diameter sizes ranging from less than $10\mu\text{m}$ up to more than $40\mu\text{m}$ without any additional wafer thinning process (Fig. 2.10).

2.3 Insulator, Diffusion Barrier- and Seed-Layer Deposition

The fabrication step following the silicon etching of the TSV is the deposition of insulator, barrier and seed layer. The metallization consists of Cu and is applied by ECD. Since Cu has a high diffusivity in silicon as well as in silicon oxide it requires a defect free conformal barrier layer which simultaneously serves as adhesion or wetting-layer and a conformal conducting layer which serves as starting or seed layer for the ECD process. The fabrication of TSVs with aspect ratios exceeding 10:1 clearly limits the application of conventional deposition processes. Indeed, the production of high aspect ratio TSV requires deposition process enabling the deposition of homogeneous layers on large aspect ratios. In principle, three different deposition processes with a variety of materials are available: physical vapor deposition (PVD), chemical vapor deposition (CVD), and ALD. Depending on the deposition process, the coverage in the high aspect ratio structures can be very inhomogeneous, with increasing loss in film thickness when approaching the trench

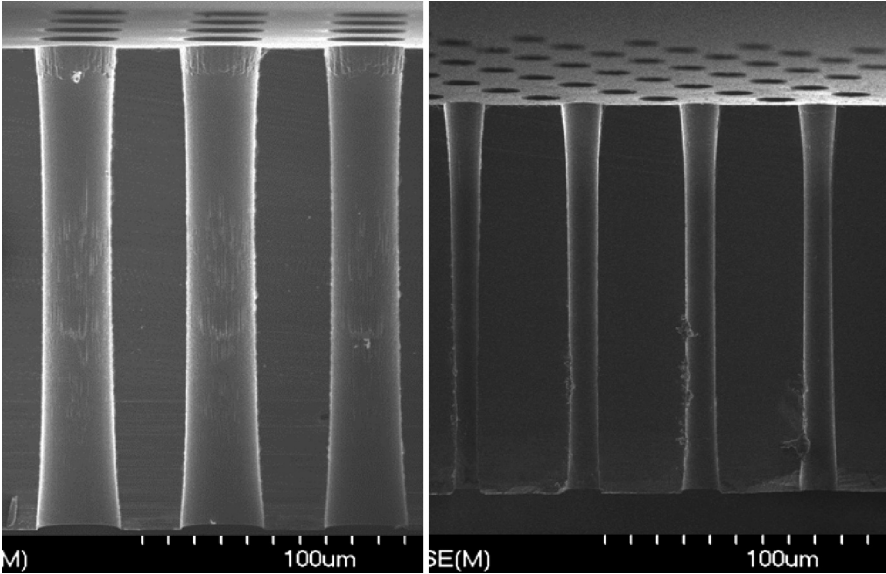


Fig. 2.10 SEM after silicon via etching onto a stop layer releasable afterwards and additional enlargement of TSV diameter on wafer front- and back-side. *Left:* 20 μm diameter, 200 μm TSV length. *Right:* 10 μm diameter, 200 μm TSV length

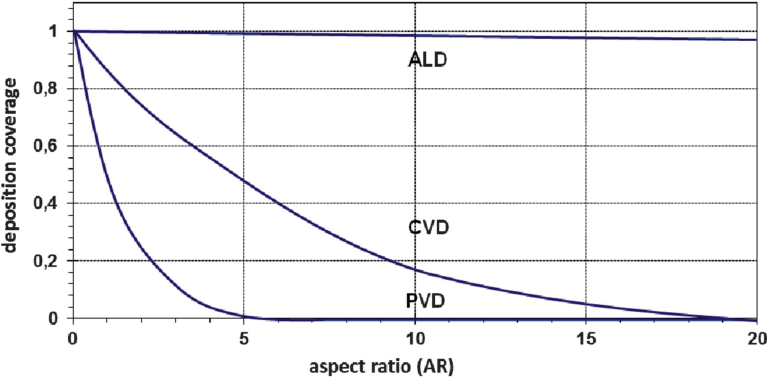


Fig. 2.11 Schematic graph of deposition coverage in comparison of PVD, CVD, and ALD deposits process

bottom. The film appears discontinuous and does not serve as insulator, barrier or seed layer any more. As shown in Fig. 2.11 the capability to coat trench or a TSV sidewalls by several deposition processes is limited. The step coverage of an optimized process for the TEOS-based plasma-enhanced CVD of silicon dioxide into TSV structures decreases below 30 % for aspect ratios larger than 2.5:1 [9]. Similar values constrain the use of conventional PVD processes for the deposition

of barrier and seed layer [10]. The AR limits for the different deposition techniques are as follows: PVD, $AR \leq 5:1$; CVD, $AR \leq 15:1$; ALD, $AR \geq 10:1$.

2.3.1 Insulator Deposition

An insulation layer, e.g., SiO_2 , is necessary to ensure proper electrical functionality of the TSV. After enlargement of the TSV diameter, the rough inner surface of the vias (≤ 100 nm) is smoothed by a plasma-enhanced chemical vapor deposition (PE-CVD)-TEOS (tetraethylorthosiloxane) process which is required for the electrical insulation of the through contacts. CVD techniques are based on the chemical reaction between the precursor reactants of the gas phase stream and the surface of the substrate or the chemical decomposition of the precursor reactants above the substrate, after which they get adsorbed at the substrate surface. In both cases the adsorbed reactants diffuse along the surface until they find an energy-favorable bonding spot. This is where the film is formed. The by-products of the reactions desorb and are pumped out with the gas stream.

The insulator deposition is carried out as low pressure PE-CVD by means of a microwave assisted ECR-concept (2.45 GHz). It is dependent on the aspect ratio as well. Sufficient step coverage for ARs from 5:1 up to 15:1 was achieved (Fig. 2.12) and the process temperature of around 340 °C resulted in low carbon content of the CVD films. The typical breakdown voltages of the insulator layer range from 9 up to 10 MV/cm.

An alternative to PE-CVD of TEOS is the thermal oxidation of the silicon wafer. A thermal oxide insulator layer offers better film properties, including better electrical and optical properties. In contrast to the PE-CVD of TEOS, the deposition rate in thermal oxidation does not depend on the aspect ratio and the layer thickness of the insulator is constant on the whole wafer. For thermal oxidation an oxidizing agent diffuses to the SiO_2/Si interface at high temperature and reacts with the Si substrate. Thermal oxidation of silicon is usually performed at a temperature between 800 and 1200 °C. Thermal oxide is based on a chemical reaction of oxygen and silicon, and requires the diffusion of the oxidant through the already grown SiO_2 to the unreacted Si surface. Here, the silicon is converted by the oxygen to silicon oxide. So there is no layer deposited onto the substrate, but the silicon is “consumed.” For every unit thickness of silicon consumed, 2.27 unit thicknesses of oxide will appear. If a bare silicon surface is oxidized, 44 % of the oxide thickness will lie below the original surface, and 56 % above it.

To achieve homogeneous layers by thermal oxidation, the TSV must be free of polymer residues and has to have low surface roughness. Thermal oxidation enables the generation of a uniform insulator layer thickness (1 μm or more) on the sidewalls of the TSV irrespective of the aspect ratio. The oxide thickness is proportional to \sqrt{t} where t is the oxidation time. Therefore a thickness of 2 μm appears as a practical limit since even at a maximum furnace temperature of 1100 °C, it takes more than

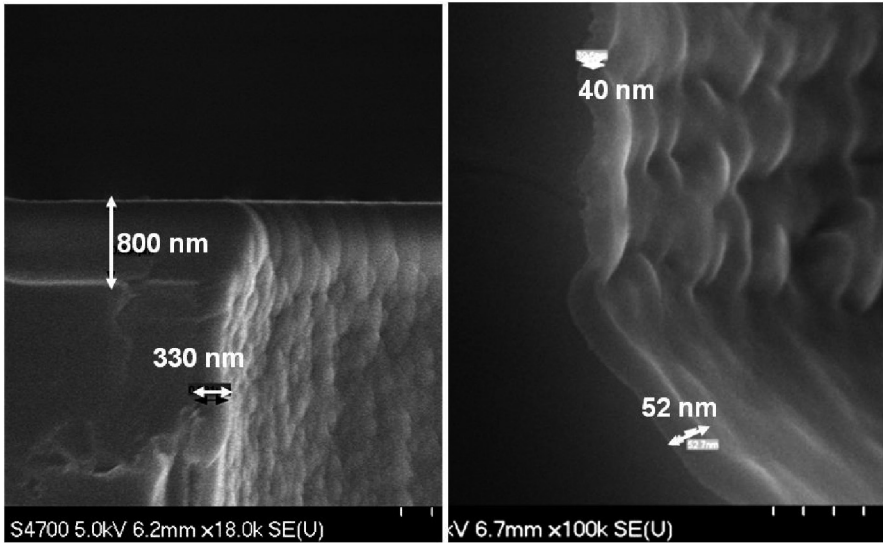


Fig. 2.12 PECVD TEOS-SiO₂ 800 nm. *Left:* TSV-diameter = 10 μ m depth 95 μ m details: 330 nm on sidewall top. *Right:* TSV-diameter = 10 μ m depth 95 μ m details: 40 nm on sidewall bottom

8 h to grow 2 μ m. It is important to mention that thermal oxidation is applicable to an interposer and trench-first scheme but is not applicable for a trench-middle or trench-last process flow.

2.3.2 Atomic Layer Deposition

The TSV geometry generally has high aspect ratio (AR) due to the fact that the TSV required area needs to be minimized. As alluded to before, the challenges associated with high-AR TSV are the DRIE process and the material deposition on the TSV sidewalls. As shown in Fig. 2.11 and discussed before, the capability to coat trench sidewalls by PVD or CVD is limited. An exceptional technology in this respect is ALD.

ALD is a special kind of heterogeneous CVD technology based on a self-limiting monolayer chemisorption of a precursor gas according to a kind of Langmuir adsorption isotherm. This is followed by exposition of the substrate to a second gas reacting with the absorbent to the desired material, enabling again the self-limiting chemisorption of the first precursor [11]. The dosing of the different gases is separated by purging the deposition chamber with inert gas to avoid gas phase (homogeneous) reactions. To grow the desired film, the four-step sequence (Precursor 1-purge-Precursor 2-purge) is applied in a cyclic way (see Fig. 2.13). The growth per cycle is typically less than an Angstrom. Due to limitations in the

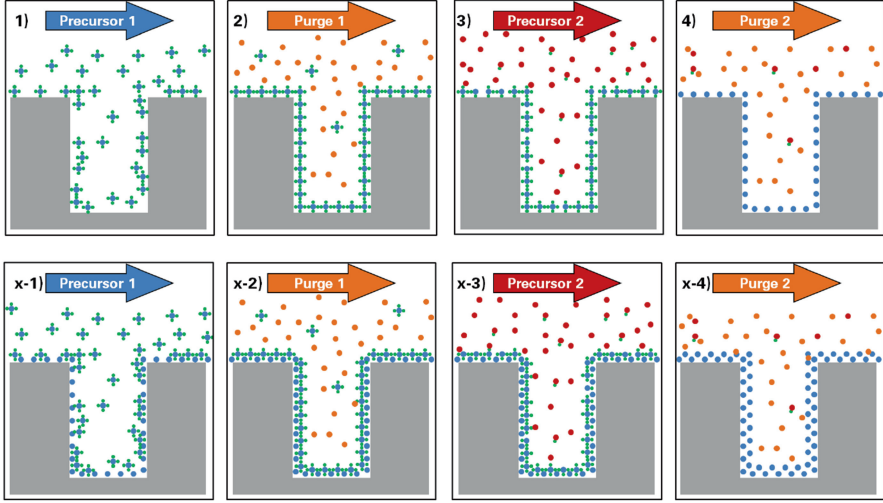


Fig. 2.13 ALD process phases

adsorption site density or the limited capability to access sites that are blocked by the relatively large organometallic precursor (steric hindrance), the amount of adsorbed effective material is less than a monolayer. Therefore this technique is specifically well suited for the growth of very thin films of a few nanometers.

The described process scheme is generally valid for the so-called homogeneous growth regime considering a layer-by-layer growth of a material on itself. Starting the growth of a material on a different substrate requires a nucleation process that may result in a layer-by-layer mode or in an island formation. The growth can be substrate enhanced or inhibited [12]. It might require up to several hundred ALD cycles to initiate a film growth. Based on the self-limiting adsorption mechanism, the ALD technique shows unique step coverage and a superior uniformity. An improvement of the step coverage is generally possible by extending the exposure time, allowing the precursor more time to find accessible unoccupied adsorption sites.

In relation to the TSV process, ALD could be used to grow the insulator film. However, to avoid parasitic capacitances, the insulator film should be thick, which would take a long time using ALD. Instead, as explained before, thermal oxidation is used of the insulator film. On the other hand, for the copper barrier ALD would be an excellent choice. It is also the adopted choice for the seed layer needed for copper electroplating [13, 14]. Since an ALD process for copper is not available, we have chosen ruthenium (Ru) as seed layer and tantalum nitride (Ta₂N₅) as barrier material. The properties of these materials are generally known [15, 16]. The major limitation of ALD is its low deposition rate of less than a monolayer per cycle. In particular, the Ru process is hampered by an initial growth delay of about 15 cycles.

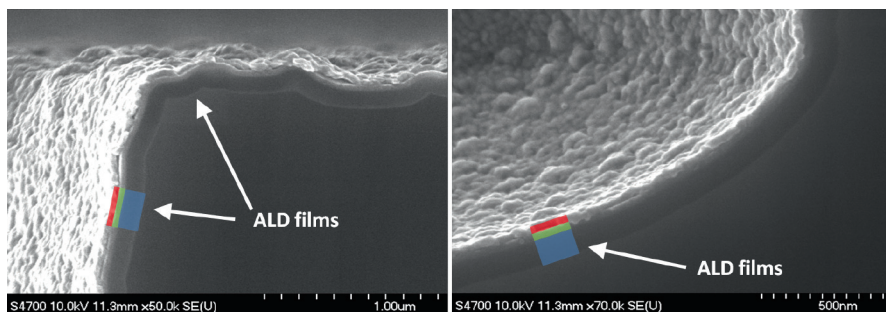


Fig. 2.14 Examples for an insulator—diffusion barrier- and seed-layer film stack in a TSV with a 20:1 aspect ratio. ALD films *blue*: insulator 100 nm Al_2O_3 ; ALD films *green*: barrier 32 nm TaN; ALD films *red*: seed 33 nm Ru; (TSV-diameter = 5 μm depth 130 μm , details: sidewall top, sidewall bottom) [19]

In this case the nucleation of the seed layer takes place by island formation. Both aspects hamper the formation of closed ultra thin layers.

In the following we present an ALD film stack for a high aspect ratio copper-based TSV. The state of the art copper diffusion barrier in current interconnect technologies is based on a tantalum nitride-based copper diffusion barrier, which is typically produced by PVD [17, 18]. Wojcik et al. showed that ALD films are less conducting than conventional PVD Ta-N films, but they have similar copper diffusion barrier properties [19]. The TaN (or TaC) ALD films are deposited in a showerhead ALD chamber using (*tert*-butylimido)tris(diethylamido)—TBTDET as a precursor. An additional post deposition anneal significantly improves the structural and electrical properties of the TaN-based ALD films [20, 21]. The Ru-ALD films are deposited in a showerhead ALD chamber using (ethylcyclopentadienyl)(pyrrolyl)ruthenium(II)—ECPR as a precursor and molecular oxygen as was presented for the first time in Junige et al. [22] .

For layers down to 33 nm (Ru) and 32 nm (TaN) on 100 nm Al_2O_3 insulator ALD films, conformity and continuity have been proven by Knaut et al., using scanning electron microscopy (Fig. 2.14) [19]. The investigations on high aspect ratios ($\text{AR} > 10:1$) have shown that a deposition of only 5–10 nm TaN barrier layer and a 5–10 nm Ru seed layer is sufficient for subsequent ECD of copper. In this case, 900 nm SiO_2 is used as insulator.

2.4 Electrochemical Deposition

Similar to damascene technology, the ECD process in TSV technology uses sulfuric acid–copper sulphate electrolytes with a small amount of chloride anions (usually 30–70 mg/L) and a set of three organic additives: accelerator, suppressor, and leveler. Because of the huge difference in the dimensions of structures to be

filled (damascene technology on nm-level, TSV on μm level), the duration of the deposition process is significantly different as well (damascene technology takes seconds to minutes while TSV takes minutes to hours). As a consequence two main parameters in the chemical composition of TSV electrolytes were modified. Firstly, the used copper concentration is increased (often 40–60 g/L) to dampen the effects of copper ion depletion inside the TSV during the deposition process. Secondly, the additive organic set consists of other chemical compounds. Obviously, applied current densities are much lower in TSV technology (1–3 mA/cm²) than in damascene technology (10–30 mA/cm²). The latter is meant to prevent copper ion depletion within the structures when diffusion is the overriding transport process.

The current state of TSV technology is the formation of copper seed layers by plasma-enhanced physical vapor deposition (PE-PVD) followed by Cu-ECD which is realized up to an aspect ratio of 10 reliably. Here, we replaced PE-PVD of Cu by thermal ALD of Ru (see Sect. 2.3.2) aiming at filling TSVs with aspect ratios higher than 10.

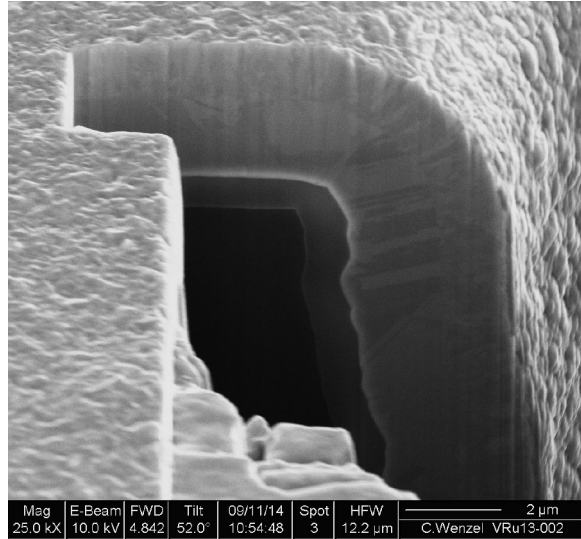
In comparison with Cu, Ru as a noble metal shows higher resistivity to acid attack (corrosion) but has a higher specific resistance than Cu (Ru: 7.43 $\mu\Omega\text{ cm}$ [300 K]; Cu: 1.67 $\mu\Omega\text{ cm}$) [23]. As expected, the specific resistance of Ru-ALD layers was dependent on film thickness and significantly higher than Ru bulk value. On 10 and 20 nm thick layers (30 \pm 3) $\mu\Omega\text{ cm}$, resp., (19 \pm 3) $\mu\Omega\text{ cm}$ were measured. Ru, in contrast to other noble metals, has high affinity to oxygen. Guo et al. reported a 1 nm Ru oxide film on PVD Ru [24]. In electrolytes, at potentials well below the formation of thick oxide layers, the oxidation of Ru is limited to the top layer of the film. At polycrystalline Ru, it was shown by in situ IR spectra measurements, that even at low potentials in acid solutions OH[−] ions of water cover the surface, preventing specific sorption of electrolyte anions over the whole potential range between hydrogen and oxygen evolution [25].

To prevent the negative influence of supposed superficial Ru-O species on Cu-ECD process (especially on Cu nucleation), a cathodic pretreatment in deaerated sulphuric acid followed by a rapid wet transfer to a Cu plating electrolyte was proposed in the literature (e.g., [26] and [27]). We have used a wafer with freshly deposited Ru layers.² According to our results under these conditions the Cu deposition performance and adhesion of Cu on Ru proved satisfactory.

Before starting the ECD we prewetted with 10 % SpherolyteTM (Atotech) in 10 % sulphuric acid for 10–20 s, rinsed shortly with deionized water, and then the TSVs were filled with basic electrolyte (i.e., without organic additives) by immersing the wafer under vacuum (−600 mbar). The removed wafer was rapidly transferred to a simple bench-top cell (on a magnetic stirrer) and contacted equidistant between two Cu anodes; the transfer took about 1.5–2 min until current flow was guaranteed. The electrolyte was 0.27 M Cu²⁺, 1.73 M H₂SO₄, 1.45 mM Cl[−] with optimized concentrations of commercially available (InterviaTM Viafill Acid Copper, Rohm & Haas) leveler, brightener (i.e., accelerator; SPS), and carrier (i.e., suppressor) [19].

² Storage of such wafers can be for only a very short time under nitrogen atmosphere or vacuum.

Fig. 2.15 Focused ion beam (FIB) cut of Cu-enhanced TSV: 3.6 μm Cu-ECD after 10 nm thermal Ru-ALD, 5 nm thermal TaN-ALD seed layer, and 900 nm SiO_2 insulator; TSV geometry: diameter 20–200 μm depth (AR10:1)



The obtained Cu thickness was about 2 μm (Figs. 2.15 and 2.16) deposited with current densities around 2.5 mA/cm^2 for 35–40 min; the ratio between thinnest film thickness in structure in reference to field region on wafer top (step coverage) was 70 %.

2.5 Interconnect and Bumping: Waferbumping for Cu and Al Metal Layer on Waferlevel

In this section, we present a process for the creation of interconnect and flip-chip bumps for an Si interposer on wafer scale by using ECD of tin-lead (Sn60Pb40—liquidus temperature 183 °C) or tin-silver (Sn97Ag3—liquidus temperature 221 °C) solder bumps [28]. The process steps are shown in Fig. 2.17. With this technique it is possible to create solder bumps on an interposer with Cu and Al metal pads and a passivation layer. For the ECD a conductive film using 50 nm wolfram titan (WTi) as adhesion layer and 150 nm copper as seed layer is deposited by PVD. A 20–30 μm thick resist layer serves a template for the pattern plating process and enables a uniform deposition of the solder bumps. Afterwards the under-bump metallization is created by ECD of 5 μm copper and 1 μm nickel layer. In the next step, depending on the pad size, an approximately 30 μm thick tin-lead or tin-silver is deposited by ECD. The WTi and Cu overall metallization is removed by a wet chemical etching after the stripping of the resist. For the bump formation the solder bump is reflowed in glycerin using 210 °C/20 s for SnPb and 235 °C/20 s for SnAg (Fig. 2.18).

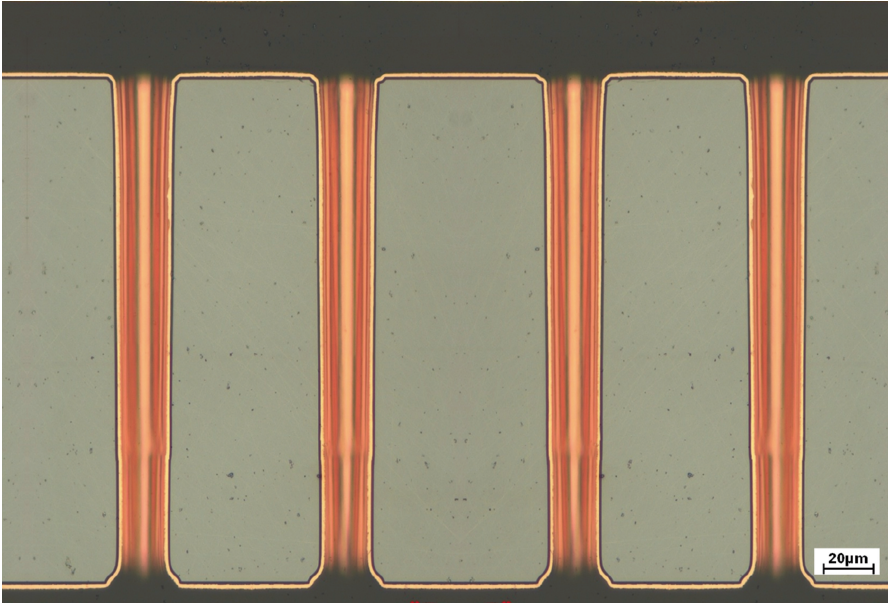


Fig. 2.16 Copper enhanced TSV: 2 μm Cu-ECD after barrier and seed layer 5 nm thermal TaN-ALD + 10 nm thermal Ru-ALD TSV geometry: diameter 20–200 μm depth (AR10:1); layer stack: 900 nm SiO₂; 5 nm TaN; 10 nm Ru; 2 μm Cu

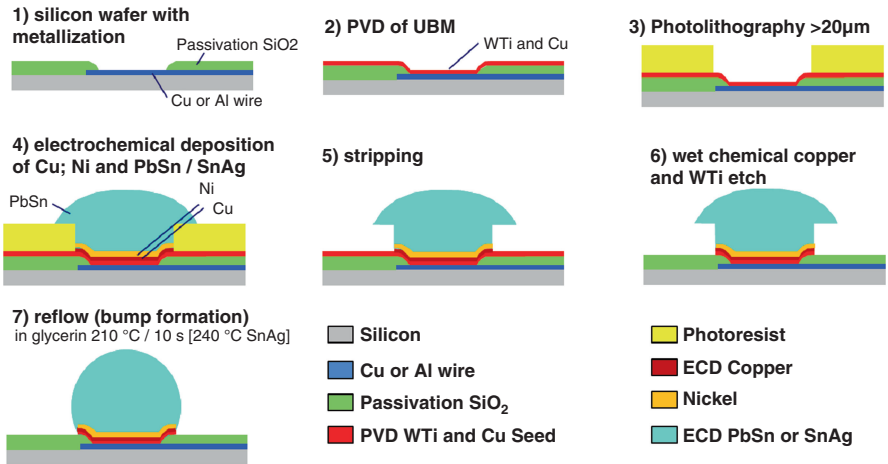


Fig. 2.17 Wafer-level process for ECD solder bump deposition for interconnect and interposer

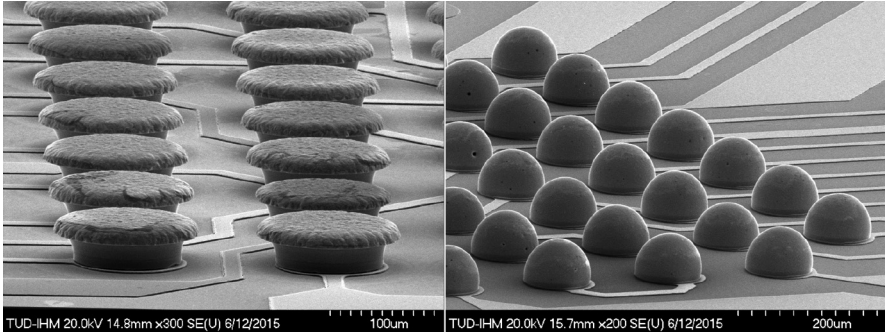


Fig. 2.18 SnAg solder bump deposited by ECD. *Left*: before reflow. *Right*: after reflow. Reflow temperature: 235 °C/20 s in glycerin

2.6 Conclusion

This chapter has described a manufacturing process for the creation of an Si interposer using copper-based TSV for 3D integration and chip stacking. A silicon via etching process for aspect ratios from 10:1 to 20:1 using a sacrificial Al-stop layer in 200 µm thick wafers has been demonstrated. The TSVs are formed using deep reactive ion etching (DRIE). The polymeric sidewall passivation layers created during DRIE processing are stripped wet-chemically and the Al-stop layer is removed by an additional wet-etch process. Furthermore, residual polymer is removed and the sidewalls are smoothed by reactive ion etching in an oxygen-nitrogen trifluoride plasma. Thus it is possible to generate high aspect ratio TSVs, having little surface roughness, no notching, and adapted profiles with no additional wafer thinning. To prevent leakage between different interconnects, an insulating silicon dioxide layer is grown by thermal processing. The high aspect ratio TSV structures were coated with an ALD film stack consisting of a 5–10 nm TaN-based copper diffusion barrier and a 10 nm Ru(C) seed layer for copper plating. The TSVs are either filled or just enhanced with copper in an electrochemical plating process. An additional front and back side lithography is used to generate the metallization layer mask for the subsequent patterning processes. The copper layers on both sides of the interposer are structured in a wet etching process and the redistribution lines on the front and the back side of the wafer are created by pattern plating. The seed and the barrier layers are removed afterwards in a plasma etch process. In a waferbumping process, the interconnect and flip-chip bumps for the Si interposer are created on wafer scale using ECD of tin-lead³ or tin-silver⁴ solder. In the subsequent chapters of Part I of the book, it is this interposer TSV process that is used in all

³ Sn60Pb40—liquidus temperature 183 °C.

⁴ Sn97Ag3—liquidus temperature 221 °C.

the circuits, systems, and CAD technology demonstrators (Chaps. 3–6, and 9). The electrical characterization of the TSV, including pads and bumps, is presented in the next chapter.

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