

Preface

So I devoted several months in privacy to the composition of a treatise on the mysteries of Three Dimensions.

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The future evolution of the form factors of cell phones, tablets, wearable electronic devices, microsensors, and other similar gadgets of the world's digital fabric requires that we develop integration technologies that enable volume-based assembly of chips, sensors, devices, and interfaces. 3D stacked chips and 3D-integrated circuits belong to such volume-based approaches. These volume-based technologies have already made their way into electronic products such as memory devices and cell phones and are slated to become the dominant trends in microsystem fabrication in the next decade. Many research monographs about this topic have already been published, including a three-volume edited book entitled *Handbook of 3D Integration*, by Wiley-VCH. Springer has also published several research monographs on this topic. One of the most recent ones is the 2013 book by Sung Kyu Lim, entitled *Design for High Performance, Low Power and Reliable 3D Integrated Circuits*.

This book covers recent work on 3D integration conducted by researchers from the Technical University of Dresden, Germany, and the Masdar Institute of Science and Technology, Abu Dhabi, UAE, under the framework of Twinlab 3D Stacked Chip (3DSC), a joint collaborative effort focusing on heterogeneous 3D integration. The book addresses some of the most important challenges in this emerging technology, especially as they pertain to 3D heterogeneous integration. Indeed, one of the promises of 3D chip stacks is to enable the integration, under very small form factors, of chips belonging to different semiconductor technologies (e.g. CMOS vs. SiGe), different design modalities (e.g. digital vs analogue), and different physical domains (e.g. electrical vs. optical). In addition, under the same small form factors, the 3D chip stacks will help extend the integration domain to include not only the processing and communication functions but also the sensing and the power sourcing functions. Recent industrial examples of heterogeneous 3D integration include CMOS imaging sensors and MEMS inertial sensors.

The issues and challenges of heterogeneous 3D integration are addressed at both the process and system levels with particular emphasis on the 3D integration of on-chip high-speed links and optoelectronic systems. In particular, the book contains original material on the use of interposers in 3D-integrated CMOS and Si photonics. Processing, modelling, design, and CAD aspects are all considered and treated in a

coherent framework for the first time in the open literature. Of particular interest are interposer process recipes for the manufacturing of high-aspect ratio through-silicon vias (TSVs) that do not require any wafer thinning. Such TSVs may be used for high-speed serial communication in both the electrical and optical domains. Particular attention has been given to the design of transceivers for serial links having TSVs in their path and to the design of digitally assisted clocking circuits for 3D chip stacks. Topical coverage also includes the 3D heterogeneous integration of various photonic devices such as tunable resonators, power sources such as photovoltaic cells, and non-volatile memories based on new materials systems (e.g. ZnO). Finally, the thermal challenges of 3D stacked chips are addressed from the viewpoints of accurate, on-chip, temperature sensing, early physical design planning using thermal TSVs, and the development of athermal photonic components for optoelectronic 3D chip stacks.

The book consists of 17 chapters organised in two parts. The first part, with ten chapters, is devoted to electronic 3D integration using copper TSVs. The second part, with the remaining seven chapters, is devoted to photonic and optoelectronic 3D integration using photonic TSVs. Each part opens with an introductory chapter, I for Part I and II for Part II, positioning the research work in the context of the integrated electronic and Si photonic circuits and systems. Here is a short summary of the content of each part.

In Chap. 2, a process recipe is proposed for the fabrication of high-aspect ratio (up to 20:1) copper TSVs for Si interposer-based 3D integration. The recipe uses atomic layer deposition (ALD) to deposit the copper barrier and the seed layer for copper electroplating. Such usage enables the fabrication of high-quality TSVs with uniform cladding deposition along the TSV height.

In Chap. 3, a 3D interposer architecture is used as a platform for the design and implementation of energy-efficient serial communication links across a 3D chip stack. The communication link implementation includes the design of an energy-efficient, low-voltage-swing, multibit capacitive transceiver based on a detailed equivalent circuit model of the TSV channel. Silicon results using GLOBAL-FOUNDRIES 28 nm SLP CMOS technology show that the transceiver design outperforms competing solutions by more than $2\times$ in terms of energy efficiency (Joule per bit per number of TSV channels).

The main motivation for developing serial links for TSV channels is to reduce the number of TSVs needed and thus reduce the area overhead of 3D integration. When multiple signal TSVs are needed in closer proximity to each other, crosstalk will occur and channel equalisation to overcome crosstalk noise on signal TSVs will be needed. This is the main topic of Chap. 4 where equalisation method is implemented in the discrete-time domain and is based on an equivalent circuit model of the capacitive crosstalk between neighbouring TSVs. It also uses realistic assumptions on the IO cells to which the TSVs are connected. Of particular interest in Chap. 4 is the impact of quantisation on the equaliser's performance. It is found that a 3-bit, non-uniform quantiser can outperform a 5-bit uniform quantiser by $2\times$ in terms of crosstalk rejection.

While the quantisation aspects of equalisation pertain to the transmitter, the issue arises as to how to reconstruct the received signal on the TSV channel using the coarsest analogue-to-digital converter (ADC), namely, a 1-bit ADC. In Chap. 5, this issue is addressed in the context of designing energy-efficient receivers for TSV-based communication links.

Heterogeneous integration presents the designer with the challenge of implementing clocking schemes that have to satisfy multiple requirements at the global system level and for each local clock in the system components. Such requirements arise in the multiprocessor system-on-chips. This clock design challenge is addressed in Chap. 6, where an all-digital, phase-locked-loop (ADPLL) architecture is used as the backbone of a clocking solution for a heterogeneous multiprocessor system. The ADPLL is multi-phase and is used to generate fractional frequencies for cores and components with the distinguishing feature of allowing instantaneous changes in the frequency division ratio within a single clock cycle. Such features are important for implementing high-performance dynamic voltage and frequency scaling (DVFS) protocols on a per-core basis. For the ADPLL, silicon results are provided for an implementation in GLOBALFOUNDRIES 28 nm CMOS process that shows a controllable clock from 80 MHz to 2 GHz, having a power consumption of 0.64 mW and occupying an area of 2340 μm^2 . The frequency synthesiser is also implemented in GLOBALFOUNDRIES 65 nm and 28 nm processes and is shown to achieve competitive figures of merit in area, power consumption, frequency range, and fractional granularity.

DRAM memory cubes were amongst the earliest commercial products using 3D integration technology. These products have been mainly driven by the high-performance computing market and are meant to bridge the performance gap that exists between system memory and CPU/GPU. For non-volatile memory (NVM) such as NAND or NOR flash, no such commercial products exist yet, but R & D work is under way to realise a high-capacity, 3D flash memory. In Chap. 7 of Part I, the technological issues of building a low-power, high-density NVM are addressed. It is shown that Si nanoparticles can enhance charge trapping in NVM and thus can be used to improve retention time and reduce programming and reading voltages. The latter will result not only in lower power consumption but also in mitigating the impact of thermal gradients on stacked NVM layers.

Of course the issue of thermal monitoring and management remains one of the most challenging aspects of 3D ICs. The book devotes three Chaps. 8, 10, and 16, to address this issue at the levels of monitoring, physical design, and device design, respectively. In Chap. 8, the problem of accurate on-chip temperature measurement is investigated, and a novel, compact, temperature sensor is proposed, achieving sub 1 °C accuracy over a temperature range from 0 to 100 °C. A distinguishing feature of the proposed design is the use of the bandgap reference of the temperature sensor as a reference voltage in the 12-bit successive-approximation register ADC. The issue of the number and placement of these on-chip temperature sensors is a research topic of its own and would require full information on the physical design of the 3D IC and its thermal map.

Chapter 10 is devoted to thermal-aware early physical design of 3D IC. The issue of the 3D IC floor planning is considered under the requirement that the resulting floor plan has a temperature map that falls within a predefined set of specifications across the chip stack. This is achieved using thermal TSVs which play, for heat conduction, the role that electrical TSVs play for signal transmission. The proposed floor planning algorithm achieves more than 100 K reduction in temperature for a four-layer stack at a thermal TSV via density of less than 0.5 %.

At the component design level, Chap. 16 in Part II addresses the issue of designing Si photonic components that are insensitive to temperature variations. The challenge here is that temperature impacts not only the index of refraction but also the wavelength at which the Si photonic device operates. For the case of a Mach–Zehnder interferometer (MZI), Chap. 16 proposes an *athermal* design that has a spectral sensitivity of less than 10 pm/K over the 1510–1590 nm wavelength range. The design is based on a mathematical formulation imposing both first-order and second-order sensitivity constraints on the MZI phase condition.

Besides the thermal challenge in 3D chip stacks, the lack of computer-aided design tools that are fully adapted to the 3D design environment has also been a hurdle. Early work on CAD for 3D IC focused on extending IC tools and environments to account for vertical chips stacking using TSVs. Yet, 3D integration is not just a chip technology, it is also a packaging technology, with its “supply chain” including not only IC-centric environments but also packaging and printed-circuit board environments. This viewpoint is adopted in Chap. 9 of Part I, where methodologies for 3D chip-package co-design are described in details using the TSV interposer technology demonstrator of Chaps. 3 and 6 as a case study.

In Part II, after an introductory chapter on the importance of optical communication for interconnect-centric IC design, Chap. 12 offers fabrication recipes of three possible options for manufacturing an optical TSV which are presented. They are an air-filled TSV with Si walls, a polymer-filled TSV with SiO₂ cladding, and a hybrid TSV with copper walls. These optical TSVs are fabricated, characterised, and compared in terms of their eye diagrams, bit error rates, and transmitted optical power.

Chapter 13 surveys both the passive and active photonic devices that are the building blocks of photonic communication links. One of the potential benefits of heterogeneous 3D die stacking is the seamless integrations of optical power sources such as III/V semiconductor lasers with Si photonic components using optical TSVs of the type proposed in Chap. 12. In Chap. 13, lasers, photonic modulators, and photodetectors are described along with an overview of the optical, electrical, and optoelectronic measurement techniques for photonic components.

An example of a Si photonic device is given in Chap. 14, where the theory, design, and numerical validation of a tunable silicon microring resonator are presented. Such tunable resonators are essential components for designing filters with controllable resonant frequencies as may be required in waveform-division multiplexing systems. The tuning mechanism adopted in the design is that of a microelectromechanical cantilever. This mechanism has the distinct advantage of being low-power and fully compatible with the Si photonic fabrication platform.

It is well known that photonic transmission is very sensitive to temperature variations. This sensitivity becomes even more problematic in 3D optoelectronic integration where temperature gradients are common due to the blocking of heat conduction paths. As was mentioned previously, Chap. 15 proposes a Mach–Zehnder interferometer (MZI) design that is insensitive to temperature variations. This is achieved by carefully selecting the dimensions of the MZI waveguides so as to satisfy phase invariance conditions with respect to temperature and spectral variations.

The realisation of full on-chip communication links achieving Terabits/s data rates requires that the IC interfaces be of sufficient bandwidth to support the optoelectronic transceivers that are expected to operate in the THz regimes. Such communication systems can be realised only if the promise of 3D heterogeneous integration is fulfilled. A case in point is the one discussed in Chap. 16, where the high-bandwidth IC drivers of laser sources are designed. To meet the data and rate and bandwidth specifications, a 130 nm SiGe BiCMOS technology is used. These laser source drivers are validated using the photonic TSV developed in Chap. 12 and are shown to support a data rate of 71 Gbits/s with a power efficiency of 13.4 mW/Gbits/s.

Chapter 17, the last chapter of the book, addresses the issue of integrating power sources and energy harvesters with 3D chip stacks with focus on photovoltaic cells. One promising technology for such integration is the back-contacted hetero-junction solar cell that can achieve up to 26 % conversion efficiency. The chapter is mainly devoted to a parametric study of the performance of such cells as expressed by their fill factors, open-source voltages, and short circuit currents.

To make the most out of the chapters of this book, the reader should have basic understanding of semiconductor processing, IC design, and photonics. Our targeted audience are faculty and graduate students in EECS programmes, engineers and technologists in the semiconductor industry, and R & D managers and leaders interested in keeping apace with the latest in academic research on 3D chip stacking.

We realise there is now a large body of literature devoted to 3D chip stacking and IC integration, and we understand that one more book in this area may pass as a belated expression of “me too-ism” in an already crowded domain. Yet we think that this book offers unique features that set it apart from other distinguished contributions to the 3D integration field. These unique features include the consideration of both electronic and photonic 3D integration, the use of high-speed, on-chip communication as a unifying and motivating theme, and the coverage of topics not typically treated under the 3D integration headline such as thermal sensing and optoelectronic ICs.

The compilation of this book would not have been possible without the dedication, hard work, and commitment of all the contributing authors. To them go our deepest gratitude and warmest thanks!

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