Micropower Incremental Analog-to-Digital Converters

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Abstract Integrated sensor interfaces require energy-efficient high-resolution data converters. In many applications, the best choice is to use incremental analog-to-digital converters (IADCs) incorporating variants of extended counting. In this chapter, we discuss the design of a micropower IADC. By using a feed-forward architecture, the IADC accumulates the residue voltage, so various hybrid variants of extended counting can be implemented. Several such schemes are reviewed and discussed, as well as the trade-off between higher order modulators, higher oversampling ratio and energy efficiency. A two-step IADC is proposed, which extends the performance of an *Nth*-order IADC close to that of a $(2N-1)$th-order IADC. A design example uses the circuitry of a second-order IADC to achieve a performance nearly equal to that of a third-order IADC. The implemented IADC achieves a measured dynamic range of 99.8 dB, and a SNDR of 91 dB for a maximum input 2.2 V_{PP} and a bandwidth of 250 Hz. Fabricated in 65 nm CMOS and operated from a 1.2 V power supply, the IADC's core area is 0.2 mm^2, and it consumes only 10.7 μW. The measured FoMs are 0.76 pJ/conv.step and 173.5 dB, both among the best reported results for IADCs.

1 Introduction

As semiconductor technology evolves, more sensory functions can be integrated on a system-on-chip (SoC). Such SoCs are found in temperature, magnetic, pressure and image sensors, as well as in weight scales and bio-potential acquisition systems. An energy- and area-efficient high resolution analog-to-digital converter (ADC) is especially critical for battery-operated sensor SoCs. Sensor applications often involve narrow-band signals with frequencies from DC [1–3] up to several hundred Hz [4–6], and so the ADC should achieve high accuracy even in the presence of DC offset voltage and flicker noise. In addition, the integrated ADC must often be

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multiplexed among many channels. In applications requiring hundreds of channels, such as in image sensors [7, 8] or for bio-potential acquisition [4–6], the ADCs must also be highly efficient in terms of power and chip area.

Incremental analog-to-digital converters (IADCs) are often the best choice for low-frequency high-resolution sensor interfaces [1, 3, 5, 6, 9, 10]. Their advantages [9–11] include simpler decimation filtering, easy multiplexing, and sufficiently low latency. IADCs are also less subject to idle tones [11]. Moreover, the finite-impulse-response (FIR) filtering of the input signal in an IADC reduces aliasing [12]. However, a first-order IADC (IADC1) needs 2^N oversampling clock periods for N-bit accuracy, requiring a high sampling frequency and so it is not energy-efficient. To enhance efficiency, higher-order modulators can be used to increase the accuracy within the same conversion time. However, high-order modulators are more prone to instability, and have a reduced non-overloading input range. As an alternative to single-loop modulators, multi-stage noise-shaping (MASH) IADCs [13, 14], and also hybrid schemes which incorporate an added Nyquist-rate ADC to perform extended counting [6–8, 14, 15] have been proposed. However, MASH modulators and hybrid extended-counting schemes increase circuit complexity, and circuit non-idealities may then cause severe performance degradation. To retain the advantages without too much overhead circuitry, we propose a second-order IADC that uses a two-step architecture.

In this chapter, the design and operation of a conventional single-loop IADC with a feedforward modulator will first be reviewed, followed by a discussion of the operation and advantages of a MASH IADC in Sect. 2. Hybrid IADCs which recycle the hardware to perform extended counting, and thus achieve excellent energy efficiency, are discussed in Sect. 3. The detailed design and theoretical analysis of an IADC that employs a two-step architecture [16, 17] is described in Sect. 4. The novel scheme is applied to a second-order IADC (IADC2). The circuit's design and measured performance are discussed in Sect. 5. By recycling the hardware of the IADC2, the performance of the proposed two-step IADC is nearly as good as that of a conventional third-order IADC (IADC3), but require much less energy for the same conversion time. Section 6 summarizes the chapter and ends with conclusions.

2 Incremental Analog-to-Digital Converters

2.1 Operation and Design of a Second-Order IADC

IADCs are *Nyquist-rate* ADCs which use oversampling and noise shaping to convert a finite number of analog samples into a single digital word. Thus, they are a hybrid of Nyquist-rate and $\Delta\Sigma$ ADCs [9, 18]. Figure 1a depicts the z-domain model of an IADC2 with a low-distortion feed-forward modulator [9, 10]. The simplified timing diagram, including the two-phase non-overlapping clocks and reset pulse, is shown in Fig. 1b. Here, M is the oversampling ratio (OSR), defined as the number

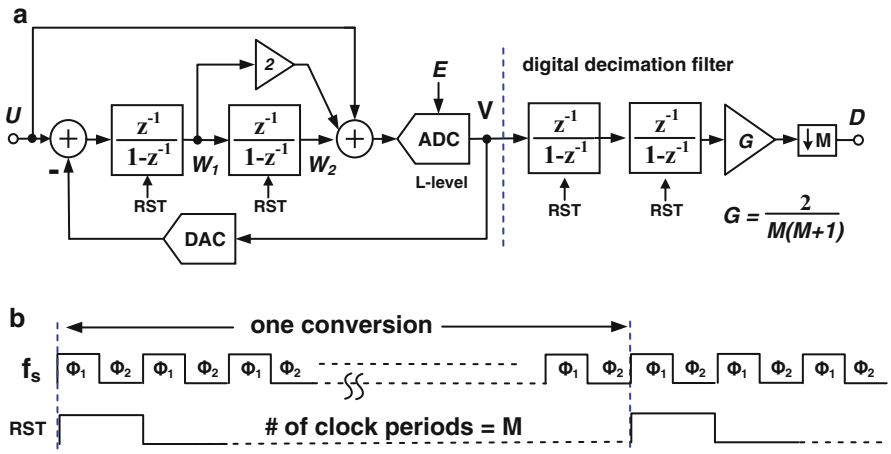

Fig. 1 (**a**) The z-domain model of a single-loop IADC2 with a low-distortion feed-forward modulator. (**b**) The simplified timing diagram

of oversampling clock periods within one conversion period. The operation of the IADC begins with a global reset pulse to clear the memories of all analog and digital blocks. After this reset, the $\Delta\Sigma$ modulator loop quantizes the analog input voltage U, and the digital filter concurrently processes the output bit stream V. After M clock periods, the next reset pulse reads the output word, and clears all memories. The circuit converts analog data *sample-by-sample*, and hence functions as a Nyquist-rate ADC.

The operation of an IADC is best understood by using time-domain analysis [9, 12]. At the end of the conversion (time index $i = M$) in Fig. 1, the variables satisfy the equation

$$U[M] + 2\sum_{i=1}^{M-1} U[i] + \sum_{K=1}^{M-1}\sum_{i=1}^{K-1} U[i] + E[M] = V[M] + 2\sum_{i=1}^{M-1} V[i] + \sum_{K=1}^{M-1}\sum_{i=1}^{K-1} V[i] \tag{1}$$

From (1),

$$\sum_{K=1}^{M}\sum_{i=1}^{K} U[i] + E[M] = \sum_{K=1}^{M}\sum_{i=1}^{K} V[i] \tag{2}$$

The least-significant-bit (LSB) quantization error E of the internal L-level quantizer is $V_{FS}/(L-1)$, where V_{FS} is the full-scale voltage. We may define the *average input voltage* $\tilde{U}$ by the relation

$$\tilde{U} \cong \frac{2}{M\,(M+1)} \sum_{j=1}^{M} \sum_{i=1}^{j} U\,[i] \tag{3}$$

Note that $\tilde{U}$ represents the input accurately only if U does not vary significantly during the conversion. From (2),

$$\tilde{U} + \frac{2}{M\,(M+1)} \frac{V_{FS}}{L-1} = \frac{2}{M\,(M+1)} \sum_{K=1}^{M} \sum_{i=1}^{K} V\,[i] \tag{4}$$

To reconstruct $\tilde{U}$ from the output bit stream, the digital decimation filter should perform the operation on the right-hand-side of (4). For an IADC2, the decimation filter can thus be simply two counters in cascade (Fig. 1). Alternatively, a multiply and accumulate (MAC) operation may be used. As (4) shows, the loop filter samples the input signal M times in one conversion, and performs finite-impulse-response (FIR) filtering [12] on the input signal.

The equivalent LSB quantization error E_{IADC2} of the IADC2 is

$$E_{IADC2} = \frac{2}{M\,(M+1)} \frac{V_{FS}}{L-1} \tag{5}$$

The effective number of bits (ENOB) and the signal-to-quantization-noise-ratio (SQNR) at full-scale input amplitude are given by

$$ENOB_2 = \log_2 \left(\frac{V_{FS}}{E_{IADC2}} \right) \tag{6}$$

and

$$\begin{aligned} SQNR_2 &= 10\ \log \left(\frac{V_{FS}^2/8}{E_{IADC2}^2/12} \right) \\ &\approx 20\ \log \left(\frac{V_{FS}}{E_{IADC2}} \right) \approx 2 \cdot 20\ \log(M) + 20\ \log\,(L-1) - 6 \end{aligned} \tag{7}$$

The analysis can be extended to an *Nth*-order IADC (IADCN). The equivalent quantization error and the maximum SQNR of an IADCN are

$$E_{IADCN} \approx \frac{N!}{M^N} \frac{V_{FS}}{L-1} \tag{8}$$

$$SQNR_N \approx N \cdot 20\ \log(M) + 20\ \log\,(L-1) - 20\ \log\,(N!) \tag{9}$$

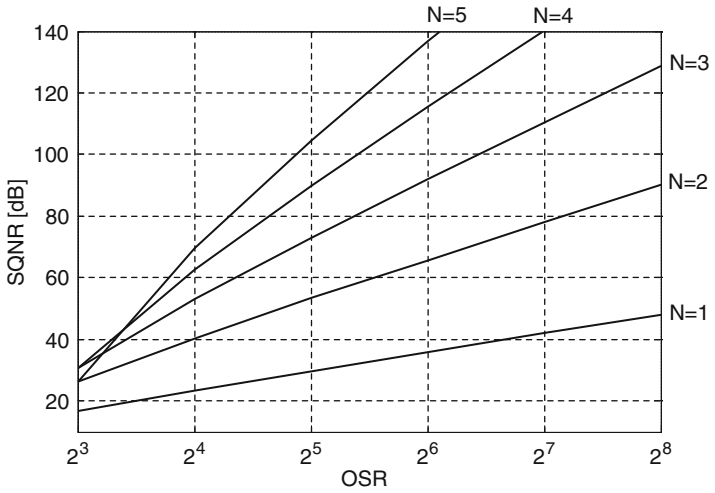

Fig. 2 SQNR versus OSR for one-bit modulator from first-order (N = 1) to fifth-order (N = 5)

The *Nth*-order loop filter scales down the internal quantization error by a factor $N!/M^N$. Figure 2 shows the calculated SQNR versus OSR for two-level ($L = 2$) modulators with orders $N = 1 \sim 5$.

2.2 MASH IADCs

To mitigate the stability problem of a higher-order single-loop IADC, the multi-stage noise-shaping (MASH) technique of a conventional $\Delta\Sigma$ ADC can be applied to an IADC [12, 13, 18]. Figure 3 shows an example of 1-1 MASH IADC2 obtained by cascading two IADC1s. A higher-order IADC can be achieved by cascading lower-order modulators and thus the energy efficiency is improved because less peripheral circuitry (quantizer and DAC circuits) is required to sustain a wide non-overloaded range.

Conventional MASH $\Delta\Sigma$ modulators [19, 20] need to use error cancellation logic (ECL) circuits before adding the bit streams of the individual loops, to cancel the quantization error of the MSB loop. The opamp DC gains in the first loop need to be very high, to avoid SQNR degradation caused by mismatch between the analog and digital realizations of the noise transfer function $\left(1 - z^{-1}\right)$. Thus, a MASH $\Delta\Sigma$ ADC for a 16-bit SNR usually requires opamp DC gains of at least 90 dB [20], which is difficult to achieve in a low-voltage design. In MASH IADCs [12, 13], the oversampled bit streams of the $\Delta\Sigma$ loops are accumulated in one or more cascaded counters. The Nyquist-rate data from each loop are accumulated separately, and the

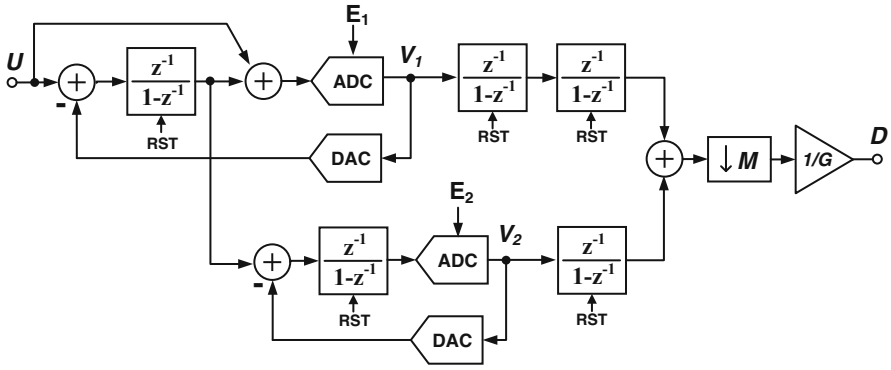

Fig. 3 A 1-1 MASH IADC

counters dump the data before the next reset pulse. The opamp gain requirements in a MASH IADC are hence much more relaxed than in their conventional MASH $\Delta\Sigma$ counterparts [12, 13].

2.3 IADC Versus ΔΣ ADCs

As discussed above, an IADC functions like a Nyquist-rate ADC, and is more suitable for use in a sensor interface than a conventional $\Delta\Sigma$ ADC. Its advantages are as follows:

- An IADC can be easily multiplexed among many channels. This saves area and the resulting sensor SoC can be cost effective.
- The latency from the analog input to the decimated digital output is only one Nyquist conversion period T_N. For an *Lth* order $\Delta\Sigma$ ADC, it is $(L+1)T_N$ [18–20].
- The idle tone is much less likely than in a conventional $\Delta\Sigma$ counterpart [11]. However, there may be "deadbands" around the quantizer's thresholds (around zero for two-level quantizer). They can be eliminated by injecting dither [9, 13].
- The decimation filter is simpler. It may be a cascade of a few accumulators, or a single MAC stage. Thus, the energy efficiency is improved.

3 Hybrid Schemes Using an IADC and a Nyquist-Rate ADC

In Fig. 1, the feed-forward loop filter processes only the shaped quantization noise. At the end of the conversion, the voltage stored at the last integrator is the residue voltage of the $\Delta\Sigma$ data conversion [6–8, 14, 15], and it is available for fine

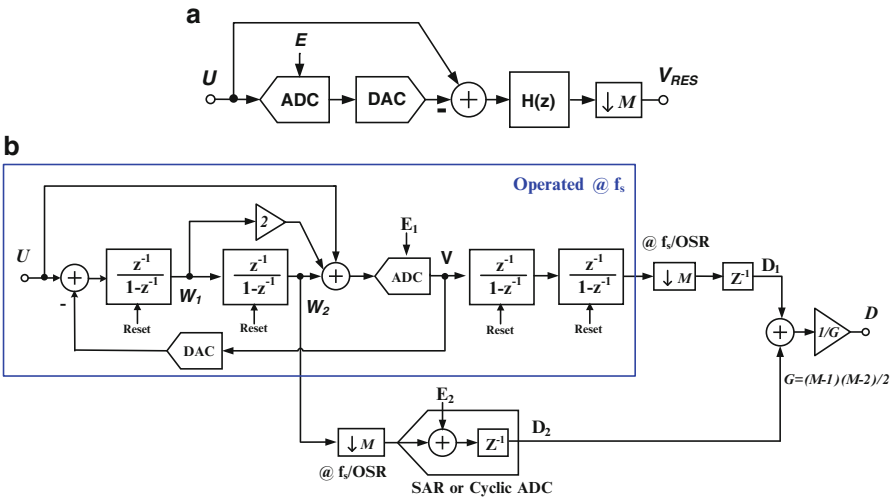

Fig. 4 (**a**) Residue voltage acquisition using a feedforward modulator. (**b**) An IADC using a second Nyquist-rate ADC for extended counting [6]

quantization. The residue voltage acquisition is illustrated in Fig. 4a. Hence, an energy-efficient SAR or cyclic ADC operated at Nyquist rate can sample the residue voltage right before the reset pulse, and perform the fine quantization [6, 21]. An example of such an extended-counting scheme is shown in Fig. 4b [6]. With proper design of the digital summation logic and decimation filter, the two cascaded loops can achieve a very high resolution with good energy efficiency. However, the last integrator needs to drive the large input capacitance of the 11-bit SAR [6], and therefore needs additional power.

For high resolution, the time required for one data conversion is usually quite long. Hence, instead of cascading two loops, the conversion can be performed in two steps, and the hardware can be shared to improve the energy efficiency [7, 8, 14, 15]. An example of a hardware-sharing extended-counting scheme is shown in Fig. 5 [7]. A discrete-time IADC1 performs the coarse quantization (Fig. 5b), and the integrator stores the residue voltage at the end of the first quantization step. In the second step, the hardware is reused and reconfigured as a 10-bit cyclic ADC to continue the fine quantization (Fig. 5c). By sharing the hardware, the energy efficiency is improved significantly.

In [22], a two-step incremental zoom ADC with a 182.7 dB figure-of-merit (FoM) was reported for DC measurements. A coarse ADC finds the six MSBs, without storing the residue, and the MSBs adjust the reference of the second-stage IADC, so as to zoom into a small range around the input signal. Then, the IADC samples the input signals, and performs the fine quantization for 1024 clock periods. Due to its smaller range, however, the input signal must be held very constant during

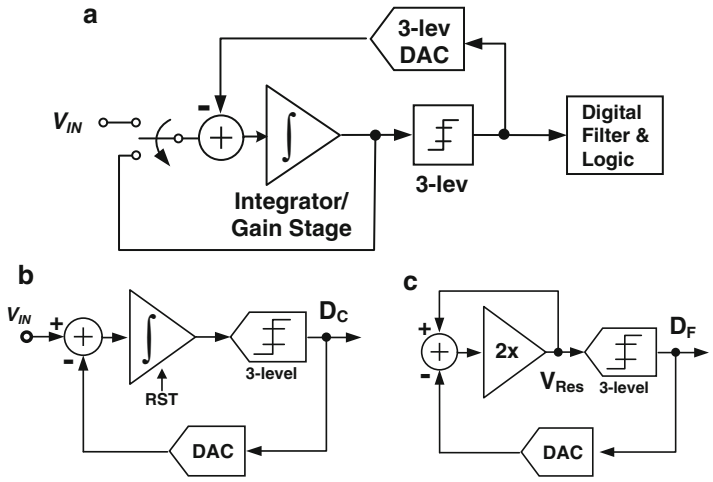

Fig. 5 (**a**) An example of IADC with extended counting using hardware sharing [7]. (**b**) A discrete-time IADC1 acts as the coarse quantization ADC. (**c**) Re-configured as a 10-bit cyclic ADC to perform the fine quantization

the second step. Thus, even though the zoom ADC can measure DC signals with extraordinary energy efficiency, it is not well-suited to wide-band signals, such as occur in bio-potential acquisition systems.

4 Two-Step Incremental ADCs

As shown in Fig. 2, we can improve the SQNR of an IADC by using a higher OSR or a higher-order modulator. For example, for an IADC2 with OSR = 64, doubling the OSR improves the SQNR by 15 dB, while increasing the order by 1 enhances the SQNR by 27 dB. Thus, it is more effective to increase the order of modulation than to raise the OSR. Unfortunately, increasing the order requires extra opamps. Besides, a higher-resolution internal quantizer is usually needed to make a higher-order modulator stable, and the complexity of the peripheral circuitry also increases. The power required increases accordingly, and the ADC becomes less efficient.

Next, a two-step architecture [23] will be described which avoids the excess power dissipation for high-resolution data conversion. Figure 6 shows the z-domain model of the proposed two-step IADC2. During the first step, lasting for M_1 clock periods, the circuit is operated as a conventional IADC2 (Fig. 6a). The residue voltage V_{RES} stored in the second integrator (INT2) after clock period M_1 is given by

$$V_{RES} = W_2[M_1] = \sum_{K=1}^{M_1-1}\sum_{i=1}^{K-1} U[i] - \sum_{K=1}^{M_1-1}\sum_{i=1}^{K-1} D_1[i] \tag{10}$$

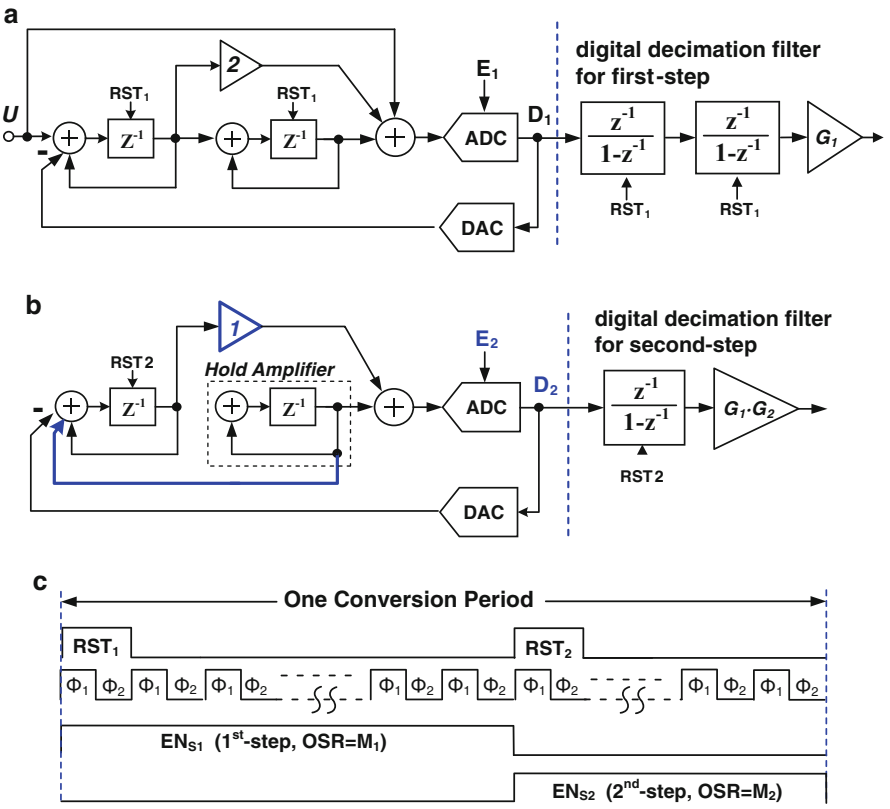

Fig. 6 The proposed IADC2 in two-step operation. (**a**) First step. (**b**) Second step. (**c**) The simplified timing diagram

The direct-input feed-forward modulator generates the residue voltage at the end of first conversion step for fine quantization.

To perform the second step (fine quantization), the analog modulator and the digital filter are reconfigured, as shown in Fig. 6b. The INT2 now stops sampling, and acts as a hold amplifier that feeds the residue voltage V_{RES} into the L-level quantizer and the first integrator (INT1). INT1 is reset again, and then samples the residue voltage V_{RES} from INT2. The reconfigured circuits act as an IADC1 for the remaining M_2 clock periods. Analysis gives

$$\sum_{i=1}^{M_2-1} V_{RES} + E_2 = \sum_{i=1}^{M_2-1} D_2\,[i] \tag{11}$$

Since V_{RES} remains constant during the second step, it can be represented as

$$\sum_{i=1}^{M_2-1} V_{RES} = (M_2 - 1) \cdot V_{RES} \tag{12}$$

The quantization error E_1 of the first step IADC2 is cancelled as in a MASH $\Delta\Sigma$ ADC [12, 13], and only the final error E_2 remains after the two-step operation. While the input voltage U is sampled only during the first step, the average of the input signal $\tilde{U}$ can be re-defined with M replaced by M_1 in (3). After the two steps of conversion, the signals satisfy

$$\tilde{U} + \frac{2}{(M_1-1)(M_1-2)(M_2-1)}E_2 = \frac{2}{(M_1-1)(M_1-2)}\left(\sum_{j=1}^{M_1-1}\sum_{i=1}^{j-1} D_1[i] + \frac{1}{(M_2-1)}\sum_{i=1}^{M_2-1} D_2[i]\right) \tag{13}$$

The decimation filter needed to reconstruct the bit streams of each step can be designed from the right-hand-side of (13). For the first step, the decimation filter can be realized by two cascaded counters. For the second step, one of the counters can be reused. Thus, the IADC2's analog and digital hardware can be used in both steps with a simple reconfiguration. The equivalent quantization error of the two step conversion can be estimated from

$$E_{21} = \frac{2}{(M_1-1)(M_1-2)(M_2-1)}\frac{V_{FS}}{L-1} \tag{14}$$

The SQNR at full-scale input amplitude is given by

$$SQNR_{21}=20\ \log(V_{FS}/E_1) \approx 2\cdot 20\ \log(M_1) + 20\ \log(M_2) + 20\ \log(L-1) - 6 \tag{15}$$

With a total OSR $= M = M_1 + M_2$, the optimal selection of the OSR values M_1 and M_2 in a two-step IADC is easily found. Defining the ratio $k = M_1/M_2$, we obtain $M_1 = kM/(k+1)$ and $M_2 = M/(k+1)$. The quantization error of the two-step IADC can then be written in the form

$$E_{21} \approx \frac{2}{M_1^2 \cdot M_2}\frac{V_{FS}}{L-1} = \frac{2}{\frac{k^2\cdot M^3}{(k+1)^3}}\frac{V_{FS}}{L-1} \tag{16}$$

The minimum of the quantization error results by setting $k = 2$. The optimum OSRs of the two steps are then $M_1 = 2M_2 = 2M/3$. The maximum $SQNR_{21}$ is

$$SQNR_{21,OPT} \approx 3\cdot 20\ \log(M) + 20\ \log(L-1) - 20\ \log(6) - 20\ \log(9/4) \tag{17}$$

For a total OSR of 192, the SQNR of the two-step IADC versus M_1 is plotted in Fig. 7a, which verifies that the maximum SQNR for $M_1 = 2M_2 = 128$. It can be seen that the optimal ratio is not very sensitive to the exact value of k.

From (9), the SQNR of an IADC3 with the same conversion time is

$$SQNR_3 \approx 3\cdot 20\ \log(M) + 20\ \log(L-1) - 20\ \log(6) \tag{18}$$

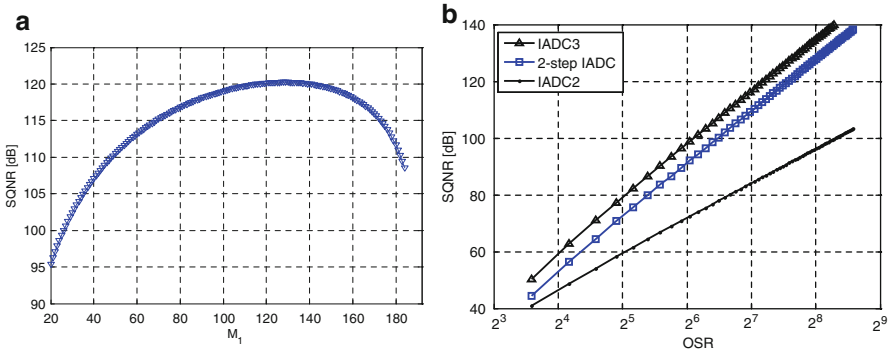

Fig. 7 (**a**) Simulated SQNR versus OSR of the first step (M_1). The input amplitude is −6 dBFS. (**b**) Simulated SQNR versus OSR for a single-loop IADC3, IADC2 and the proposed two-step IADC2. All the IADCs are assumed to have a five-level quantizer, and are tested at −6 dBFS input signal amplitude

Comparison of $SQNR_{21}$ and $SQNR_3$ shows that the two-step IADC2's SQNR is 7 dB lower than that of an IADC3. However, its noise shaping is nearly one order higher than that of a single-loop IADC2. Figure 7b compares the simulated SQNR versus OSR curves for a single-loop IADC2, a single-loop IADC3 and the two-step IADC2. For OSR = 128, an IADC2 can achieve 85 dB, and an IADC3 can achieve 117 dB with a −6 dBFS input signal. Reusing the hardware of an IADC2 in a two-step operation, results in $SQNR_{21}$ ∼110 dB, 27 dB higher than $SQNR_2$. Note also that the IADC3 will be overloaded by a −6 dBFS input signal, unless a high-resolution internal quantizer is used. A conventional 2-1 MASH modulator can mitigate the stability issue, but it requires three opamps to achieve third-order noise-shaping performance.

In the proposed two-step operation, the first-step IADC2 is operated only for 2/3 of the total conversion time. The SQNR loss is compensated by the second-step IADC1 operation. The energy efficiency is thereby improved significantly. The higher the OSR, the more significant is the resulting SQNR improvement. The extra circuit cost is low: only an additional timing control is needed to switch the hardware between the two steps. The circuit configuration is much less complex than previously reported hardware-sharing extended-counting schemes [7, 8, 15].

Generally, if the two-step architecture is applied to an *Nth*-order IADC, its performance will be boosted up to nearly that of a $(2N-1)th$-order one. By using an IADC3 in a two-step operation, as shown in Fig. 8a, an IADC3 performs the first step, and then it is re-configured as an IADC2 for the second step, as shown in Fig. 8b. Figure 8c plots the simulated SQNR of the two-step IADC3 versus the total OSR. Compared to a single-loop IADC3 and IADC2, the two-step IADC3's performance is indeed nearly equal to that of an IADC5. The optimal SQNR can be achieved for an OSR ratio 3:2, which can be derived as in (16). However, the improvement is more significant when the OSR is higher.

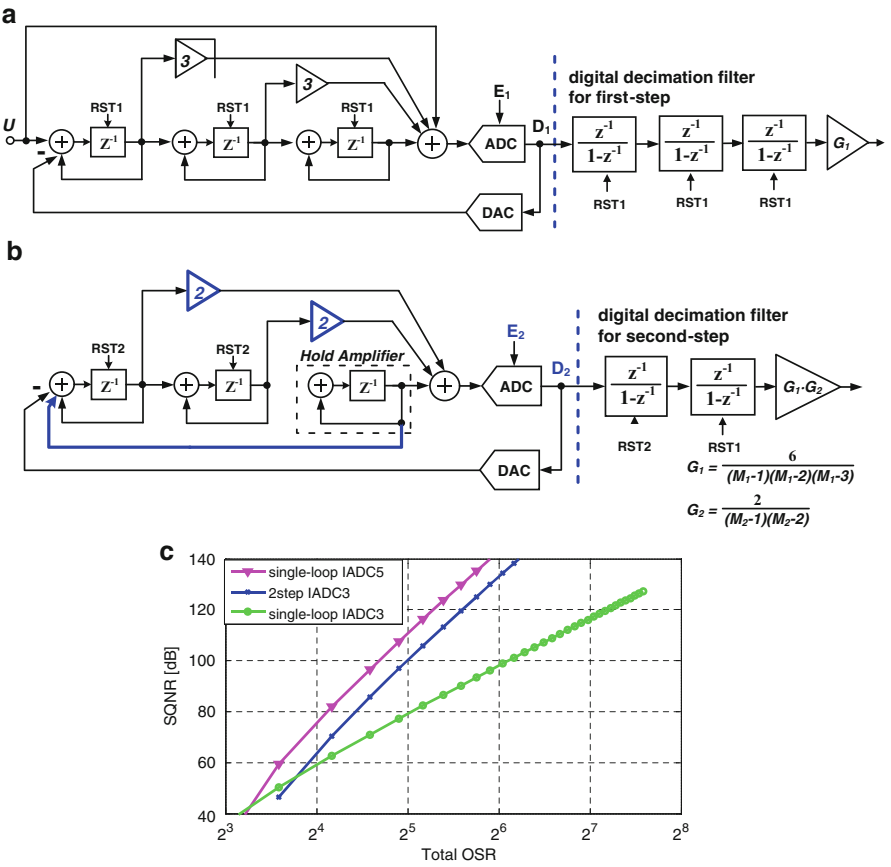

Fig. 8 The IADC3 in two step operation. (**a**) First step. (**b**) Second step. (**c**) Simulated SQNR versus single-loop IADC5 and IADC3

In [24], an algorithmic IADC was proposed with similar two-step operation. However, it requires an extra sample-and-hold stage, and also an additional clock phase to feed back the residue voltage. This complicates the circuit implementation. In our proposed two-step IADC, neither an additional phase, nor an extra active component is needed. All components are reused to accomplish higher SQNR performance, and the power consumption remains the same.

4.1 Multi-Step Operation by an IADC2

The two-step operation can be extended to multiple steps. An example using an IADC2 is shown in Fig. 9 [25]. One more integrator is added to store the residue

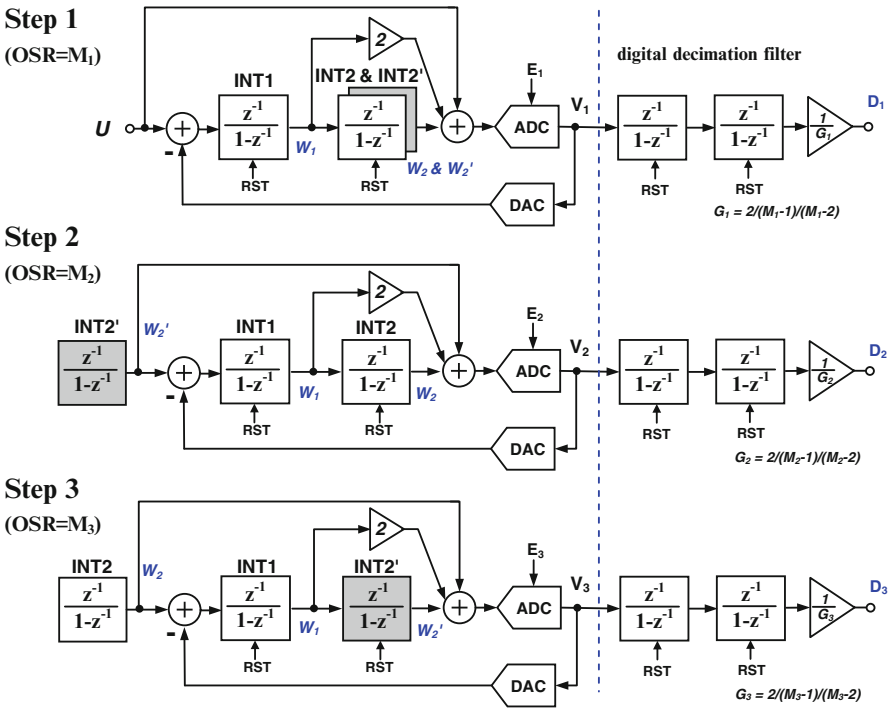

Fig. 9 An example of a multi-step IADC2 [25]

voltage during the first-step IADC operation lasting M_1 clock periods. In the second step of M_2 clock periods, the circuits is re-configured as an IADC2, and INT2′ holds the residue voltage of step one. In the third step, INT2 and INT2′ exchange roles, and the circuit is re-configured again as an IADC2. In each step, a second-order noise shaping is performed. Hence, after an OSR $= M_1 + M_2 + M_3$ clock periods, the order of noise shaping could be nearly 6. Thus, the conversion time can be reduced significantly.

5 Circuit Design Example of the Two-Step IADC

5.1 Switched-Capacitor Circuitry

When the ADC is implemented in a 65 nm technology, the leakage current of the 1-V core MOS devices degrades the performance of a switched-capacitor circuit operated at a low sampling frequency. However, the leakage current of the 2.5 V I/O devices is only 2 pA/μm, which is low enough even for a high-resolution ADC. Hence, 2.5 V I/O devices were used here to implement the prototype IADC.

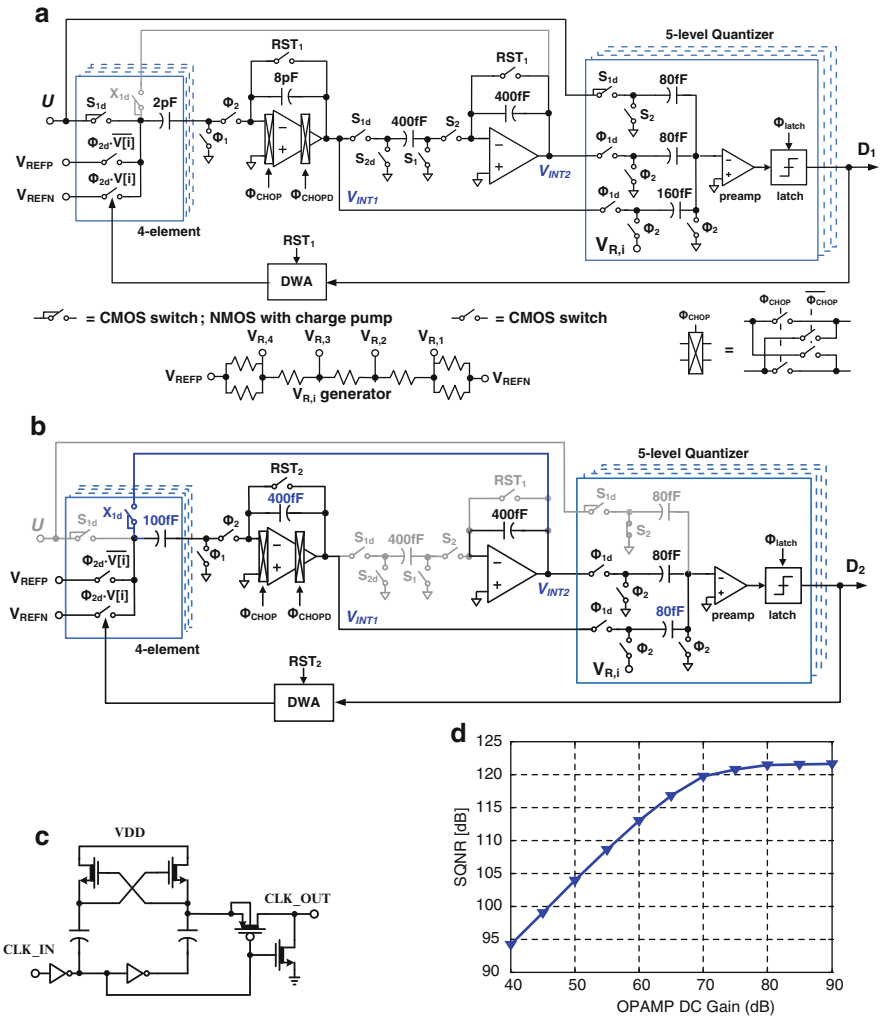

Fig. 10 The equivalent single-ended switched-capacitor circuits implementation of the two-step IADC's modulator. (**a**) First step. (**b**) Second step. (**c**) Voltage doubler. (**d**) Simulated SQNR vs. opamp gain

The switched-capacitor circuit implementation of the proposed two-step IADC's modulator is shown in Fig. 10. Single-ended equivalent circuits are shown for simplicity, but the actual implementation is fully differential. A conventional resistor string was used to generate the five-level reference voltages $V_{R,i}$ for all comparators. To operate the 2.5-V MOS devices with a 1.2-V power supply, the charge pump circuits shown in Fig. 10c were used to double the NMOS gate voltages of the sampling CMOS switches. The I/O devices do not suffer from gate and junction overdrive when operated at 2.5 V, and no extra transistors were needed to improve their reliability.

During the first step lasting $M_1 = 128$ clock periods, as shown in Fig. 10a, the gray-scaled paths are not enabled, and the circuit is working as a conventional IADC2. To achieve a 100 dB SNR, the input sampling capacitor of the first integrator is designed to be 8 pF from kT/C thermal noise consideration [6, 9]. During the second step, for $M_2 = 64$ clock periods, as shown in Fig. 10b the two-phase clocks S_1, S_2 are disabled, and X_1 and X_2 establish different input paths reconfiguring the circuit as a first-order modulator. (In the switched-capacitor circuitry used, it is simple to multiplex the different paths and to perform reconfiguration.) The second integrator (INT2), which is now acting as a hold amplifier, drives the INT1's sampling capacitors. The input sampling capacitors of INT1 can therefore be reduced from 8 to 0.4 pF, to ease the loading of INT2.

Since in our circuit the signal bandwidth is 1–250 Hz, it is sensitive to flicker noise. The first opamp's in-band flicker noise is hence mitigated by chopping, at half of the 96 kHz sampling frequency. The signal is chopped during the middle of integrator sampling phase. The input chopping switches are turned off slightly before the output chopping switches, in order to reduce the signal-dependent charge injection from the output chopping switches. Careful layout techniques were employed to make sure that the in-band residual noise caused by chopper non-idealities is low.

In the proposed two-step IADC (Fig. 6), the bit streams of each step are also separately accumulated and decimated. It has the same advantage as the MASH IADC (Fig. 3): the digital circuitry providing $\left(1 - z^{-1}\right)$ is no longer needed, and the opamp gain is much relaxed. Figure 10d shows the simulated SQNR versus the opamp DC gain. The SQNR begins to degrade only when the opamp DC gain falls below 70 dB. The required opamp gain for the proposed two-step IADC is therefore quite low, even for very high-resolution conversion. Although the loop gain in a third-order system can further relax the opamp gain, a second-order system with moderate relaxation can also save cost, and thus improve efficiency.

The detailed timing diagram for the switched-capacitor circuitry is shown in Fig. 11a. An external 96 kHz clock is used to generate the reset signals RST_1, RST_2 and the control signals EN_{S1}, EN_{S2}. The two-phase non-overlapping clock phases Φ_1 and Φ_2 at 96 kHz are used during both steps, while the S_1, S_2 and X_1, X_2 two-phase clock signals are specifically for the first and second step, respectively. Bottom-plate sampling is used to mitigate the switches' non-idealities. The delayed versions of the two-phase clock signals Φ_{1d}, Φ_{2d}, S_{1d}, S_{2d}, X_{1d}, X_{2d} and Φ_{CHOPD} are omitted for simplicity. The simplified circuit used to generate the control timing and two-phase clocks is shown in Fig. 11b. It uses only frequency dividers and simple logic circuits, and hence it is simple and does not need a complicated state machine to generate the timing controls.

For a total OSR of 192, the two-step IADC2 can ideally achieve 120 dB SQNR for a −6 dBFS input amplitude, which is adequate for a 100 dB SNR ADC. For comparison, a single-loop IADC2 with OSR = 128 and OSR = 192 can achieve only 84 dB and 91 dB SQNR, respectively. Increasing the OSR of an IADC2 from 128 to 192 can give only a 7 dB SNQR improvement, while increasing the order of

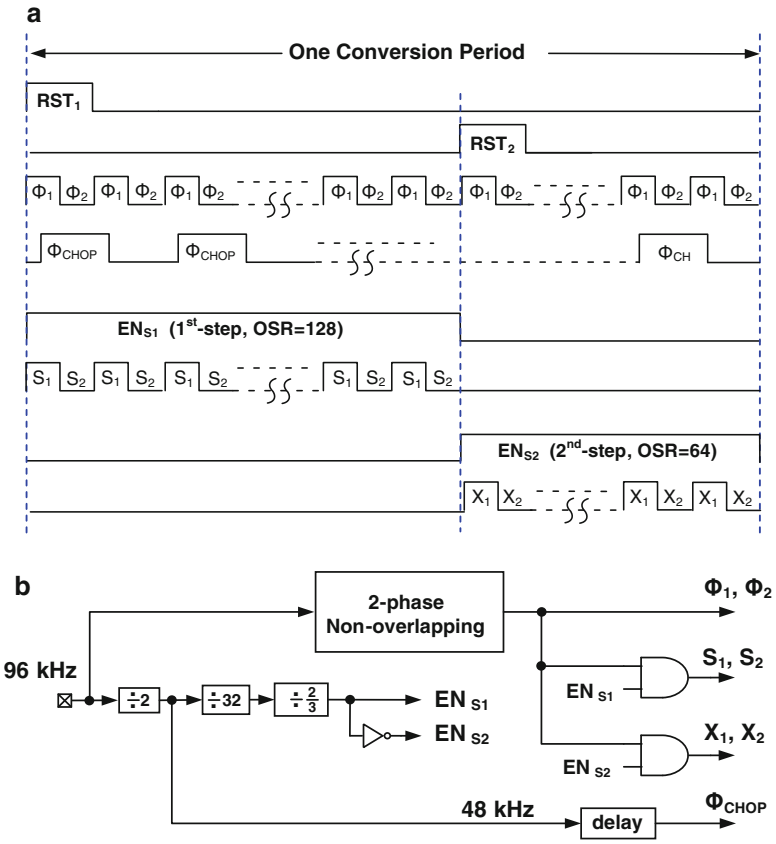

Fig. 11 (**a**) The detailed timing diagrams for the two-step IADC2. (**b**) The circuit for timing control and two-phase non-overlapping clocks

the noise-shaping by 1 can improve the SQNR significantly, by 30 dB. The power penalty for the additional conversion time of 64 clock periods and for the extra control circuitry is small. By just enabling and disabling the control clocks of the switched capacitor circuit, a simple and low-cost operation results.

The digital decimation filter shown in Fig. 6 is not implemented on the chip; the modulator's bit streams were post-processed using MATLAB. The detailed circuit design of the other building blocks can be found in [17].

5.2 Measured Performance

Defining the differential reference 2.4 V_{PP} as 0 dBFS, the measured spectra for a differential 100 μV_{PP} (−87.6 dBFS), 170 Hz, sine-wave input signal are shown in

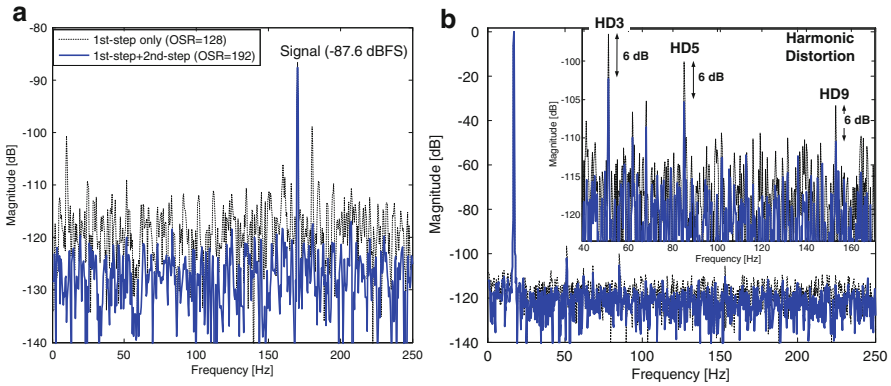

Fig. 12 Measured spectra. The *dotted-line* is for the first step only (IADC2, OSR = 128). The *solid-line* is for the two-step IADC with OSR = 192. (**a**) 100 μV_{PP} (−87.6 dBFS) input amplitude. (**b**) 2.2 V_{PP} (−0.76 dBFS) input amplitude

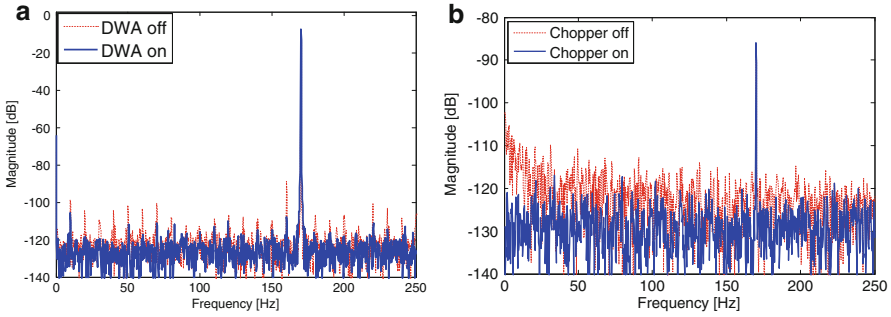

Fig. 13 Measured spectra. (**a**) DWA turned on vs. off with 1 V_{PP} (−6.8 dBFS) input amplitude. (**b**) Chopper on vs. off with 100 μV_{PP} input amplitude

Fig. 12a. The spectra obtained after the first step (OSR = 128) and the second step (OSR = 64) are plotted, showing that the second step enhances the signal-to-noise-and-distortion-ratio (SNDR) by 10.3 dB. Figure 12b shows the measured spectra for a 2.2 V_{PP} (−0.76 dBFS) 17-Hz sine-wave input. The measured SNDR is 84.7 dB for the first step, and 91 dB for two-step operation. Harmonic distortion limits the SNDR for such large signals, and the two-step operation enhances the SNDR by only 7 dB. Figure 13a shows the spectra with the DAC DWA turned on and off. The measured SNDR with a 1 V_{PP} (−7.6 dBFS) input amplitude is 84.6 dB (with the DWA on) and 75.8 dB (DWA off). Nevertheless, the in-band flicker noise degrades the SNR performance significantly. Figure 13b shows the measured spectra with the chopper turned on and off. The chopper stabilization reduces the in-band flicker noise by 11 dB.

The ADC achieves a dynamic range of 99.8 dB and a peak SNDR of 91 dB with a bandwidth from 1 to 250 Hz, consuming only 10.7 μW. Table 1shows a performance

Table 1 Performance summary and comparison

Parameters	[17] **This work**	[27] ESSCIRC '13	[21] TCAS-I '10	[6] JSSC '10	[26] ISSCC '13	[10] JSSC '06
Architecture	**IADC2 + IADC1**	10b SAR + IADC1	IADC2 + 10b cyclic	IADC2 + 11b SAR	Single-loop IADC2	Single-loop IADC3
Process	**65 nm (2.5 V MOS)**	0.6 μm	0.18 μm	0.18 μm	0.16 μm	0.6 μm
Area (mm^2)	**0.20**	1.64	0.50	3.5	0.45	2.08
VDD (V)	**1.2**	3.3	2	1.8	1	3
Sampling freq.	**96 kHz**	5 MHz	115 MHz	45.2 MHz	750 kHz	30.7 kHz
OSR	**192**	256	5	45	80	512
Input range	**2.2 V_{pp}**	2 V_{pp}	3.6 V_{pp}	2 V_{pp}	0.7 V_{pp}	6 V_{pp}
Dyn. range (dB)	**99.8**	84.6	73	90.1	81.9	120
Peak SNDR (dB)	**90.8**	70.7	72	86.3	81.9	120
Bandwidth (Hz)	**250 Hz**	9.75 kHz	11.5 MHz	500 kHz	667 Hz	7.5 Hz
Power	**10.7 μW**	64 μW	48 mW	38.1 mW	20 μW	300 μW
FoM_W (pJ/conv.)	**0.76**	1.17	1.02	1.46	1.48	24.46
FoM_S (dB)	**173.5**	166.4	156.8	161.3	157.1	164.0

summary and comparison with recent state-of-the-art single-loop IADCs [10, 26], as well as with hybrid IADCs using extended-counting schemes [6, 21, 27]. The Walden (FoM_W) and Schreier (FoM_S) figure-of-merits were also calculated, using the formulas

$$FoM_W = \frac{power}{2^{ENOB} \cdot 2BW} \tag{19}$$

$$FoM_S = DR + 10 \cdot \log\left(BW/power\right) \tag{20}$$

For this device, $FoM_W = 0.76$ pJ/conv.-step and $FoM_S = 173.5$ dB were found, both among the best reported results.

6 Conclusions

In this chapter, we first reviewed the design and operation of a conventional single-loop IADC2 using time-domain analysis. The advantages and design considerations of MASH IADCs were also discussed. Using a feedforward modulator, the loop filter accumulates the residue voltage, and stores it at the last integrator's output node. The residue voltage can then be used for fine conversion through an extended counting scheme, which significantly raises the energy efficiency. Several such schemes were reviewed, and their advantages and drawbacks discussed.

To further improve the energy efficiency, we proposed multi-step operation for high-resolution ADCs for use in integrated sensor interface circuits. For example, the components of an *Nth*-order IADC can be re-used to quantize the residue voltage in a second-step operation, resulting in noise-shaping performance close to that of an IADC of order $(2N-1)$. The extra cost is only simple added timing control circuits. Moreover, the required opamp gains can be as low as 60 dB even for 100 dB SNR. The principle can be extended to three- and higher-step operation.

A design example of a two-step IADC2 was demonstrated. The ADC was fabricated using 2.5 V I/O MOS devices in a 65-nm technology, and operated with a 1.2 V power supply. The measured performance showed a 100 dB dynamic range and 91 dB maximum SNDR for a signal bandwidth from 1 to 250 Hz. The device consumed only 10.7 μW. The measured Walden and Schreier FoMs were 0.76 pJ/conversion-step and 173.5 dB, respectively, among the best published IADC FoMs. The active area is 0.2 mm^2, which is the smallest among published designs. The results verify that the proposed two-step IADC is a very area- and energy-efficient solution for integrated sensor systems.

References

1. Wu R, Chae Y, Huijsing JH, Makinwa KAA (2012) A 20-bit ±40mV range read-out IC with 50-nV offset and 0.04% gain error for bridge transducers. IEEE J Solid-State Circuits 47(9):2152–2163
2. Tan Z, Shalmany SH, Meijer GCM, Pertijs MAP (2012) An energy-efficient 15-bit capacitive-sensor interface based on period modulation. IEEE J Solid-State Circuits 47(7):1703–1711
3. Tan Z, Deval P, Daamen R, Humbert A, Ponomarev YV, Chae Y, Pertijs MAP (2013) A 1.2-V 8.3-nJ CMOS humidity sensor for RFID applications. IEEE J Solid-State Circuits 48(10):2469–2477
4. Van Helleputte N et al (2011) A 345 μW multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction and integrated DSP. IEEE J Solid-State Circuits 50(1):230–244
5. Chen C-H, Crop J, Chae J, Chiang P, Temes GC (2012) A 12-bit 7 μW/channel 1 kHz/channel incremental ADC for biosensor interface circuits. In: Proceedings of the IEEE international symposium on circuits and systems (ISCAS), pp 2969–2972
6. Agah A, Vleugels K, Griffin PB, Ronaghi M, Plummer JD, Wooley BA (2010) A high-resolution low-power oversampling ADC with extended-range for bio-sensor arrays. IEEE J Solid-State Circuits 45(6):1099–1110
7. Kim J-H et al (2012) A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor. In: IEEE ISSCC digest of technical papers, pp 390–392
8. Oike Y, El Gamal A (2013) CMOS image sensor with per-column sigma delta ADC and programmable compressed sensing. IEEE J Solid-State Circuits 48(1):318–328
9. Markus J, Silva J, Temes GC (2004) Theory and applications of incremental delta sigma converters. IEEE Trans Circuits Syst I 51(4):678–690
10. Quiquempoix V, Deval P, Barreto A, Bellini G, Markus J, Silva J, Temes GC (2006) A low-power 22-bit incremental ADC. IEEE J Solid-State Circuits 41(7):1562–1571
11. Kavusi S, Kakavand H, El Gamal A (2006) On incremental sigma-delta modulation with optimal filtering. IEEE Trans Circuits Syst I 53(5):1004–1015
12. Caldwell TC, Johns DA (2010) Incremental data converters at low oversampling ratios. IEEE Trans Circuits Syst I 57(7):1525–1537
13. Robert J, Deval P (1988) A second-order high-resolution incremental A/D converter with offset and charge injection compensation. IEEE J Solid-State Circuits 23(3):736–741
14. Harjani R, Lee TA (1998) FRC: a method for extending the resolution of Nyquist rate converters using oversampling. IEEE Trans Circuits Syst II 45(4):482–494
15. Maeyer JD, Rombouts P, Weyten L (2004) A double-sampling extended-counting ADC. IEEE J Solid-State Circuits 39(3):411–418
16. Chen C-H, Zhang Y, He T, Chiang P, Temes GC (2014) A 11 μW 250 Hz BW two-step incremental ADC with 100 dB DR and 91 dB SNDR for integrated sensor interfaces. In: IEEE custom integrated circuits conference (CICC)
17. Chen C-H, Zhang Y, He T, Chiang P, Temes GC (2015) A micro-power two-step incremental analog-to-digital converter. IEEE J Solid-State Circuits 50(8)
18. Carbone P, Xu F, Kiaei S, Temes GC (2014) Incremental and extended-range data converters. In: Design, modeling and testing of data converters. Springer, Berlin, pp 143–159
19. Schreier R, Temes GC (2005) Understanding delta-sigma data converters. IEEE Press/Wiley, Pascataway
20. Fujimori I et al (2000) A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8× oversampling ratio. IEEE J Solid-State Circuits 35(12):1820–1828
21. Lee CC, Flynn MP (2011) A 14b 23 MS/s 48 mW resetting ΔΣ ADC. IEEE Trans Circuits Syst I 58(6):1167–1177
22. Chae Y, Souri K, Makinwa KA (2013) A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset. IEEE J Solid-State Circuits 48(12):3019–3027

23. Chen C-H, Zhang Y, Jung Y, He T, Ceballos JL, Temes GC (2013) Two-step incremental analogue-to-digital converter. Electron Lett 49(4):250–251
24. Mulliken G, Adil F, Cauwenberghs G, Genov R (2002) Delta-sigma algorithmic analog-to-digital conversion. In: Proceedings of the IEEE international symposium on circuits and system (ISCAS), pp 687–690
25. He T, Zhang Y, Meng X, Chen C-H, Temes GC (2015) Micro-power multi-step incremental ADCs for multi-channel sensor interfaces. In: Proceedings of the IEEE international symposium on circuits and systems (ISCAS), 2015, to appear
26. Chen C, Tan Z, Pertijs MAP (2013) A 1V 14b self-timed zero-crossing-based incremental $\Delta\Sigma$ ADC. In IEEE ISSCC digest of technical papers, pp 274–275
27. Ha S et al (2013) 85 dB dynamic range 1.2 mW 156 kS/s biopotential recording IC for high-density ECoG flexible active electrode array. In: Proceedings of the European solid-state circuits conference (ESSCIRC)

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