

Chapter 2

Design and Implementation of Ultra-Low-Power ZigBee/WPAN Receiver

In recent years, the proliferation of short-range wireless applications for Internet of Things and personal healthcare calls for ultra-low power and cost CMOS radios [1]. Ultra-low voltage (ULV) designs have been one of the key directions to approach a better power efficiency [2–5]. Regrettably, an ULV supply will limit the voltage swing, and device's f_T and overdrives, deteriorating the spurious-free dynamic range (SFDR) while necessitating area-hungry inductors (or transformers) to assist the bias and tune out the parasitic capacitances. This chapter describes the design and implementation of a compact, low-power and high-SFDR receiver suitable for ZigBee or wireless personal area network (WPAN) applications. The research background can be outlined as follows.

Four potential ultra-low-power receiver architectures are shown in Fig. 2.1. The first (Fig. 2.1a) employs a single low-noise transconductance amplifier (single-LNTA) followed by two passive I/Q mixers and transimpedance amplifiers (TIAs). If a 50 %-duty-cycle local oscillator (50 % LO) is applied, this topology can suffer from image current circulation between the I and Q paths, inducing I/Q crosstalk, unequal high-side and low-side gains, IIP2 and IIP3 [6]. Lowering the LO duty cycle to 25 % (Fig. 2.1b) can alleviate such issues [7], at the expense of extra sine-to-square LO buffers and logic operation. Another alternative is to add two signal buffers before the mixers (Fig. 2.1c), but they must be linear enough (i.e., more power) to withstand the voltage gain of the low-noise amplifier (LNA) [8, 9]. The basis of our proposed solution (Fig. 2.1d) is to split the LNTA into two, such that a single-ended RF input is maintained, while allowing isolated passive mixing that facilitates the use of a 50 % LO for power savings.

This chapter is organized as follows: Sect. 2.1 will give an overview of the operating principle of the proposed “split-LNTA + 50 % LO” receiver. An analytical comparison of it with the existing “single-LNTA + 25 % LO” architecture will be presented in Sect. 2.2. In Sect. 2.3, a number of circuit techniques will be proposed, including: (1) a low-power voltage-mode transimpedance amplifier (TIA) to enhance the out-channel linearity both at RF and baseband (BB); (2) a mixed-supply (V_{DD}) design approach [10] to alleviate the design trade-offs in RF LNTA (power, gain and noise) and BB TIA (power, linearity and signal swing); (3) a low-power LO generation scheme that consists of a LC voltage-controlled oscillator (VCO) and an input-impedance-boosted Type-II RC-CR network. They

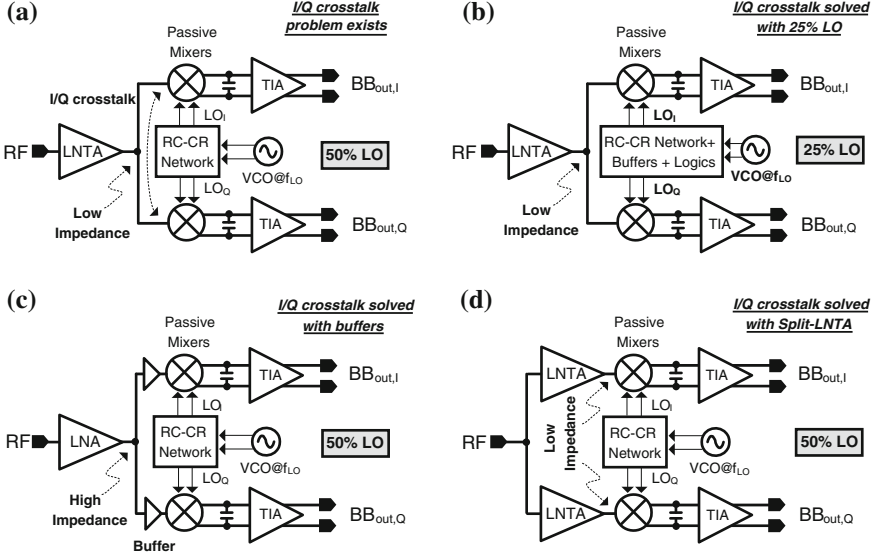


Fig. 2.1 Four potential receiver architectures: **a** Single-LNTA + 50 % LO. **b** Single-LNTA + 25 % LO. **c** Single-LNA + 50 % LO + signal buffers. **d** Split-LNTA + 50 % LO (proposed)

optimize the VCO's output swing with the LC tank's quality factor, while offering adequate I/Q accuracy at low power. The measured experimental results will be reported in Sect. 2.4.

2.1 Proposed “Split-LNTA + 50 % LO” Receiver

The split-LNTA (Fig. 2.2) is based on two self-biased inverter-based amplifiers (M_1 , M_2 and R_F), which have no inner parasitic pole. They also can take the speed advantage of fine linewidth CMOS to lower the device overdrive voltages, featuring a high g_m -to- I_d efficiency at low V_{DD} ($V_{DD06} = 0.6$ V). Its single-ended RF input avoids the RF balun and its associated insertion loss. In front of the split-LNTA, a proper co-design between the RF input capacitance (C_{in}) and bond wire (L_{bw}) facilitates the input impedance matching, while offering a passive pre-gain (A_v) decisively important to the NF and power efficiency. The two LNTAs convert the RF signal (v_{in}) into two equal currents $i_{out,I}$ and $i_{out,Q}$ for the I and Q channels, respectively. To avoid the parasitic and area impact from AC coupling, $i_{out,I}$ and $i_{out,Q}$ are directly DC-coupled to the passive mixers (M_3 and M_4). As long as the DC current passing through M_3 and M_4 is kept small, the $1/f$ noise induced by the mixers can be minimized [11]. This aim can be achieved by matching the output common-mode level of the LNTA to that of the BB TIA.

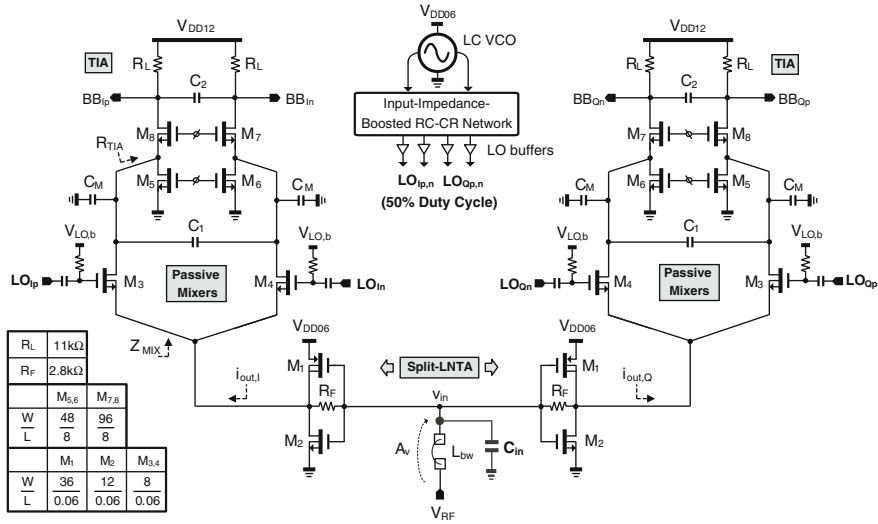


Fig. 2.2 Schematic of the proposed receiver exploiting passive pre-gain, split-LNTA, passive mixers, 50 % LO and common-gate TIAs

The 50 % 4-phase LO ($LO_{Ip,n}$ and $LO_{Qp,n}$) is generated by a 2.4-GHz LC VCO followed by a new type-II RC-CR network, which features a capacitor divider at the input to boost the input impedance. When driving the LO to the mixers (M_3 and M_4), a proper DC level ($V_{LO,b}$) can optimize the switching time. The down converted low-IF (2 MHz) signal is further amplified by a common-gate TIA ($M_{5,8}$ and R_L), which uses a 1.2 V (V_{DD12}) supply to accommodate more signal swing and enhance linearity. Here, we assume a complex low-IF filter will follow the BB TIA, rendering the $1/f$ noise and IIP2 not significant and will not be further addressed. Due to the bidirectional transparency of passive mixers [7, 8], the BB capacitors (C_1 and C_M) can enhance the selectivity at both RF (the output of the LNTA) and BB, improving the out-band linearity. The grounded C_M also helps to suppress the common-mode RF feed through, which is limited by the bond wire inductance that appears in series with C_M under common-mode operation.

2.2 Comparison of “Split-LNTA + 50 % LO” and “Single-LNTA + 25 % LO” Architectures

This Section presents an analytical comparison of the two architectures: “split-LNTA + 50 % LO” and “single-LNTA + 25 % LO”. For brevity, “50 % LO” and “25 % LO” are exploited to represent them, respectively. Figure 2.3a, b show their simplified equivalent circuits. For a fair comparison, the two LNTAs in Fig. 2.3a are modeled as g_m (transconductance) and $2R_{out}$ (output resistance),

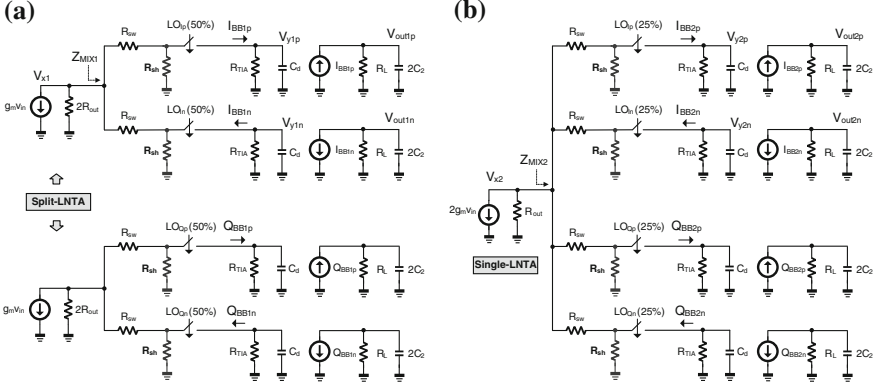


Fig. 2.3 Small-signal equivalent circuits. **a** Split-LNTA + 50 % LO. **b** Single-LNTA + 25 % LO

whereas the single LNTA in Fig. 2.3b is modeled as $2g_m$ and R_{out} . These models are developed under the same approach described in [12–14], where the harmonic up-conversion in passive mixers is modeled as R_{sh} . The impedances looking into the 50 %-LO and 25 %-LO mixers are denoted as Z_{MIX1} and Z_{MIX2} , respectively. Each mixer features an on-resistance of R_{sw} . R_{TIA} is the input resistance of the TIA. The single-ended differential mode capacitance is denoted as $C_d (=C_M + 2C_1)$.

2.2.1 Gain

For Fig. 2.3a, we summarize in (2.1)–(2.5) the derived expressions of both Z_{MIX1} and the voltage gain ($A_{V_{X1}}$) at V_{x1} at the LO + IF frequency ($\omega_{LO} + \omega_{IF}$); the baseband output current (I_{BB1}) with respect to v_{in} ; the voltage gain ($A_{V_{Y1}}$) at $V_{y1p,n}$, and finally the voltage gain ($A_{V_{out1}}$) at $V_{out1p,n}$,

$$Z_{MIX1}|_{@(\omega_{LO} + \omega_{IF})} \approx R_{sw} + \left(\frac{2Z_{BB}}{\pi^2} // R_{sh} \right) \quad (2.1)$$

$$\text{where } Z_{BB} = \frac{1}{s(2C_1 + C_M)} // R_{TIA}; R_{sh} \approx \frac{2}{3}(2R_{out} + R_{sw})$$

$$A_{V_{X1}}|_{@(\omega_{LO} + \omega_{IF})} \approx g_m(2R_{out} // Z_{MIX1}) \quad (2.2)$$

$$\frac{I_{BB1}}{v_{in}}|_{DC} = \frac{I_{BB1p} - I_{BB1n}}{v_{in}} \approx g_m \frac{2R_{out}}{R_{TIA} + 2(2R_{out} + R_{sw})} \frac{4}{\pi} = G_{m1} \quad (2.3)$$

$$A_{V_{Y1}}|_{DC} = A_{V_{Y1p}} - A_{V_{Y1n}} \approx G_{m1} R_{TIA} \quad (2.4)$$

$$A_{V_{out1}}@DC = A_{V_{out1p}} - A_{V_{out1n}} \approx G_{m1}R_L \quad (2.5)$$

Similarly, for Fig. 2.3b, we have (2.6)–(2.10) the derived expressions of both Z_{MIX2} and the voltage gain ($A_{V_{x2}}$) at V_{x2} at the LO + IF frequency ($\omega_{LO} + \omega_{IF}$); the baseband output current (I_{BB2}) with respect to v_{in} ; the voltage gain ($A_{V_{y2}}$) at $V_{y2p,n}$, and finally the voltage gain ($A_{V_{out2}}$) at $V_{out2p,n}$,

$$Z_{MIX2}|@(\omega_{LO} + \omega_{IF}) \approx R_{sw} + \left(\frac{2Z_{BB}}{\pi^2} // R_{sh} \right) \quad (2.6)$$

$$\text{where } Z_{BB} = \frac{1}{s(2C_1 + C_M)} // R_{TIA}; R_{sh} \approx 4(R_{out} + R_{sw})$$

$$A_{V_{x2}}@(\omega_{LO} + \omega_{IF}) \approx 2g_m(R_{out} // Z_{MIX2}) \quad (2.7)$$

$$\frac{I_{BB2}}{v_{in}}@DC = \frac{I_{BB2p} - I_{BB2n}}{v_{in}} \approx 2g_m \frac{R_{out}}{R_{TIA} + 4(R_{out} + R_{sw})} \frac{4\sqrt{2}}{\pi} = G_{m2} \quad (2.8)$$

$$A_{V_{y2}}@DC = A_{V_{y2p}} - A_{V_{y2n}} \approx G_{m2}R_{TIA} \quad (2.9)$$

$$A_{V_{out2}}@DC = A_{V_{out2p}} - A_{V_{out2n}} \approx G_{m2}R_L \quad (2.10)$$

Note that the output capacitance of the LNTA was neglected. In fact, the output capacitance of LNTA will induce C_{out} and $2C_{out}$ for the g_m and $2g_m$ LNTA stages, respectively. This will render the output impedance ratio at V_{x1} and V_{x2} slightly larger than 2. Besides, the parasitic capacitor will affect R_{sh} too. The proposed separated gm stage imposes a smaller C_{out} and thus lowers the degradation of gain and NF when compared with those predicted by Eqs. (2.11) and (2.12). With proper sizing, it would be possible to achieve $R_{sw} \ll R_{out}$ and $R_{sw} \ll R_{TIA}$ and R_L , such that the gain difference between 25 % LO and 50 % LO at different RF and BB nodes can be estimated as,

$$\begin{aligned} \Delta A_{V_{x1,2}}@ \omega_{LO} &= 20 \log A_{V_{x2}} - 20 \log A_{V_{x1}} \approx 20 \log \frac{2(R_{out} // \frac{2R_{TIA}}{\pi^2} // 4R_{out})}{2R_{out} // \frac{2R_{TIA}}{\pi^2} // \frac{4R_{out}}{3}} = 6 \text{ dB} \\ \Delta A_{V_{y1,2}}@DC &= 20 \log A_{V_{y2}} - 20 \log A_{V_{y1}} = 20 \log \left(\sqrt{2} \frac{R_{TIA} + 4R_{out} + 2R_{sw}}{R_{TIA} + 4R_{out} + 4R_{sw}} \right) \approx 3 \text{ dB} \\ \Delta A_{V_{out1,2}}@DC &= 20 \log A_{V_{out2}} - 20 \log A_{V_{out1}} = 20 \log \left(\sqrt{2} \frac{R_L + 4R_{out} + 2R_{sw}}{R_L + 4R_{out} + 4R_{sw}} \right) \approx 3 \text{ dB} \end{aligned} \quad (2.11)$$

From (2.11), the 25 % LO should have a higher gain at both RF and BB nodes than the 50 % LO. However, as analyzed in Sect. 2.3.3, a higher gain at RF will penalize the IIP3, while a higher BB gain can be achieved easily by using a larger R_L . Regarding the impact of these gain differences to the NF it will be analyzed next.

2.2.2 NF

The NF is analyzed according to the equivalent LTI noise model [12–14]. As shown in Fig. 2.4a, b, the four noise sources are the thermal noises from R_s ($V_{n,Rs}^2 = 4kTR_s$), LNTA ($I_{n,gm}^2 = 4kT\gamma_1 g_m$ or $I_{n,2gm}^2 = 4kT\gamma_1 2g_m$), R_{sw} ($V_{n,sw}^2 = 4kTR_{sw}$) and the noise from TIA is $V_{n,TIA}^2 \approx 4kT\gamma_2/g_{m_TIA} \approx 4kT\gamma_2 R_{TIA}$, given that the output impedance of the mixer is sufficiently large. Here, g_{m_TIA} is the transconductance of the bias transistor for the TIA, while the noise from the CG device is degenerated. An accurate model of the TIA noise can be found in [11]. The noise of R_F is ignorable and the noise coupling between the I and Q paths under a 50 % LO is minor (confirmed by simulations), easing the NF calculation of each path separately. The noise factor (F) can be found by dividing the total output noise by the portion related with R_s contribution,

$$F = 1 + \frac{\gamma_1}{R_s A_v^2 G_m} + \frac{R_{sw}}{R_s A_v^2 G_m^2 R^2} + \frac{(R + R_{sw})^2}{R_s A_v^2 G_m^2 R^2 \beta \gamma_2 R_{TIA}} + \frac{a \gamma_1}{R_s A_v^2 G_m} + a + \frac{a R_{sw}}{R_s A_v^2 G_m^2 R^2} \quad (2.12)$$

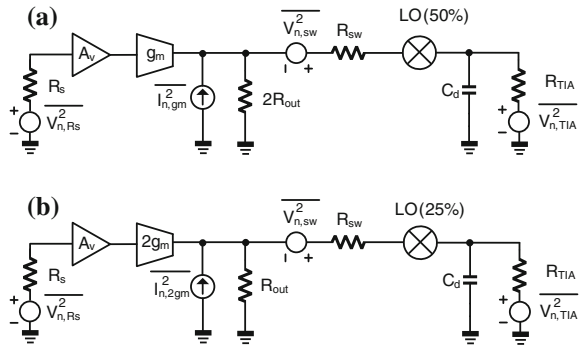
where $\beta = \frac{2}{\pi^2}$ is the down conversion scaling factor and a is the harmonic folding factor,

$$a = \left(\frac{\pi^2}{4} - 1 \right), G_m = g_m \text{ and } R = 2R_{out} \text{ for Fig.2.4(a)}$$

$$a = \left(\frac{\pi^2}{8} - 1 \right), G_m = 2g_m \text{ and } R = R_{out} \text{ for Fig.2.4(b)}$$

In (2.12), the 2nd term is from the LNTA, the 3rd term is from the mixer, and the 4th term is from the TIA. The rest of the terms are the noise folding from the odd harmonics of the LO for LNTA, R_s and R_{sw} , respectively. The NF calculated from

Fig. 2.4 Equivalent LTI noise model with pre-gain for **a** 50 % LO (Fig. 2.3a) and **b** 25 % LO (Fig. 2.3b)



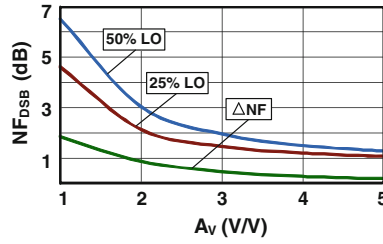


Fig. 2.5 Simulated NF_{DSB} and ΔNF against A_V for 50 % LO and 25 % LO

(2.12) for 50 % LO is single sideband (SSB). For a double sideband (DSB) NF, it is 3 dB less. Since the harmonic's power of 50 % LO is larger than that of 25 % LO, the folding terms of 50 % LO are also higher. From (2.12), the DSB NF of 50 % LO and 25 % LO are plotted in Fig. 2.5 as a function of A_V , where $\Delta NF = NF_{50\%} - NF_{25\%}$. $R_{sw} = 50 \Omega$, $\gamma_1 = \gamma_2 = 1$, $g_m = 9 \text{ mS}$, $R_{out} = 200 \Omega$ and $R_{TIA} = 2.5 \text{ k}\Omega$. It can be seen that ΔNF is reduced to 0.91 dB (0.51 dB) when A_V is just 2 V/V (3 V/V), which is easily achievable in practice. In fact, a moderated A_V can even eliminate the need of the LNTA (or LNA) [3]. However, when considering also the input matching and LO-to-RF isolation, both pre-gain and LNTA should be employed concurrently. The simulated LO-to-RF isolation is $< -100 \text{ dBm}$. Due to the passive pre-gain, the IIP3 of the receiver is more demanding than the NF, promoting the use of a 50 % LO. Together with its power advantage (i.e. lower VCO frequency and no divider), our proposed topology (i.e., pre-gain + split-LNTA + 50 % LO) should ease the tradeoff between NF, IIP3, area and power.

2.2.3 IIP3

The 3rd-order intermodulation (IM3) distortion is analyzed to assess the linearity. The aim is to find the in-band IIP3 of the receiver under 50 % LO and 25 % LO in response to two-tone excitation. Assuming that the nonlinearity of the receiver is dominated by the LNTA, its nonlinearity contributions are considered as:

- (a) 3rd-order LNTA nonlinearity due to input excitation v_{in} [$\alpha_2 (I/V^3)$].
- (b) 3rd-order LNTA nonlinearity due to output excitation v_x [$\alpha_3 (I/V^3)$].

Thus, $i_{ds} = \alpha_1 v_{in} + \alpha_2 v_{in}^3 + \alpha_3 v_x^3$. If the coefficients α_1 , α_2 and α_3 are assumed to be proportional to the device W/L ,

For 50 % LO, $\alpha_1 = g_m$, $\alpha_2 = g_{m3}$, $\alpha_3 = g_{o3}$;

For 25 % LO, $\alpha_1 = 2g_m$, $\alpha_2 = 2g_{m3}$, $\alpha_3 = 2g_{o3}$.

where g_{m3} and g_{o3} are the 3rd-order nonlinear transconductance and conductance, respectively. With a two-tone excitation of amplitude A and the 1st-order voltage

gain and current gain given in (2.1)–(2.11), the IM3 output voltage for each of the nonlinear coefficients listed above can be written as,

$$v_{o3z2} = \frac{3}{4} g_{m3} A^3 I_{BB1} R_L; \quad v_{o3z3} = \frac{3}{4} g_{o3} A_{V \times 1}^3 A^3 I_{BB1} R_L$$

for a 50 % LO. Thus,

$$\text{IM}_{3_50\%} = \frac{v_{o3z2} + v_{o3z3}}{v_{01z1}} = \frac{\frac{3}{4} g_{m3} A^3 I_{BB1} R_L + \frac{3}{4} g_{o3} A_{V \times 1}^3 A^3 I_{BB1} R_L}{A g_m I_{BB1} R_L}$$

Let $\text{IM}_{3_50\%} = 1 \rightarrow \text{IIP}_{3_50\%} = \sqrt{\frac{4g_m}{3(g_{m3} + g_{o3}A_{V \times 1}^3)}} \quad (2.13)$

Following the same procedure, the IIP3 for 25 % LO can be derived as,

$$\text{IIP}_{3_25\%} = \sqrt{\frac{4g_m}{3(g_{m3} + g_{o3}A_{V \times 2}^3)}} \quad (2.14)$$

Since $A_{V \times 2} > A_{V \times 1}$, we can find that, from (2.13)–(2.14), the LNTA's 3rd-order nonlinearity term is larger for a 25 % LO. Thus, the IIP3 of 50 % LO should be better than that of 25 % LO, benefiting the SFDR since both architectures will feature a similar NF after adding the pre-gain.

2.2.4 Current- and Voltage-Mode Operations

Both 25 % LO and 50 % LO architectures can be intensively designed for current-mode or voltage-mode operation. For a high-performance design like [7, 8, 12], $R_{TIA} \ll R_{out}$ and $R_{sw} \ll R_{out}$ are preferred to keep the signals in the deep current mode. As such, (2.3) and (2.8) can be simplified as $G_{m1} = \frac{2g_m}{\pi}$ and $G_{m2} = \frac{2\sqrt{2}g_m}{\pi}$, respectively. Both of them are higher when compared to themselves in the voltage-mode operation. In terms of IIP3 and NF, the current mode is also preferable since $A_{V \times 1} \approx g_m(R_{sw} + \frac{2}{\pi}R_{TIA})$ and $A_{V \times 2} \approx 2g_m(R_{sw} + \frac{2}{\pi}R_{TIA})$ will be lower, and the noise due to the folding term and TIA will be also smaller as noted in (2.12).

Nevertheless, the current-mode operation also brings up two sizing constraints being less attractive for *low-power* design: (1) a low R_{sw} entails a large device W/L and a higher overdrive voltage for the mixers; both calling for a larger power budget in the LO path, and (2) a low R_{TIA} implies that the TIA has to draw a large bias current. For example, if a low R_{TIA} of 50 Ω is required from the 1.2-V TIA (a common-gate amplifier), its bias current is as high as $I_{bias} = 2$ mA for a typical overdrive voltage of 200 mV. Thus, for ultra-low-power applications like

Table 2.1 Proposed Receiver under current- and voltage-mode operations

Mode	Gain	NF	In-Band IIP3	Power	Suitable for
Current mode (Small R_{sw} & R_{TIA})	\nearrow	\searrow	\nearrow	\nearrow	High performance
Voltage mode (Large R_{sw} & R_{TIA})	\searrow	\nearrow	\searrow	\searrow	Ultra low power

ZigBee/WPAN that has relaxed NF and linearity requirements, higher R_{sw} and R_{TIA} are preferable to operate the receiver more on the voltage mode. A summary of performance differences in current- and voltage-mode operations is given in Table 2.1.

2.3 Circuit Techniques

2.3.1 Impedance Up Conversion Matching

From Sect. 2.2, we expect a passive pre-gain A_v of 2 to 3 V/V. As shown in Fig. 2.6a, A_v can be derived under $R_{in} = R_s$,

$$\frac{V_{out}^2}{2R_{out}} = \frac{V_s^2}{8R_s}, V_{out} = V_{in}A_v, V_{in} = 0.5V_s \Rightarrow A_v = \sqrt{\frac{R_{out}}{R_{in}}}$$

Thus, an up-conversion matching network is entailed to ensure $A_v > 1$. A convenient way to achieve it is to use L_{bw} to resonate with C_{in} . The schematic is shown in Fig. 2.6b. The parallel connection of C_{in} and R_{out} can be transformed into

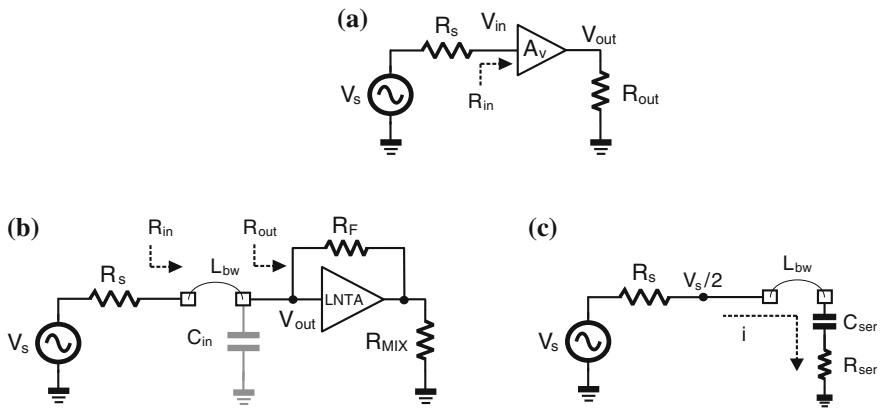


Fig. 2.6 Input impedance matching: **a** A_v converts R_{out} to R_{in} to match with R_s , **b** L_{bw} C_{in} as an impedance conversion network and its **c** narrowband equivalent circuit

a series connection of C_{ser} and R_{ser} , as shown in Fig. 2.6c. At $L_{\text{bw}}C_{\text{ser}}$ resonance, and with $R_{\text{ser}} = R_s$ and $i = \frac{V_s}{2R_{\text{ser}}}$, we have,

$$V_{\text{out}} = V_{R_{\text{ser}}} + V_{C_{\text{ser}}} = \frac{V_s}{2} (1 - j \frac{Q_c}{2})$$

where,

$$V_{R_{\text{ser}}} = -j \frac{Q_c V_s}{2} s C_{\text{ser}} R_{\text{ser}} = \frac{V_s}{2}$$

$$V_{C_{\text{ser}}} = \frac{1}{j \omega_0 C_{\text{ser}}} \frac{V_s}{2 R_{\text{ser}}} = -j \frac{Q_c}{2} V_s,$$

$$\omega_0 = \frac{1}{\sqrt{L_{\text{bw}} C_{\text{ser}}}} \text{ and } Q_c = \frac{\sqrt{L_{\text{bw}}/C_{\text{ser}}}}{R_{\text{ser}}}$$

Interestingly, such a voltage boosting factor $\sqrt{1 + Q_c^2/4}$ is larger than the conventional inductively-degenerated LNA, which is only $\frac{Q_c}{2}$. In fact, when the capacitance of the PCB trace is accounted, the Q of the matching network will be higher, easing the impedance matching.

2.3.2 Mixer-TIA Interface Biased for Impedance Transfer Filtering

For the employed single-balanced passive mixers, the RF-to-IF feed through has to be addressed. Based on Fig. 2.7, we can calculate the currents i_{M7} and i_{M8} with respect to the RF current i_{RF} as given by,

$$i_{M7} = \frac{i_{\text{RF}}}{2} [1 - \text{sign}(\cos \omega_{\text{Lot}})] \quad (2.15)$$

$$i_{M8} = \frac{i_{\text{RF}}}{2} [1 + \text{sign}(\cos \omega_{\text{Lot}})] \quad (2.16)$$

They imply that the currents can be decomposed into the differential mode (Fig. 2.7a) with amplitude of $2i_{\text{RF}}/\pi$ at BB, and into the common mode (Fig. 2.7b) with amplitude of $0.5i_{\text{RF}}$ at RF. To suppress the latter, C_M was added to create a lowpass pole (C_M/R_{TIA}). For the differential IF signal, the pole is located at $(C_M + 2C_1)/R_{\text{TIA}}$, which suppresses the out-of-channel interferers before they enter the TIA. As such, the TIA can be biased under a very small bias current. The resultant high input impedance of the TIA, indeed, benefits both BB and RF

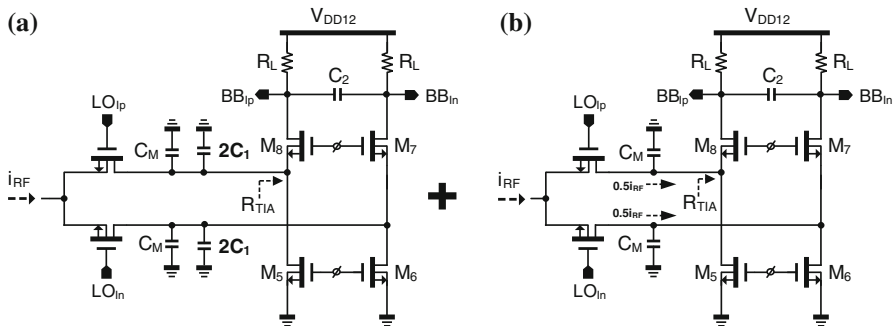


Fig. 2.7 Equivalent circuits of the mixer-TIA interface for **a** the differential low-IF signal and **b** the common-mode RF feed through

filtering because of the bidirectional impedance-translation property of the passive mixers [7, 8]. Figure 2.8 shows the simulated out-band IIP3, which is subject to the allowed total capacitance of $C_M + 2C_1$. For instance, when $C_M + 2C_1$ is increased from 16 to 42 pF, the out-band IIP3 raises from +2.5 to +4.7 dBm, at the expense of the die area. For the on-resistance of the mixer switches (R_{sw}), it involves a tradeoff of the LO path's power to the out-band IIP3 and NF. As shown in Fig. 2.9, if R_{sw} is increased from 50 to 150 Ω for power savings, the NF and out-band IIP3 will be penalized by ~ 1 dB.

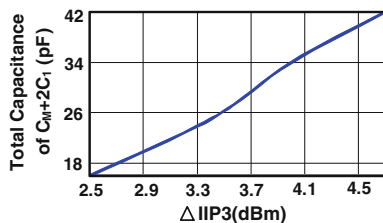


Fig. 2.8 Out-band IIP3 can be improved by allowing more total capacitance of $C_M + 2C_1$

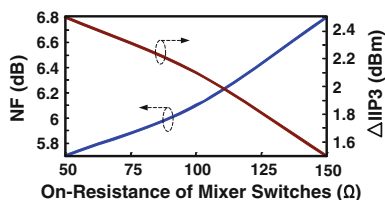


Fig. 2.9 The on-resistance of the mixer switches represents a tradeoff among the LO-path's power, out-band IIP3 and NF

2.3.3 RC-CR Network and VCO Co-Design

The LC VCO (Fig. 2.10a) employs a complementary $NMOS$ - $PMOS$ ($M_{1,4}$) negative transconductor. For power savings, M_1 and M_2 are based on AC-coupled gate bias ($V_{vco,b}$) to lower the supply to 0.6 V. Here, we implement a capacitive divider (C_{M1} and C_{M2}) to boost the input impedance of its subsequent two-stage RC - CR network (Fig. 2.10b). The optimization details are presented next.

RC - CR network is excellent for low-power and narrowband I/Q generation. With a Type-II architecture, both phase balancing and insertion loss can be better optimized than its Type-I counterpart [15]. For instance, the simulated insertion loss of a two-stage Type-II RC - CR network is roughly 2 dB as shown in Fig. 2.11, which will be raised to 4 to 5 dB if a Type-I topology is applied (not shown). For low-power LO buffering, the amplitude balancing is critical because its imbalance will lead to inconsistent zero-crossing points, resulting in AM to duty-cycle

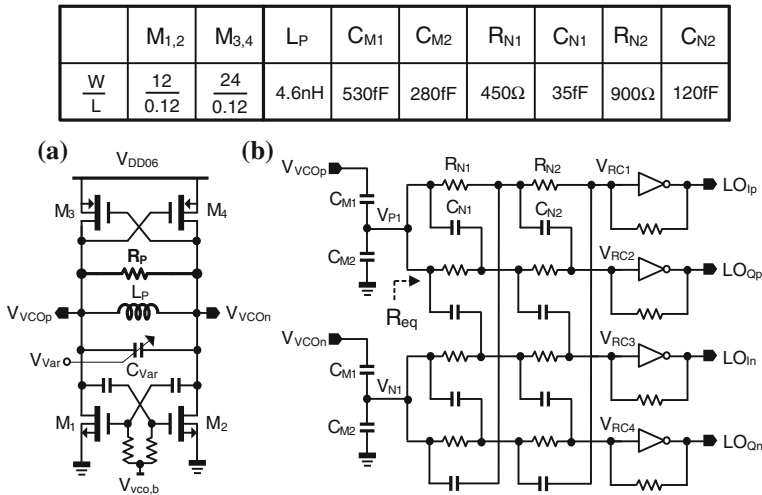


Fig. 2.10 **a** LC VCO and **b** the proposed input-impedance-boosted two-stage Type-II RC - CR network for 4-phase 50 % LO generation

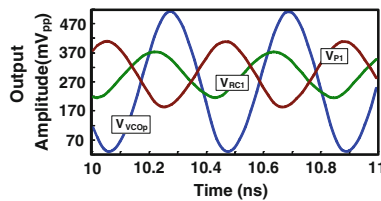


Fig. 2.11 Simulated time-domain signals at the output of the VCO ($V_{vco,p}$), capacitor divider (V_{p1}) and the RC - CR network (V_{RC1})

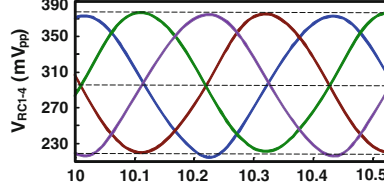


Fig. 2.12 Simulated time-domain signals at V_{RC1-4}

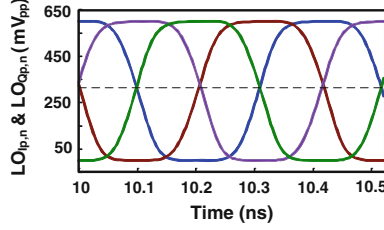


Fig. 2.13 Simulated time-domain signals at $LO_{Ip,n}$ and $LO_{Qp,n}$

distortion. Figures 2.12 (V_{RC1-4}) and 2.13 ($LO_{Ip,n}$ and $LO_{Qp,n}$) are the simulated transient waveforms, showing the consistent duty cycle and zero-crossing points achieved in the proposed design.

For a RC - CR network operated at 2.4 GHz, if we select $R_{N1} = 1 \text{ k}\Omega$, C_{N1} is just 66 fF, which benefits the area, VCO tuning range and phase noise, but the I/Q accuracy over PVT variations should be considered [16]

$$\frac{\sigma(\text{Image Out})}{\text{Desired Out}} = 0.25 \sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2} \quad (2.17)$$

Since ZigBee/WPAN applications call for a low image-rejection ratio (IRR) of 20–30 dB [17], according to (2.17), the matching of the resistors (σ_R) and capacitors (σ_C) can be relaxed to 2.93 % for a 30-dB IRR (3σ). The sizes of $C_{N1,2}$ and $R_{N1,2}$ are summarized in Fig. 2.10. The poles from $C_{N1,2}$ and $R_{N1,2}$ are distributed around 2.4 GHz to cover the PVT variations. The impact of R_{N1} to the VCO can be analyzed as follows:

When the VCO's inductor is 4 nH with a Q of 20 ($R_P \approx 1.2 \text{ k}\Omega$), we have $R_{\text{tank}} \approx 0.5R_P/0.5R_{N1}$. Thus, directly connecting the RC - CR network to the VCO will limit the LC tank's Q_{tank} degrading the phase noise [18, 19]. To alleviate this, we boost up the equivalent input resistance of the RC - CR network (R_{eq}) by adding a capacitive divider (C_{M1} and C_{M2}). For the total tank capacitance C_{tank} , it can be approximated as

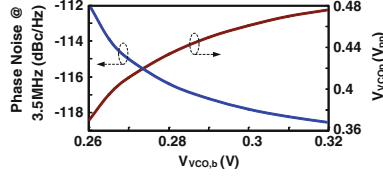


Fig. 2.14 Trade-off between VCO output amplitude and phase noise with respect to $V_{vco,b}$

$$C_{\text{tank}} \approx 2C_{\text{var}} + \frac{(C_{M2} + 2C_{N1})C_{M1}}{C_{M1} + C_{M2} + 2C_{N1}} \quad (2.18)$$

By defining an input-impedance boosting factor n ,

$$n = \frac{C_{M1}}{C_{M1} + C_{M2} + 2C_{N1}} \quad (2.19)$$

we have

$$V_{P1} \approx nV_{VCOp} \quad (2.20)$$

It means that the signal swing (V_{P1}) delivered to the RC - CR network are in trade-off with n . Handily, in our V_{CO} , sweeping $V_{vco,b}$ can track the phase noise with the output swing (Fig. 2.14). Given a bias current and a phase noise target, R_{tank} can be set from $V_{VCOp} \approx 2I_{\text{bias}}R_{\text{tank}}$, and n can be set from (2.21) with a specific R_p and R_{eq} ,

$$R_{\text{tank}} \approx \frac{R_{\text{eq}}}{n} \parallel \frac{R_p}{2} \quad (2.21)$$

In this work, $n = 0.6$ is selected to balance the output swing with C_{tank} and the total tank resistance (R_{tank}).

2.4 Experimental Results

The receiver (Fig. 2.15) fabricated in 65-nm CMOS occupies an active area of 0.14 mm^2 and is encapsulated in a 44-pin CQFP package for PCB-based measurements. The estimated bond wire inductance is $\sim 7 \text{ nH}$ for the provided package ($13.5 \times 13.5 \text{ mm}$). Figure 2.16 shows that the measured S_{11} is -8 dB within 2.24–2.46 GHz (for a different package, external inductor or capacitor can be added to optimize S_{11}). The simulation results with and without considering the PCB trace capacitances are also given. The measured voltage gain is 32.8–28.2 dB and the DSB NF is between 8.6–9 dB for an IF spanning from 1 to 3 MHz, as shown in Fig. 2.17. We also measured the gain and NF from 2.2 to 2.6 GHz (Fig. 2.18).

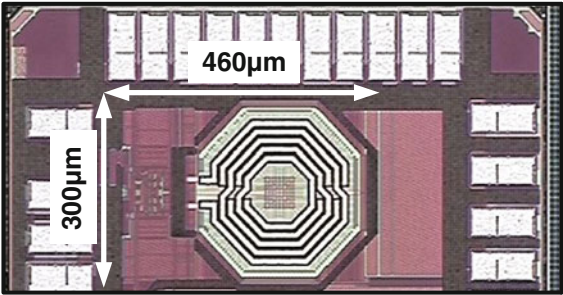


Fig. 2.15 Chip micrograph of the fabricated receiver

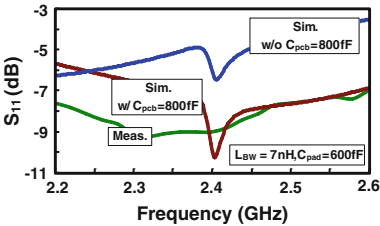


Fig. 2.16 Measured S_{11} , and simulated S_{11} with and without C_{pcb}

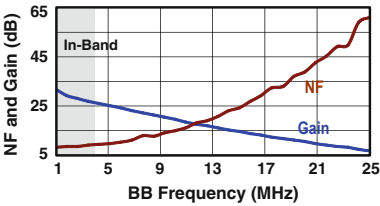


Fig. 2.17 Measured receiver gain and NF versus BB frequency

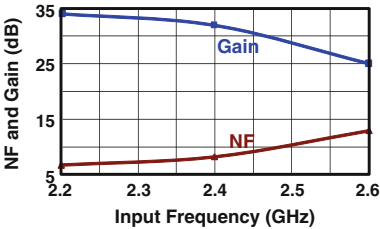


Fig. 2.18 Measured receiver gain and NF versus input signal frequency

For a narrowband receiver, the linearity is mainly justified by the out-channel linearity tests. According to the case given in [17, 20], two tones are applied at $[f_{LO} + 10\text{ MHz}, f_{LO} + 22\text{ MHz}]$ with a power level sweeping from -24 to -32 dBm . Because of the RF and baseband filtering associated with the bidirectional property of passive mixers, the out-band IIP3 (Fig. 2.19) achieves -7 dBm and the $P_{1\text{dB}}$ is -26 dBm .

For the VCO, it measures 21 % tuning range from 2.623 to 2.113 GHz, as shown in Fig. 2.20. At 3.5-MHz offset, the phase noise (Fig. 2.21) is -112.46 dBc/Hz ,

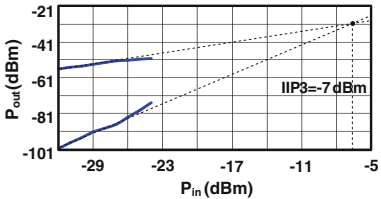


Fig. 2.19 Measured out-of-band IIP3

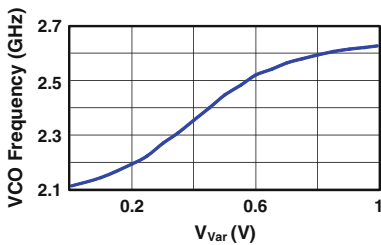


Fig. 2.20 Measured VCO turning range

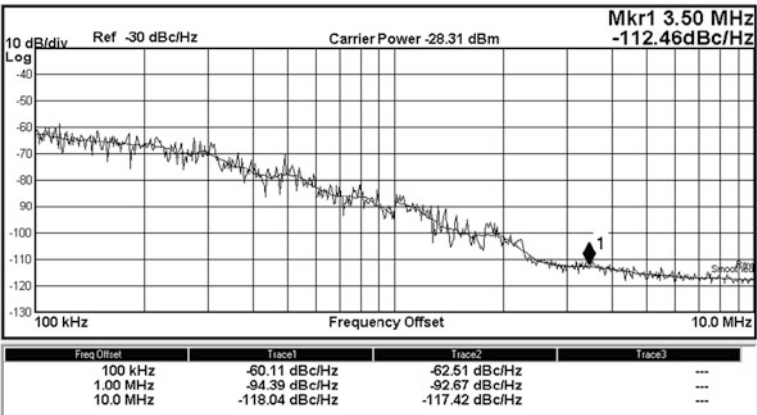


Fig. 2.21 Measured VCO phase noise at 2.4 GHz

fulfilling the specification (-102 dBc/Hz [17, 20]) with an adequate margin. From frequency 100 kHz to 1 MHz, the result fits the $1/f^3$ slope, and from 1 to 10 MHz, it starts to be saturated, primarily limited by the small output amplitude (-28.31 dBm) of the test buffer.

Based on transient measurements, the I/Q BB differential outputs (Fig. 2.22) has ~ 0.08 dB gain mismatch and 2° phase match, corresponding to an IRR of ~ 25 dB.

The performance summary and benchmark are given in Table 2.2 [5, 17, 21–27]. This work [28] succeeds in achieving the highest power and area efficiencies via proposing a mixed- V_{DD} topology co-optimized with a number of circuit techniques. Only one on-chip inductor is entailed in the VCO. The achieved NF and out-band IIP3 correspond to a competitive SFDR of 59.4 dB according to [17, 19],

$$\text{SFDR} = \frac{2(P_{\text{IIP3}} + 174\text{dBm} - \text{NF} - 10\log B)}{3} - \text{SNR}_{\min} \quad (2.22)$$

where $\text{SNR}_{\min} = 4$ dB is the minimum signal-to-noise ratio required by the application, and $B = 2$ MHz is the channel bandwidth. As presented in Figs. 2.8 and 2.9, the SFDR can be further optimized by allowing more budgets in area (bigger $C_M + 2C_1$) and/or power (smaller on-resistance of the mixer switches), being a design-friendly architecture easily adaptable to different specifications.

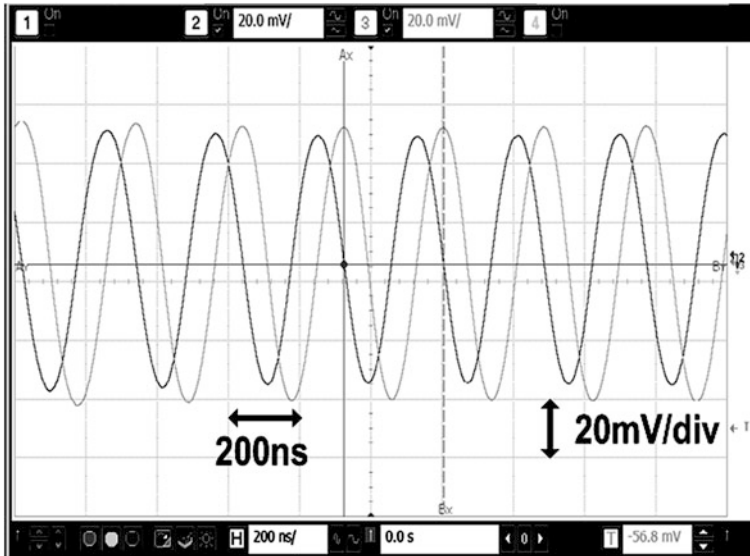


Fig. 2.22 Measured I/Q BB transient outputs

Table 2.2 Performance summary and benchmark with the state-of-the-art

Parameters	JSSC'08 [21]	JSSC'10 [22]	TCAS-I'10 [24]	TMTT'11 [23]	TMTT'11 [26]	TMTT'06 [27]	ISSCC'13 [5]	ISSCC'13 [25]	This work
Gain (dB)	35	67	24.5	51	22.5	30	83	55	32
DSB NF (dB)	7.5	16	16.5 (SSB)	3.2	7 (SSB)	7.3 (SSB)	6.1	9	8.8
Out-band IIP3 (dBm)	-10	-10.5	-19 (in-band data)	-32 (in-band data)	-21.5 (in-band data)	-8	-21.5	-6	-7
SFDR (dB)	58.3	52.3	38.3	36.5	51	59.8	51.6	60	59.4
VCO phase noise (dBc/Hz)	N/A	-127 @ 3 MHz	N/A	N/A	N/A	N/A	-112 @ 1 MHz	-115 @ 3.5 MHz	-111.4 @ 3.5 MHz
Power (mW)	5.4 (w/o VCO)	32.5 (w/VCO)	2.52 (w/o VCO)	8.1 (w/o VCO)	1.06 (w/o VCO)	1.8 (w/o VCO)	1.6 (w/VCO)	2.7 (w/VCO)	1.4 ^b (w/VCO)
No. of inductor or transformer	2	3	3	5	3	2	4	2	1
Die area (mm ²)	0.23 (w/o VCO)	2.88 (w/VCO)	N/A	1.27 (w/o VCO)	1.1 (w/o VCO)	2.07 ^a (w/o VCO)	2.5 ^a (w/VCO)	0.26 ^a (w/VCO)	0.14 (w/VCO)
Supply (V)	1.35	0.6	1.8	1.8	1.2	1.8	0.3	0.6/1.2	0.6/1.2
CMOS Tech.	90 nm	90 nm	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m	65 nm	65 nm	65 nm

^aInclude more BB gain stages and filters. ^bThe power breakdown is LNTA: 0.4 mW, TIA: 0.18 mW and VCO + Buffer: 0.82 mW

2.5 Conclusions

A mixed- V_{DD} 2.4-GHz ZigBee/WPAN receiver measuring state-of-the-art performances has been described. It features passive pre-gain, a split-LNTA, a high-input-impedance BB TIA and a low-power 50 % LO generation scheme. They together lead to improved power and area efficiencies, as well as a high SFDR while eliminating the need of a RF balun. These beneficial features render this work as a superior receiver candidate for cost and power reduction of ZigBee/WPAN radios in nanoscale CMOS.

References

1. P. Choi, H. Park, I. Nam et al., An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4GHz. *IEEE J. Solid-State Circ.* **38**, 2258–2268 (2003)
2. C.-H. Li, Y.-L. Liu, C.-N. Kuo, A 0.6-V 0.33-mW 5.5-GHz receiver front-end using resonator coupling technique. *IEEE Trans. Microw. Theory Tech.* **59**(6), 1629–1638 (2011)
3. B.W. Cook, A. Berny, A. Molnar et al., Low-power, 2.4-GHz transceiver with passive RX front-end and 400-mV supply. *IEEE J. Solid-State Circ.* **41**, 2767–2775 (2006)
4. A.C. Herberg, T.W. Brown, T.S. Fiez et al., A 250-mV, 352- μ W GPS receiver RF front-end in 130-nm CMOS. *IEEE J. Solid-State Circ.* **46**, 938–949 (2011)
5. F. Zhang, K. Wang, J. Koo et al., A 1.6mW 300 mV-Supply 2.4 GHz Receiver with -94dBm Sensitivity for Energy-Harvesting Applications, in *ISSCC Digital Technical Papers*, pp. 456–457, Feb 2013
6. A. Mirzaei, H. Darabi, J.C. Leete et al., Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers. *IEEE J. Solid-State Circ.* **44**, 2678–2688 (2009)
7. A. Mirzaei, H. Darabi, J.C. Leete et al., Analysis and optimization of direct-conversion receivers with 25 % duty-cycle current-driven passive mixers. *IEEE Trans. Circ. Syst. I, Reg. Papers* **57**, 2353–2366 (2010)
8. A. Balankutty, P.R. Kinget, An ultra-low voltage, low-noise, high linearity 900-MHz receiver with digitally calibrated in-band feed-forward interferer cancellation in 65-nm CMOS. *IEEE J. Solid-State Circ.* **46**, 2268–2283 (2011)
9. Y. Feng, G. Takemura, S. Kawaguchi et al., Digitally assisted IIP2 Calibration for CMOS direct-conversion receivers. *IEEE J. Solid-State Circ.* **46**, 2253–2267 (2011)
10. P.-I. Mak, R.P. Martins, A 0.46-mm² 4-dB NF unified receiver front-end for full-band mobile TV in 65-nm CMOS. *IEEE J. Solid-State Circ.* **46**, 1970–1984 (2011)
11. N. Poobuapheun, W.-H. Chen, Z. Boos et al., A 1.5-V 0.7-2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers. *IEEE J. Solid-State Circ.* **42**, 1669–1677 (2007)
12. C. Andrews, A.C. Molnar, A passive mixer-first receiver with digitally controlled and widely tunable RF interface. *IEEE J. Solid-State Circ.* **45**, 2696–2708 (2010)
13. C. Andrews, A.C. Molnar, Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers. *IEEE Trans. Circ. Syst. I, Reg. Papers* **57**, 3092–3103 (2010)
14. A. Molnar, C. Andrews, Impedance, Filtering and Noise in N-phase Passive CMOS Mixers, in *Proceedings of IEEE CICC*, pp. 1–8, Sept 2012

15. J. Kaykovuori, K. Stadius, J. Ryynanen, Analysis and design of passive polyphase filters. *IEEE Trans. Circ. Syst. I, Reg. Papers* **55**, 3023–3037 (2008)
16. F. Behbahani, Y. Kishigami, J. Leete et al., CMOS mixers and polyphase filters for large image rejection. *IEEE J. Solid-State Circ.* **36**, 873–887 (2001)
17. A. Liscidini, M. Tedeschi, R. Castello, Low-power quadrature receivers for ZigBee (IEEE 802.15.4) applications. *IEEE J. Solid-State Circ.* **45**, 1710–1719 (2010)
18. T.H. Lee, in *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd edn. (Cambridge University Press, Cambridge, 2004)
19. B. Razavi, *RF Microelectronics*, 2nd edn. (Prentice-Hall, Upper Saddle River, 2011)
20. W. Kluge, F. Poegel, H. Roller et al., A fully integrated 2.4-GHz IEEE 802.15.4-compliant transceiver for ZigBee TM applications. *IEEE J. Solid-State Circ.* **41**, 2767–2775 (2006)
21. M. Camus, B. Butaye, L. Garcia et al., A 5.4mW/0.07 mm² 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4 WPAN stand. *IEEE J. Solid-State Circ.* **43**, 1372–1383 (2008)
22. A. Balankutty, S. Yn, Y. Feng et al., A 0.6-V Zero-IF/Low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications. *IEEE J. Solid-State Circ.* **45**, 538–553 (2010)
23. J.-S. Syu, C. Meng, C.-L. Wang, 2.4-GHz low-noise direct-conversion receiver with deep N-well vertical-NPN BJT operating near cutoff frequency. *IEEE Trans. Microw. Theory Tech.* **45**, 538–553 (2010)
24. J. Kaykovuori, K. Stadius, J. Ryynanen, An energy-aware CMOS receiver front end for low-power 2.4-GHz applications. *IEEE Trans. Circ. Syst. I, Reg. Papers* **57**, 2675–2684 (2010)
25. Z. Lin, P.-I. Mak, R.P. Martins, A 1.7mW 0.22 mm² 2.4 GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65 nm CMOS, in *ISSCC Digital Technical Papers*, pp. 448–449, Feb 2013
26. J.L. Gonzalez, H. Solar, I. Adin et al., A 16-kV HBM RF ESD protection codesign for a 1-mW CMOS direct conversion receiver operating in the 2.4-GHz ISM band. *IEEE Trans. Microw. Theory Tech.* **59**, 2318–2330 (2011)
27. T.-K. Nguyen, V. Krizhanovskii, J. Lee et al., A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18 μ m CMOS technology. *IEEE Trans. Microw. Theory Tech.* **54**, 4062–4071 (2006)
28. Z. Lin, P.-I. Mak, R.P. Martins, A 0.14-mm², 1.4-mW, 59.4 dB-SFDR, 2.4-GHz ZigBee/WPAN receiver exploiting a “Split-LNTA + 50 % LO” topology in 65-nm CMOS. *IEEE Trans. Microw. Theory Tech.* **62**, 1525–1534 (2014)

Ultra-Low-Power and Ultra-Low-Cost Short-Range
Wireless Receivers in Nanoscale CMOS

Lin, Z.; Mak Elvis, P.-I.; Martins, R.P.

2016, XIV, 110 p. 72 illus., 52 illus. in color., Hardcover

ISBN: 978-3-319-21523-5