Chapter 2
The Future of Low-Power Electronics

Toshiaki Masuhara

Abstract The number of integrated transistors has increased so rapidly that it has become evident that a further increase of the performance is limited by the power dissipation. The future IT and electronics, therefore, require more efficient power-reduction solutions. In the human brain and nerve system, analog signals from sensing orgasms are processed by a network composed of neurons and synapses. This process is slow but very power-efficient because it is done by below-100 mV signal levels.

Although near-threshold or sub-threshold operation of digital CMOS circuits would be possible candidates for the future low-power electronics, the operating voltage was not scaled due to the fact that the sub-threshold characteristics of MOSFETs are not scalable. Various parameter variations of the MOSFETs also deteriorate the noise margin. Most of the existing non-volatile memories and switches have problems in operating at low voltages. It is evident that off-chip interface circuits, power delivery- and control-means, such as back-bias, and the protection devices against electrostatic discharge, also need to be integrated. If the power of the chip is greatly reduced, stacked-chip 3D integration could be an efficient solution in the future IT and electronics.

2.1 Electronics Systems and Power-Efficiency

It is expected by the JEITA Green IT Council that the power consumption of the ten major equipments (PCs, servers, storages, routers, displays, TVs, DVD-players, air-conditioners, refrigerators, and illuminations), and of the data centers increase

T. Masuhara (✉)
LEAP—Low-Power Electronics Association and Project, Niikura-bldg. 8F, 2-2, Kanda Tsukasa-machi, Chiyoda-ku, Tokyo 101-0048, Japan
e-mail: masuhara@leap.or.jp; toshi-masuhara@bridge.ocn.ne.jp

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rapidly as shown in Fig. 2.1a [1]. In the data centers, the electric power is expected to rise up to 2500 TWh/year in 2050 that is more than 17-times higher than that in 2005. This is due to the processing of big data and the rapid increase of the transactions of big data through the internet and data centers. The fraction of the electric power consumption by servers, storages, routers and switches are also shown in Fig. 2.1b [1]. It is evident that disruptive low-power technologies are needed in the future electronics and IT.

The evolution of the *computations/kWh* of computers is illustrated in Fig. 2.2. The data points for the *computations/kWh* were taken from the paper by Koomey et al. [2]. The vacuum-tube technology was replaced by the bipolar-transistor technology in the 1950s, then by bipolar or NMOS-IC technology in the 1960s. The bulk-CMOS, developed by Wanlass and Sah [3], had a feature that the stand-by power is zero due to the fact that either the pMOS or the nMOS transistor, forming a logic gate, is turned off in the digital circuit. However, since the bulk-CMOS is formed in a highly doped compensated well, the speed was not fast enough to be applied to high-end applications like NMOS. The application was limited to watches and calculators that allow slow speed. The development of the high-speed SRAM [4] in the late 1970s by the author's group was the first demonstration that bulk-CMOS can be applied to high-end integrated circuits. In the 1980s and 1990s, the use of bulk-CMOS has been expanded to most of the major integrated circuits, and it has been used for more than 30 years as the dominant technology. The rapid increase of the number of integrated transistors for more functions and performance, however, caused the rapid increase of the power dissipation. In the paper by Chen [5], it was pointed out that the module heat flux determines the limitation and causes the replacement of the dominant technology solution. He also pointed out

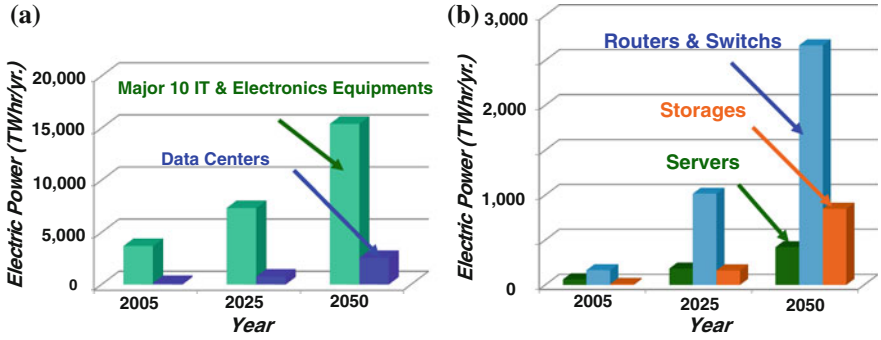


Fig. 2.1 Worldwide electric-power requirements for green IT technology estimated by JEITA (Japan Electronics and Information Technology Industries Association) Green IT Council 2013 [1]. **a** Electric-power requirement for major ten IT and electronics equipments (PCs, servers, storages, routers, displays, TVs, DVD players, air-conditioners, refrigerators and illuminations) and data centers. **b** Electric-power requirement for servers, storages, routers and switches

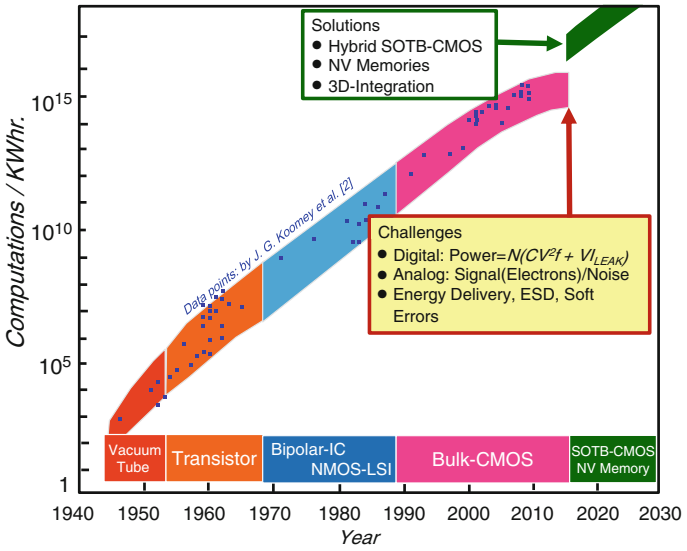


Fig. 2.2 Evolution of the computations/kWh and the major device technologies. Data points are taken from Koomey's paper [2]. Bulk CMOS needs to be exchanged by another technology solution by 2020 due to the power-dissipation limit (© 2009 IEEE)

that, around 2010, ultra-low-voltage and 3D technology would replace the conventional bulk-CMOS. Although many techniques to decrease the power have been developed so far, the saturation of the *computations/kWh* is expected in the future due to the heat-dissipation problem. It is, therefore, expected that the current bulk-CMOS will be replaced by another technology solution by the end of the decade due to the power-dissipation limit.

One of the most effective ways to reduce power in IT systems is the reduction of the power-supply voltage. This is because the power is determined by,

$$Power = N\left(CV^2 f + VI_{LEAK}\right).$$

The scaling of the device size and the supply voltage in the past worked when the MOSFET size was above 14 nm. Due to the leakage and sub-threshold slope of MOSFETs that are not scalable, the scaling below 14 nm has not been as efficient as it has been in the past. Challenges associated with the reduction of the power supply need to be solved at the same time. In digital circuits, they must be stable against parameter, voltage and temperature (*PVT*) variation. This means that enough margin needs to be ensured against noises, such as power-supply bounce, EMI noise, 1/*f* and the random telegraph noise of MOSFETs, and the soft errors due to

noise by high-energy particles. Secondly, to convert analog signals from the inputs to digital, enough signal-to-noise ratio is needed, which requires that analog circuits operate at a higher supply voltage than that of the digital part. Thirdly, integrated circuits must be operated with on-chip stable and controllable energy-delivery means, and they must be robust against electronic static discharge (ESD).

In the future society, wireless sensor networks (WSN) that utilize autonomous and maintenance-free sensors, will become essential parts of the society as illustrated in Fig. 2.3. The sensor network will be used in many applications including agriculture and food supply, medical services and health care, traffic control, monitoring of the social infra-structure, and ambient sensing such as river, weather, lands, and ocean. A technology solution for both low power and maintenance-free features are required. The sensors require not only digital processing of data, security and ID, but also wireless interfaces with extremely-low-power features. Either the energy harvesting, or perpetuum operation, in other words, the life-long operation with an installed battery becomes essential in such applications. Future mobile equipment, such as robots and smart mobility, also requires an energy-efficient and high *computations/watt* solution.

A project called, "*Ultra-Low Voltage Device Project for Low Carbon Society*", was performed in the *Low-Power Association and Project (LEAP)* since 2010–2015. The purpose of the project was to develop enabling technology solutions that reduce the power of the electronics and IT equipments by one order of magnitude against that of the existing ones by the below-0.4-V operation of the integrated

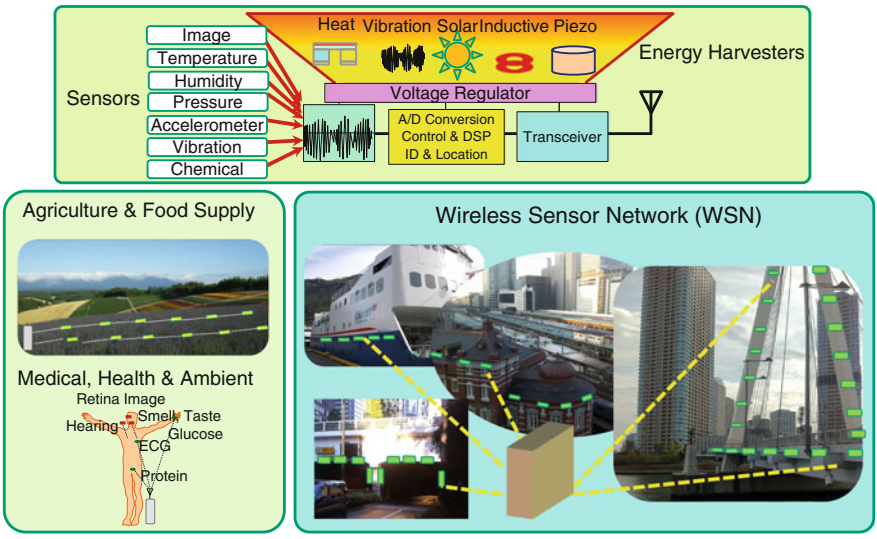


Fig. 2.3 Internet-of-things (IoT) paradigm requiring technology-solutions featuring low power, maintenance-free, and wireless access to internet (© LEAP)

circuits. In the project, three enabling technologies were developed. The first technology is the new CMOS operable at 0.4-V with much less standby current. The second solution is the nano-carbon interconnect for use in 3D flash memories such as BICS [6]. The third solution is the development of low-voltage non-volatile resistive memories. Three types of non-volatile memories and a switch were chosen. These include an embedded MRAM for cache application, a switch for post-fabricated logic configuration, and a new memory called TRAM for tier-0 storage. These were integrated in the backend process to avoid excessive thermal history.

2.2 Low-Power CMOS Technology

2.2.1 Hybrid SOTB CMOS Technology

The most effective way to reduce the power-supply voltage is to reduce the parameter variation of the MOSFETs. The SOTB (Silicon on Thin-buried-Oxide) MOSFETs, a variation of the fully-depleted (FD) SOI MOSFET with thin BOX (buried oxide) layer, was first developed by Tsuchiya et al. [7]. The SOTB-CMOS is a good candidate for low-voltage operation because of the low impurity concentration in the channel region resulting in small parameter variations. It also has a thin BOX layer to control the threshold voltage by applying a back-bias. In the *Ultra-Low Voltage Device Project*, a practical hybrid SOTB CMOS integrated circuit shown in Fig. 2.4, was developed and demonstrated. In the developed SOTB CMOS, the bulk-CMOS portion is fabricated by stripping off the BOX layer used for the SOTB-CMOS, where the SOTB-CMOS are optimized for low-voltage logic and SRAMs. The bulk-CMOS is used for I/O circuits, analog circuits such as A/D, D/A converters, ESD protection devices, and on-chip power converters where a higher voltage capability is required, and the legacy circuits.

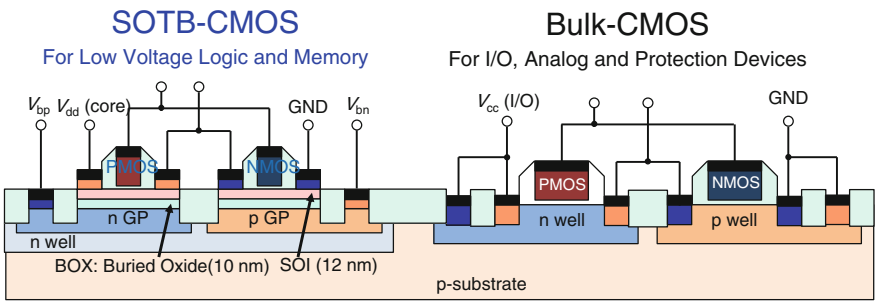


Fig. 2.4 Cross-section of the hybrid SOTB-CMOS. The SOTB-CMOS is optimized for low-voltage logic and SRAMs. The bulk-CMOS is used for I/O, analog, ESD protection and on-chip power converters, requiring higher voltage, and legacy circuits [8] (© 2014 IEEE)

An extensive study of the MOSFET parameter variation for bulk-CMOS was done for threshold-voltage V_{th}, and on-current I_{on}, in the MIRAI project as described in the NEDO project report [9]. The variation of V_{th} and I_{on} is originated by a non-uniform potential barrier in the channel region due to the random dopant fluctuation, and the variation of the gate work-function, the gate edge-roughness, the resistance of the source-drain extension, and the stress and the strain in the MOSFETs. It is proven that the random dopant fluctuation is the major origin of the variation. Figure 2.5 illustrates the simulated *DIBL* and V_{THC} variations for *2000* bulk and SOTB MOSFETs by Prof. Hiramoto, the Univ. Tokyo [10]. It is evident that the variation of the barrier-lowering due to random dopant fluctuations gives rise to the fluctuation of the channel potential, resulting in the variation of the *DIBL* and V_{THC}. It is also shown that both the variation of *DIBL* and V_{THC} is reduced in the FD-SOI as compared to those in the bulk-MOSFET. Better channel potential control by the gate-field in FD-SOI makes it possible to reduce the doping in the channel region, if the adjustment of the V_{TH} by the gate work-function is done properly.

I_d-V_g characteristics of the *high*-V_{th} (*HVT*), *medium*-V_{th} (*MVT*), and *low*-V_{th} (*LVT*) SOTB MOSFETs were optimized for 0.4 V operation as shown in Fig. 2.6 [11]. The threshold voltages are tuned by the Hf and Al in the gate so that the nMOS and pMOSFETs exhibit the symmetrical characteristics at zero gate voltage. The variation of the V_{th} for 1 M MOSFETs is shown in Fig. 2.7 [12]. It is demonstrated that the SOTB MOSFET has a smaller V_{th} variation, in other words, a smaller worst V_{th} value, that makes possible a lower-voltage operation. At the same time, the SOTB MOSFET realizes a smaller I_{ON} variation that results in a larger worst I_{ON}. This is an attractive feature in realizing higher performance at low supply voltages.

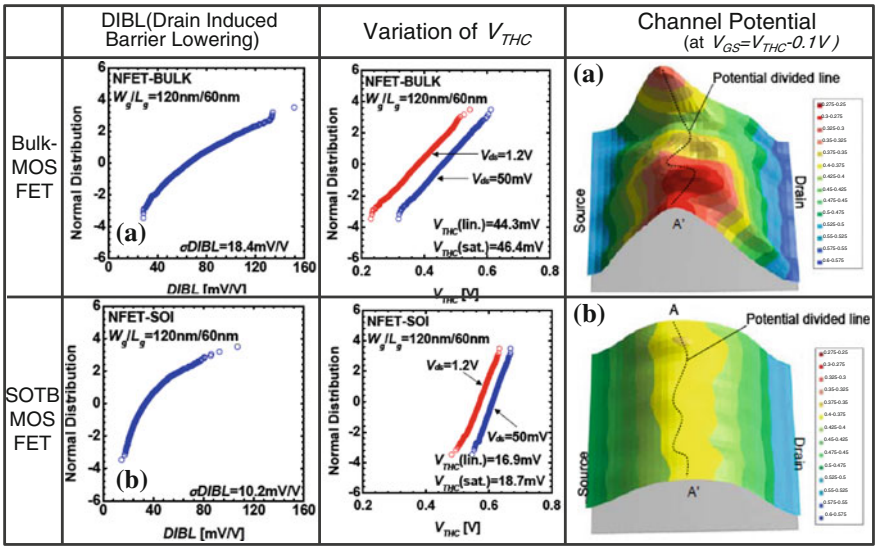


Fig. 2.5 Simulated *DIBL*, and V_{THC} variations for 2000 transistors in the bulk and SOTB MOSFETs. The potential diagrams in the channel are shown to the right by different colors corresponding to 0.025-volt scale [10] (© 2010 IEEE)

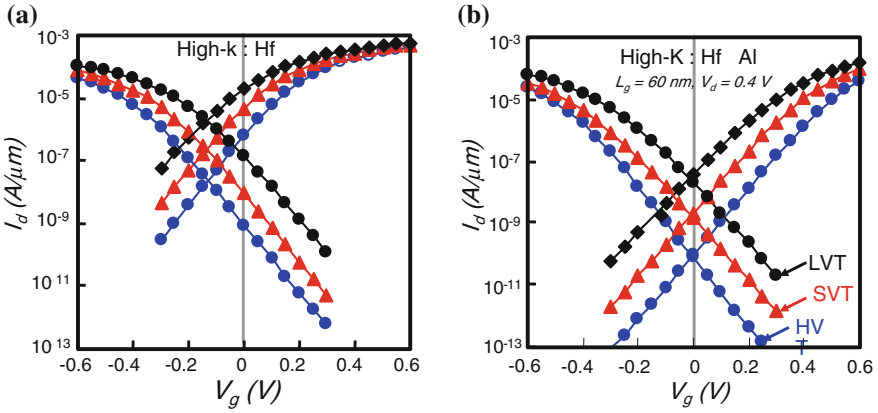


Fig. 2.6 I_d-V_g characteristics of SOTB nMOS and pMOSFETs optimized for 0.4 V operation. The threshold-voltages are tuned by the Hf and Al so that nMOS and pMOSFETs exhibit the symmetrical characteristics at zero-gate voltage [11] (© IEEE). **a** I_d-V_g characteristics with Hf in the gate-material. **b** I_d-V_g characteristics for LVT, SVT, and HVT MOSFETs with Hf and Al in the gate-material

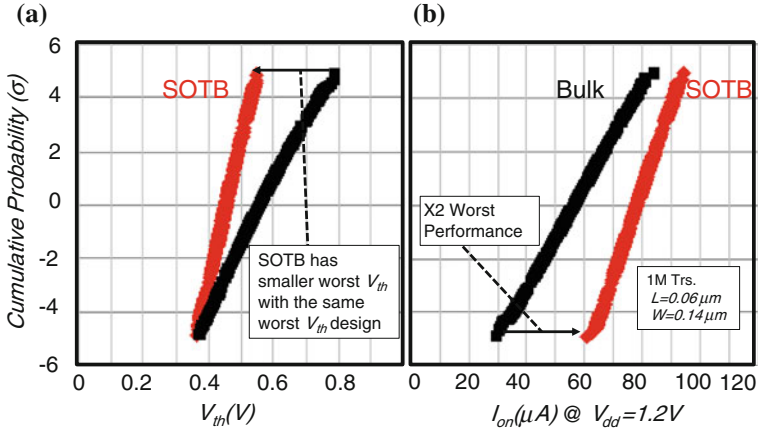


Fig. 2.7 Comparison of the variation (cumulative probability) of the V_{th} and I_{on} for 1 M SOTB and bulk nMOSFETs [12] (© IEEE). **a** Cumulative probability of the V_{th} of 1 M SOTB and bulk nMOSFETs. **b** Cumulative probability of the I_{ON} of 1 M SOTB and bulk nMOSFETs

2.2.2 *Low-Voltage SRAM*

The low-voltage SRAM was developed using 65 nm SOTB CMOS technology. Figure 2.8 illustrates (a) the cross-section of the SOTB transistor, (b) the SEM photo of the SRAM memory cell, (c) access-time versus supply-voltage V_{dd}, (d) fail-bit distribution versus V_{dd}, and (e) active/standby power of the SRAM when

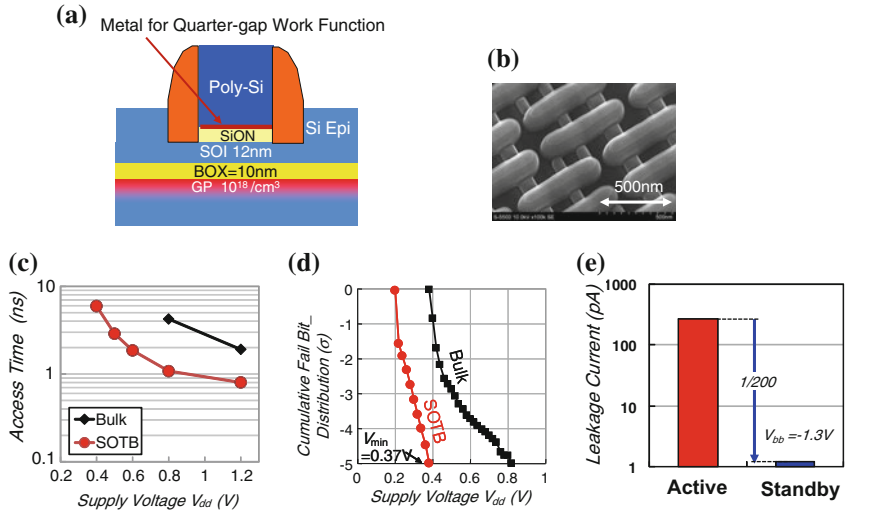


Fig. 2.8 2 Mb, 65 nm SOTB-CMOS SRAM operated at 0.37 V [12] (© 2013 IEEE). **a** Cross-section of the SOTB transistor. **b** SEM Photo of the SRAM cell. **c** Access time of the SRAM. **d** Fail-bit of the SRAM as a function of V_{dd}. **e** Leakage-current of the SRAM cells

a back-bias voltage of −1.3 V is applied [12]. Although several SRAM circuit techniques were developed to operate the SRAM at low voltage, this demonstration was simply done by using the conventional 6-transistor SRAM cell without any voltage-boosting techniques for the word- and bit-lines to compare the technologies. It can be seen that the developed SOTB-CMOS SRAM operates at an access-time of 5.5 ns at 0.4 V, whereas the bulk-CMOS using the same design cannot be operated below 0.8 V. This indicates that the SRAM does not need ECC (error-correction-code) to rescue fail-bits, whereas the tail-portion of the fail-bits in the bulk-CMOS SRAM are usually rescued by the ECC circuits to increase the yield in low-voltage operation. It is also seen in Fig. 2.8e, that the leakage-current in the standby-mode could be efficiently reduced by more than 2 orders by applying a V_{bb} = −1.3 V as compared to the leakage in the active mode. This indicates the effectiveness of the threshold-voltage control in SOTB-CMOS.

2.2.3 *Low-Voltage Microprocessor and Logic Circuits*

A low-voltage microprocessor with 144 KB SRAM was developed using 65 nm SOTB CMOS technology [8]. The photomicrograph of the fabricated chip and the simple block-diagram is shown in Fig. 2.9. Since a bulk-CMOS microprocessor can be integrated on the same chip, a comparison of the performance and of the energy for both designs was done as shown in Fig. 2.10. It is exhibited that the SOTB-CMOS microprocessor could be operated at 0.22 V with a clock frequency

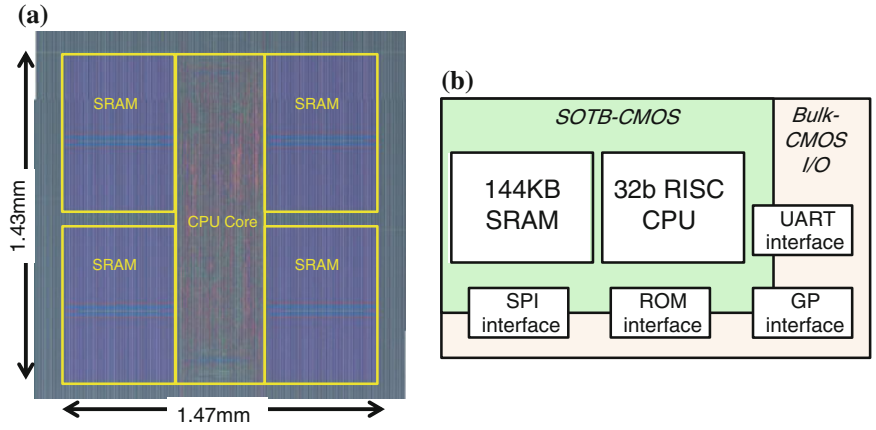


Fig. 2.9 SOTB-CMOS microprocessor with 144 KB SRAM that operates at less than 0.5 V [8] (© 2014 IEEE). **a** Photomicrograph of the chip. **b** Simplified block-diagram of the 32 b-RISC microprocessor

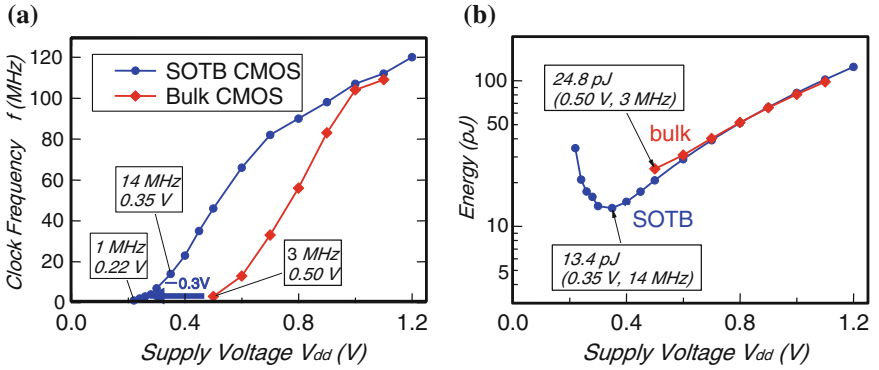


Fig. 2.10 Performance of the SOTB-CMOS and the bulk-CMOS microprocessor [8] (© 2014 IEEE). **a** Clock-frequency as a function of the supply-voltage. **b** Energy (pJ) as a function of the supply-voltage

of 1 MHz whereas the minimum operating voltage of the bulk-CMOS is 0.5 V. It is also seen from (b), that 14 MHz operation was performed at the minimum energy of 13.4 pJ at $V_{dd} = 0.35$ V in SOTB-CMOS. The sleep-current of the microprocessor at 0.35 V is shown in Fig. 2.11 (a) as a function of the supply-voltage V_{dd}, and (b) as a function of the CPU temperature, indicating that the back-bias contributes to effectively reduce the sleep-current by more than two orders-of-magnitude. The comparison of the leakage-current in the bulk and the SOTB nMOSFET is shown in Fig. 2.12. In the bulk nMOSFETs, the substrate-leakage becomes the dominant portion of the total leakage-currents when negative back-bias is applied, and hence, the leakage cannot be reduced below 1/10 of that at zero back-bias. In the

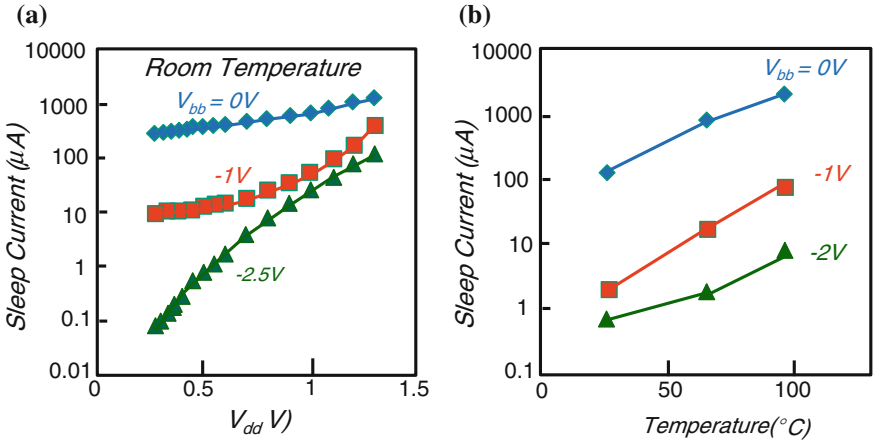


Fig. 2.11 Sleep-current of the SOTB-CMOS microprocessor [8] (© 2014 IEEE). **a** Sleep-current of the CPU as a function of the supply-voltage V_{dd}. **b** Sleep-current of the CPU as a function of the temperature

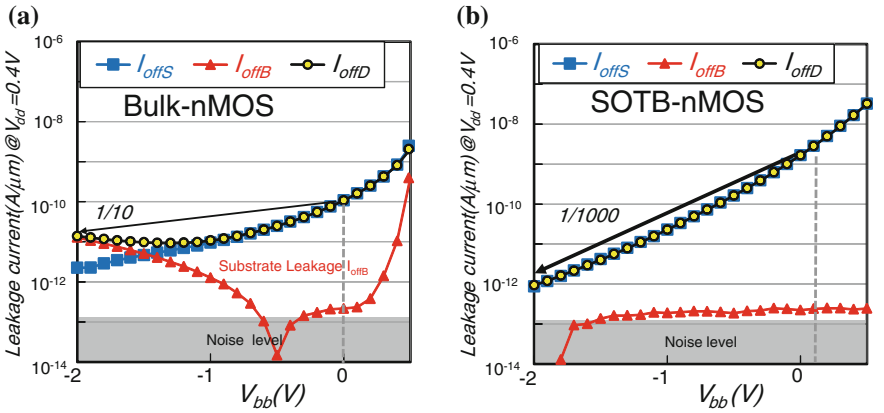


Fig. 2.12 Comparison of the leakage-currents in the bulk- and the SOTB-nMOSFET [12] (© 2013 IEEE). **a** Leakage-currents in the bulk-nMOSFET as a function of back-bias V_{bb}. Substrate leakage increases when a large back-bias is applied. **b** Leakage-currents in the SOTB-nMOSFET as a function of back-bias V_{bb}. Substrate leakage does not increase when a large back-bias is applied

SOTB MOSFET, the leakage-path does not exist because the substrate is insulated by the buried-oxide (BOX) layer. This makes possible a reduction of the leakage-current to 1/1000 of that for zero back-bias voltage as seen in Fig. 2.12b. Effective control of the threshold-voltage by back-bias makes possible to minimize the leakage-current at elevated temperatures, avoiding the abnormal operation at an elevated temperature. It also can compensate for the threshold-voltage increase at low-temperature operation. Such wide controllability by the back-bias makes possible an operation of the processor in a much wider temperature range.

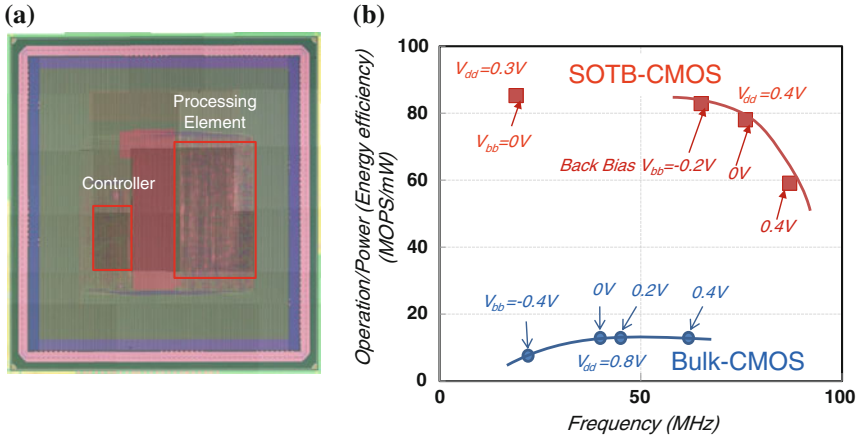


Fig. 2.13 Performance of the SOTB-CMOS accelerator CMA (cool mega array) designed by Keio Univ. (© IEICE). **a** Photomicrograph of the cool-image-array chip designed by using SOTB-CMOS. **b** Energy-efficiency (operation/power) by alpha-blender benchmark versus frequency as a function of supply-voltage and back-bias voltage

To demonstrate the performance of a logic circuit, an SOTB-CMOS Cool-Mega-Array (CMA) consisting of a controller and processing-element was developed by Prof. Amano's group, Keio Univ. [13]. The photomicrograph of the chip is shown in Fig. 2.13a. The comparison of the performance/power (efficiency) of the SOTB-CMOS CMA and the bulk-CMOS CMA was done by using the alpha-blender benchmark. The result is shown in Fig. 2.13b. The comparison shows that the SOTB-CMOS CMA can be operated at V_{dd} = 0.3–0.4 V as compared to 0.8 V in the bulk-CMOS, and it exhibits an energy-efficiency 5-times-higher than that of the bulk-CMOS CMA. This indicates that the low-voltage operation is effective to get higher MOPS/mW in digital signal- or image-processing applications. It has been pointed out that a dedicated-processor solution provides 1000-times higher performance compared to the microprocessor solution. This is due to the CPU-memory bottleneck [14]. This suggests that the combination of the low-voltage CPU and a dedicated-processing element such as CMA or off-loader enables much better performance/power solutions.

2.3 Low-Power Non-volatile Memories and Switches

In present-day electronics and IT equipment, many types of memories are used in each hierarchy. Program-execution is done in the processors with embedded memories, using data from an off-chip DRAM main memory or working buffer. Embedded memories include SRAM/DRAM L1 to L3 cache memories, ROMs or non-volatile PROM for firmware. In storage, HDD has been used as the dominant

device. Solid-State Disk (SSD) using NAND-type flash memories are now replacing HDD in the tier 0, 1 class storage device.

In memory-cell circuits, such as DRAM, SRAM, or Flash memories, electronic charge, the product of *CV*, where *C* is the capacity of the memory-node and *V* is the memory voltage, is used as means to store "1's" and "0's". When the capacity *C* or the voltage *V* becomes small, the memory-signal becomes small. As a result, marginal sensing of the small signal becomes a problem. Since these memory-cells are volatile, they lose memory information when the supply-voltage is turned *OFF*. It is, therefore, necessary to keep the power-supply *ON,* or re-load the memory data, when the memory turns *ON* again. In the *ON* condition, the memory-cell leakage due to the sub-threshold current needs to be either compensated for or refreshed to keep the memory charge in the cell as illustrated in Fig. 2.14a. In the non-volatile resistive-change memory cells, illustrated in Fig. 2.14b, once "high" and "low" resistivity-values are written into the memory material, the memory information can be sustained, even if the power-supply is turned *OFF*. The read-operation is done by sensing the current in the memory resistor. The sensing at low voltage, however, requires enough signal-to-noise ratio (S/N) as illustrated. Various resistive-change memories such as MRAMs, ReRAMs, and PCMs, are now in development. In this section, three types of resistive-change memories and switches are described, that have been developed by LEAP for low-voltage operation.

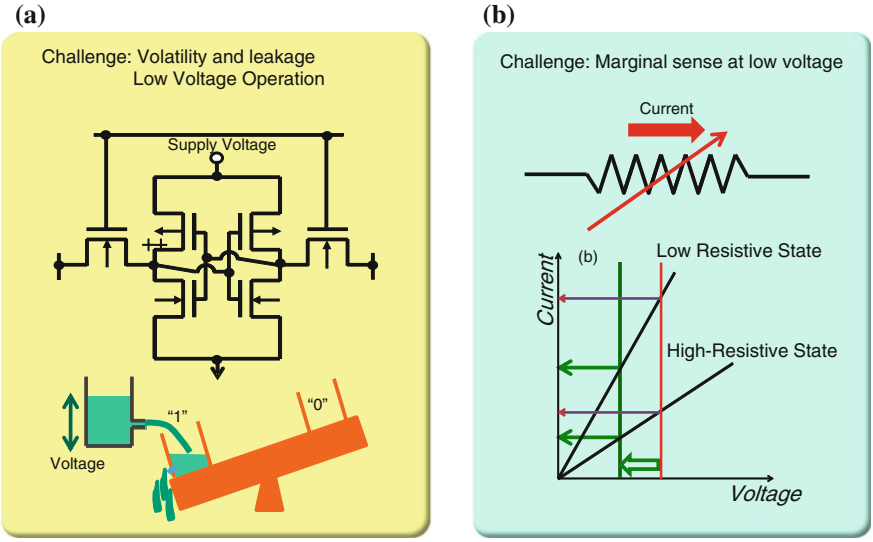


Fig. 2.14 Challenges of the low-voltage memories. In low-voltage operation, the non-volatile resistive memory cell has an advantage over the volatile voltage memory-cell due to leakage compensation and volatility (© LEAP). **a** Voltage memory cell (SRAM or 1T-DRAM). **b** Non-volatile resistive-change-type cell

2.3.1 MRAM for Cache Applications

Figure 2.15 illustrates an MTJ used in STT-MRAM for low-voltage and low-power cache applications developed by LEAP [15]. An essential part of the MRAM consists of a tunnel-insulator sandwiched by pinned and free-ferromagnetic layer. Writing "1's" and "0's" is done by the current-flow through the tunnel-insulator and by changing the spin-direction of the free layer. Since enough current-density is required to change the spin direction, a small MTJ is advantageous to realize a low-power MRAM. If the free layer and the pinned layer have the same spin-direction, that state corresponds to the low-resistivity state. On the contrary, if the spin-directions are opposite, the current through the MTJ becomes lower, and that corresponds to the high-resistivity state. The current-ratio depends on the ferromagnetic material of the MTJ tunnel-insulator, and their quality. For marginal operation, the current-ratio of at least over 100 %, including variation, is desirable.

MRAM is supposed to be suitable for the non-volatile data-memory for mobile applications. This does not require a fast switching-speed, but low-voltage and

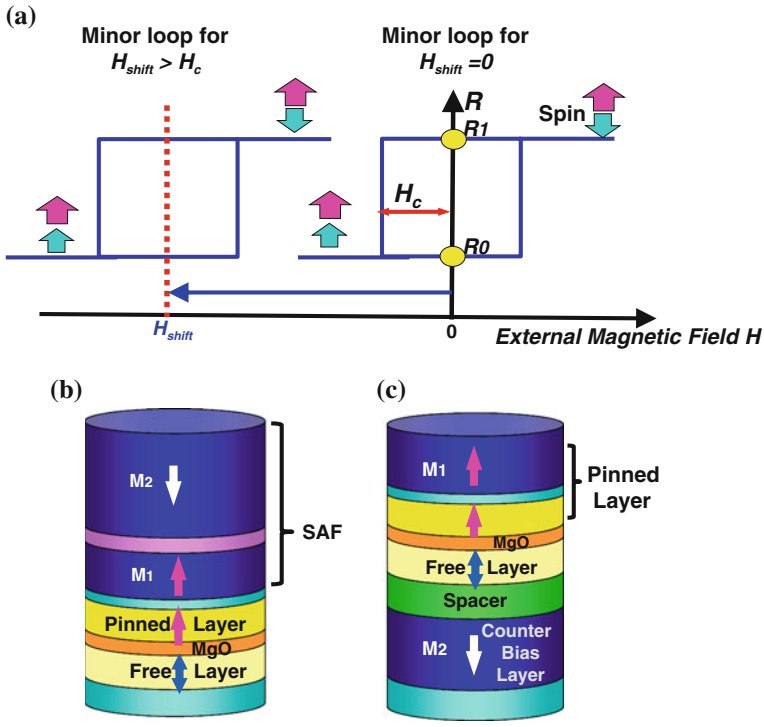


Fig. 2.15 Schematic diagram of the perpendicular magnetic tunnel-junction (MTJ) for suppressing stray-field [15] (© 2013 IEEE). **a** Illustration of the induced minor loop shift in MTJ. **b** Conventional synthetic anti-ferromagnetic (SAF) pinned layer (SP) type MTJ. **c** Counter-bias magnetic field layer (CBF) type MTJ

low-power characteristics are required. Another application of the MRAM is the embedded non-volatile cache-RAM that replaces the currently dominant SRAM or the DRAM cache. This application requires a smaller cell-area compared to that of other cache-memories, and over 10^{15} (infinite) write-erase cycles.

A Counter-Bias magnetic Field layer (CBF) type MTJ shown in Fig. 2.15 was developed for low-power cache applications [15]. In MRAM, the stray magnetic field from the pinned layer causes a shift of the minor loop H_{shift}. It is required that H_{shift} be kept as small as possible so that the symmetrical resistance-change occurs for a positive and negative external magnetic field H as shown in Fig. 2.15a. The stray magnetic field from the pinned layer, therefore, needs to be compensated for by adding an additional layer. Conventional MTJ shown in Fig. 2.15b has Synthetic Anti-Ferromagnetic (SAF) Pinned layer (SP) for this purpose. When the memory cell size is reduced for cache applications, the compensation margin of the SAF type cell may not be enough, and that makes it difficult to assure marginal operation. A Counter-Bias magnetic Field layer (CBF)-type MTJ, shown in Fig. 2.15c, exhibits a larger margin due to the fact that the counter-bias layer and spacer thicknesses could be independently optimized. The CBF MTJ cell, fabricated in the 65 nm CMOS back-end process is shown in Fig. 2.16a. The measured H_c and H_{shift} versus MTJ size in CBF structure cell for suppressing stray field indicates that the measured H_{shift} is maintained below H_c for the cell-size diameter of less than 50 nm. This shows that marginal operation is possible. To achieve read- and write-cycles of over 10^{15}, it is essential to form an MgO layer having good crystal-quality. It was verified that MgO tunnel-oxide with good crystal-quality is formed by inserting a CoFe seed layer on the CoFeB layer and oxidizing Mg deposited on CoFeB [16]. An accelerated experiment of TDDB test indicated that a write-erase cycle of over 10^{16} at 0.65 V was achieved.

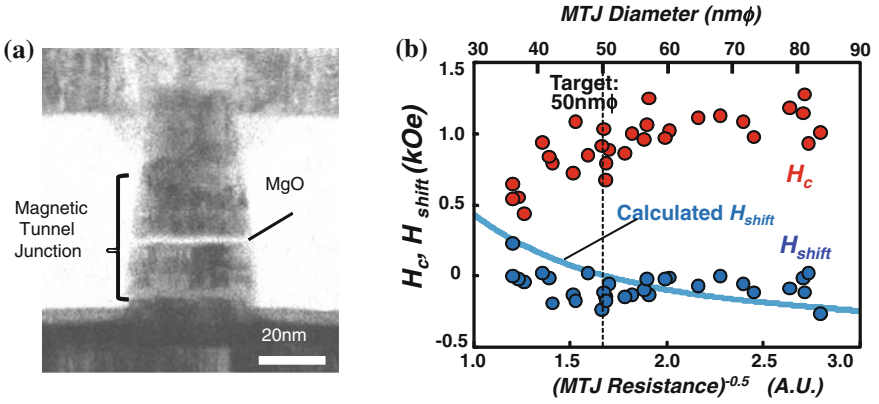


Fig. 2.16 Fabricated MTJ cell in the back-end process and the result of the stray-field suppression [15] (© 2013 IEEE). **a** Cross-sectional TEM photo of the MRAM cells. **b** Measured H_c and H_{shift} versus MTJ size in CBF structure cell for suppressing stray-field

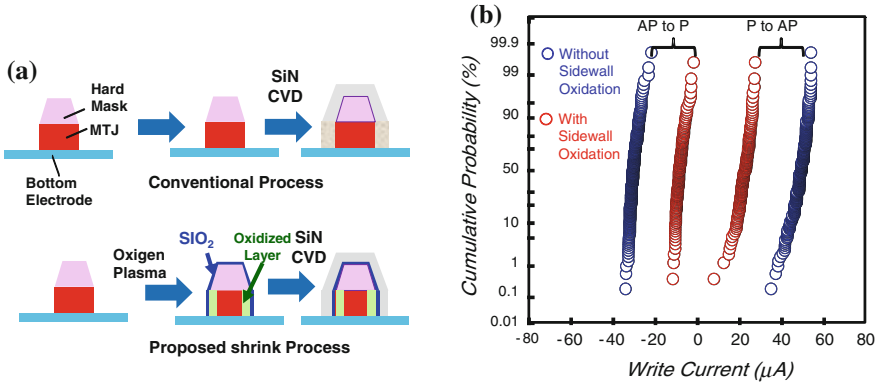


Fig. 2.17 MTJ cell-shrink process using sidewall oxidation, and write-current distribution [17] (© 2014 IEEE). STT-MRAM enables memory cell-size of $25F^2$ as compared the $150F^2$ SRAM cell where F is the feature size. **a** Sidewall oxidation MTJ cell shrink process. **b** Write-current distribution of the MTJ cell with sidewall oxidation (*red*) and without sidewall oxidation (*blue*)

To reduce the write-current, the MTJ size needs to be minimized. The challenge is to control the variation of the write-current with such a small cell-size. Figure 2.17a illustrates a new cell-size shrink process developed [17]. A sidewall-oxidation technique makes it possible to remove the periphery of the MTJ to reduce the cell-diameter. The write-current of as low as 20 μA was obtained without degrading the variation of the write-current as shown in Fig. 2.17b. Reduction of the write-current, and control of the variation would make possible the MRAM as a promising candidate for non-volatile cache memories in microprocessors applied to electronics and IT equipment.

2.3.2 *Complementary Atom-Switch for Programmable Logic After Fabrication*

In many data-processing applications, dedicated application-specific ICs (ASICs) have performance advantages over microprocessors. However, due to the rapid increase of the cost and lead (turnaround) time for design, mask, and manufacture of ASICs, the FPGA approach has become desirable in many applications. The FPGA approach is using SRAM cells and switches to configure the logic. Therefore, the SRAM area occupies a large fraction of the switch area, and a non-volatile configuration-data memory is required.

An atom-switch is a non-volatile resistive-change switch for use in programming the logic in the integrated circuits after fabrication. It utilizes the formation and annihilation of a metal-bridge in a polymer-solid-electrolyte (PSE). A schematic illustration of the atom-switch is shown in Fig. 2.18. The switch is called complementary atom-switch (CAS) [18]. As shown in Fig. 2.18a, the switch turns *ON*

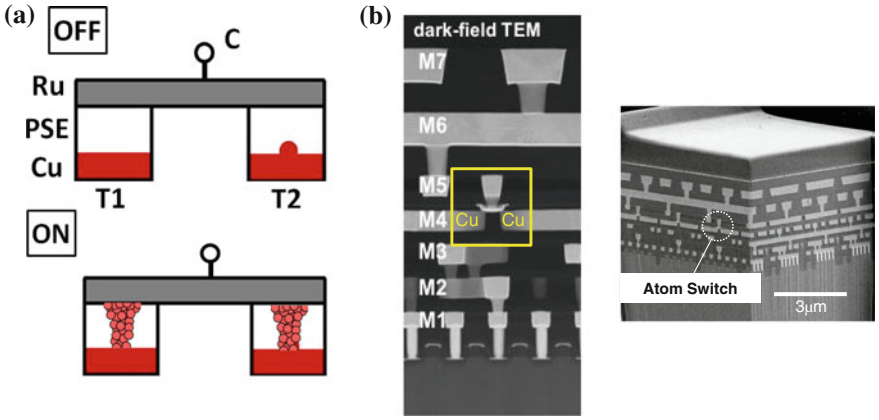


Fig. 2.18 Complementary atom-switch (CAS), a non-volatile switch device for programming after fabrication [18] (© 2012 IEEE). **a** Complementary atom-switch (CAS). **b** Cross-section of the CAS

(set), when a positive bias is applied to the Cu electrode, and it turns *OFF* (reset), when a positive voltage is applied to the Ru electrodes. The bridge is formed by the movement of the Cu ions through a polymer solid electrolyte (PSE). The CAS is formed between M4 and M5 metal layers as shown in the cross-sectional photos in Fig. 2.18b. Figure 2.19 (a) illustrates the current I_{T1C} and I_{T2C} in the set (*OFF* to *ON*)-operation, (b) I_{T1C} and I_{T2C} in the reset (*ON* to *OFF*)-operation, and (c) the ratio of I_{T1T2} (*ON*) and I_{T1T2} (*OFF*) [19]. In the set-mode, the current rapidly

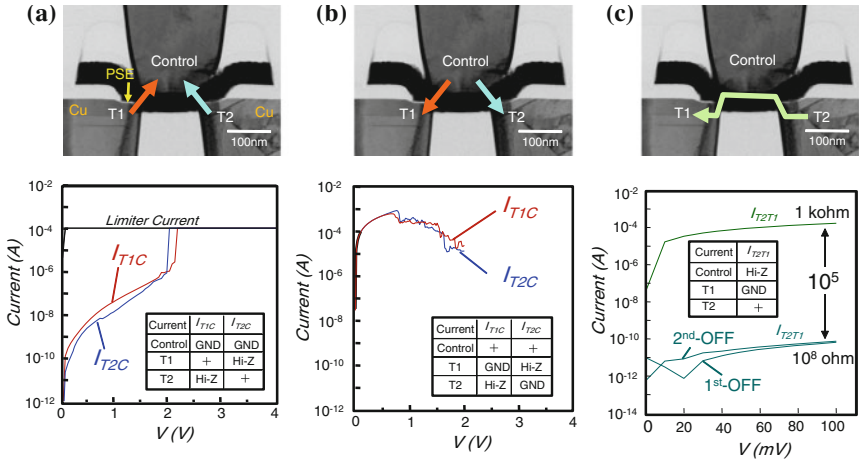


Fig. 2.19 Current versus voltage of the CAS and the ratio of the ON/OFF current I_{T1T2} of the CAS [19] (© 2011 IEEE). **a** I_{T1C} and I_{T2C} in the set (OFF to ON) mode. **b** I_{T1C} and I_{T2C} in the reset (ON to OFF) mode. **c** Ratio of the ON/OFF current of the CAS I_{T1T2}

increases at around 2 V, that is the voltage of the bridge-formation, and in the reset-operation, the current decreases logarithmically around 1–2 V. In the reading operation, the ratio of the current from T2 to T1, I_{T1T2}, is maintained to around 10^5. This makes possible a stable read-operation at a low voltage.

For programming the logic, the cell-architecture shown in Fig. 2.20 was developed [18]. The logic block consisting of 2 × 4-input LUT is programmed by the 386 CAS devices (304 for routing, 64 for LUT, and 18 for condition). The switch-block is laid out above the logic-block as illustrated in the schematic layout shown in (b). Table 2.1 illustrates a comparison of the FPGA, using a SRAM cell and a switch-transistor, and the programmable logic using CAS. The first advantage of the CAS reconfiguration over FPGA is the non-volatility. The second is the small area of the CAS compared to the SRAM cell. The three dimensional feature of the CAS layout also results in a significant area-reduction and corresponding speed and power advantage due to the reduced interconnect resistance and capacitance. Table 2.2 shows a comparison of the ASIC, FPGA, and CAS approaches in configuring logic. Although the ASIC approach has been used for many years, it suffers from design and manufacturing cost and lead-time, particularly in scaled technologies. The FPGA solution has exchanged the ASIC approach due to the zero design-cost and zero lead-time, although it has performance and chip-area penalties.

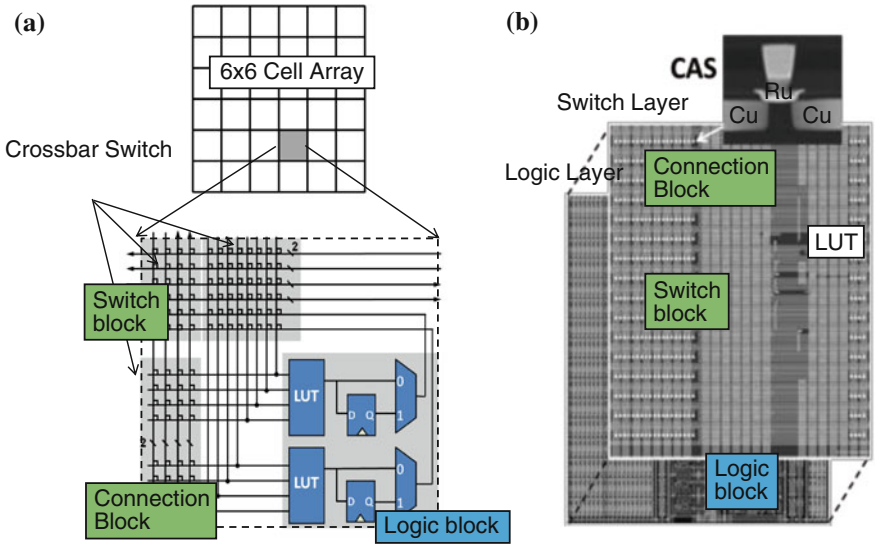


Fig. 2.20 Cell architecture of the programmable logic using CAS [18] (© 2012 IEEE). **a** Cell with 2 × 4-input LUT with 386 CAS (304 for routing, 64 for LUT, and 18 for condition) for 6 by 6 programmable logic cell (*top*). **b** Conceptual 3D-layout of the logic-cell

Table 2.1 Comparison of the FPGA and CAS programmable logic (© LEAP)

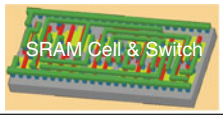
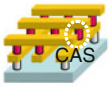
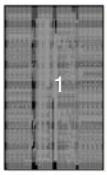
		Conventional FPGA	Programmable Logic Using CAS
Switches	Schematic Figure		
	Area Resistance Capacitance Volatility	1 1 1 Volatile	0.05 0.1 0.1 Non-Volatile
Program-mable Logic	Layout & Area		  3D Layout

Table 2.2 Comparison of the ASIC, FPGA, and programmable logic using CAS (© LEAP)

LSI	ASIC	FPGA	CAS
Power efficiency	10 or more	1	10
Chip area	1/10	1	1/4
Design cost for LSI	High (M$)	0	0
Design turnaround	Months	0	0

Compared to these, the CAS approach could provide cost and power advantages as well as the design and manufacture lead-time advantage.

Since the established Cu bridge in the PSE is very thin, the reliability might be a big concern. To achieve high reliability, the choices and the design of the electrode and PSE material, programming- and erasing-method are essential. The results of the reliability evaluation of the CAS are shown in Fig. 2.21 [19–21]. It illustrates that the proposed CAS switch has proven to be able to provide reliable non-volatile switches for post-fabricated logic programming.

The performance comparison was done between the fabricated programmed logic circuits using SRAM and that programmed by CAS. The comparison was done by using 65 nm bulk-CMOS technology and the 6 × 6 programmable logic-cell arrays. The cell shown in Fig. 2.20 is used. The delay-time and the active power were compared for three configured logics, as illustrated in Fig. 2.22. In 4b multiplexer, the delay and active power advantage of over 60 % is obtained in the CAS configuration over the SRAM configuration [22].

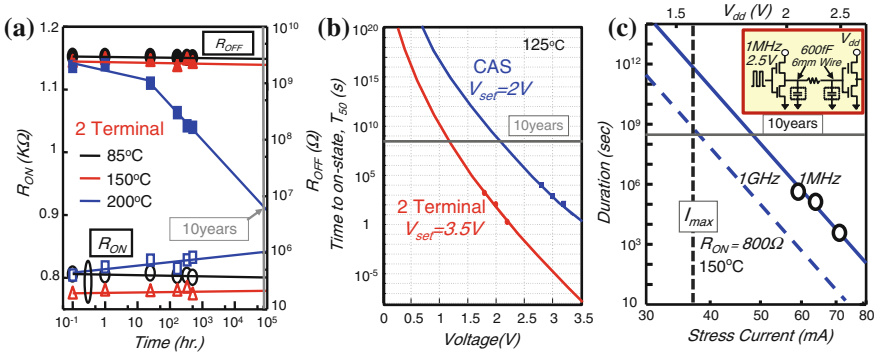


Fig. 2.21 Reliability of the programmed logic using CAS atom-switches [19–21] (© 2012 IEEE). **a** ON/OFF retention of 2-terminal atom-switch at 150 °C, 10 years. **b** OFF retention of CAS and 2-Terminal atom-switch at 125 °C, 10 years. **c** AC ON reliability when I = 37 μA, 1 GHz is applied at 150 °C, 10 years

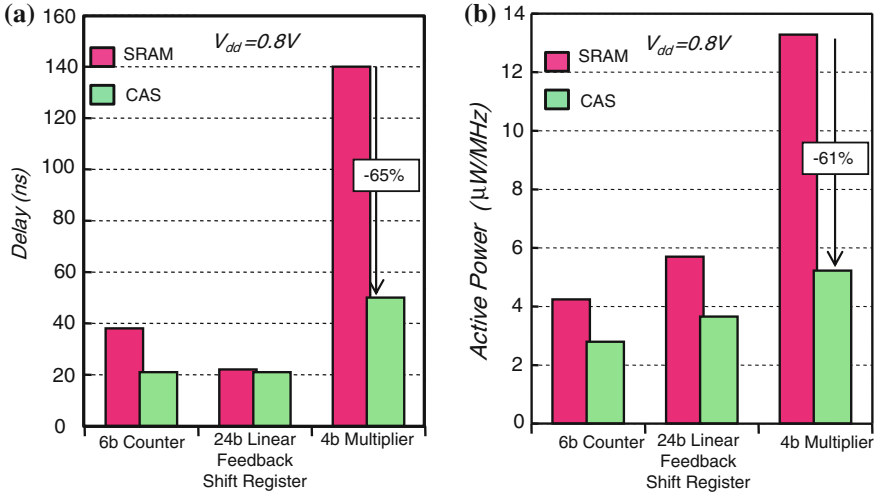


Fig. 2.22 Comparison of the delay and power in conventional FPGA using SRAM and the programmable logic using CAS [22] (© LEAP). **a** Comparison of the delay-time. **b** Comparison of the active power

2.3.3 SOTB-CMOS Microprocessor with Atom-Switch PROM

The atom-switch can be applied to PROM in a microprocessor as a low-voltage firmware memory [23, 24]. A 32 b-RISC chip was developed that utilizes a low-voltage SOTB-CMOS microprocessor and atom-switch PROM as shown in Fig. 2.23a. The microprocessor is the 5-stage pipelined 32 b RISC CPU with 2

blocks of 32 KB SRAM data memory, and 16 KB atom-switch PROM. Since the microprocessor is targeted to operate below 0.5 V, and since it is necessary to apply a relatively high voltage for programming, two series-memory-transistors are used to avoid the breakdown of the PROM-array transistors. The array is also separated by separation transistor during PROM programming. For low voltage read-operation, the PROM circuit, shown in Fig. 2.23b, and the atom-switch PROM-cell, shown in Fig. 2.23c, were designed. At such low voltages, a standard differential sense-amplifier is hard to operate stably. Therefore, a simple

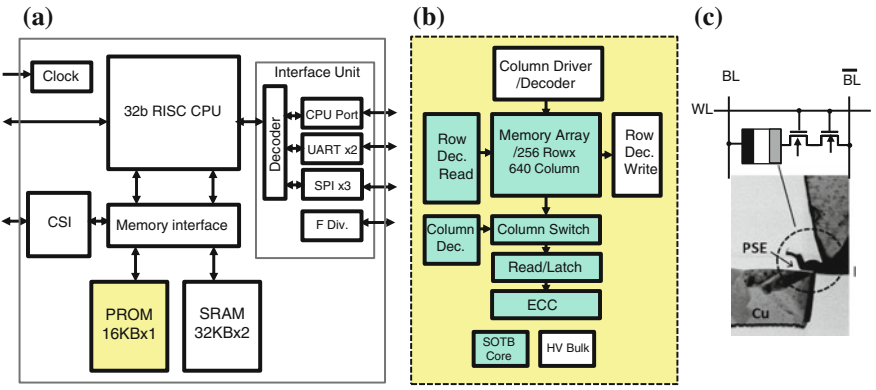


Fig. 2.23 32 b RISC CPU using SOTB-CMOS and PROM using atom-switch cells [23, 24] (© Appl. Phys.). **a** Block diagram of the 32 b RISC. **b** Block-diagram of the PROM. **c** Atom-switch PROM cell

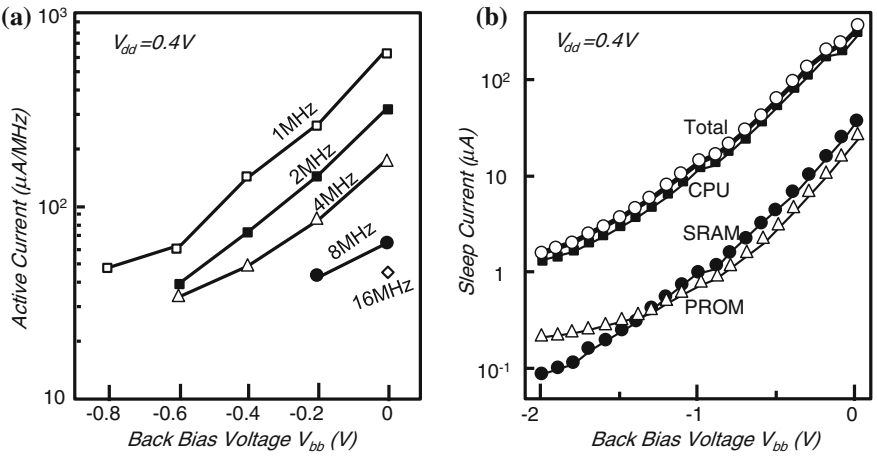


Fig. 2.24 Active current and the sleep-current of the 32 b RISC CPU using SOTB-CMOS and atom-switch PROM [23, 24] (© 2015 IEEE). **a** Active current of 32 b RISC CPU as a function of $V_{BB}(V)$. **b** Sleep-current of 32 b RISC as a function of $V_{BB}(V)$

inverter-type sense-amplifier is employed. The sensing is done by pre-charging the sensing node first, and then, the signal is read by opening the separation-transistor and column-switch. The active current and the sleep current are shown in Fig. 2.24a, b. It is seen that the microprocessor operates with 50 μA/MHz at 0.4 V with less than 2 μA standby current with a back-bias of −2 V. This indicates that the microprocessor can load application-specific firmware after fabrication, and the microprocessor can operate at 0.4 V with very low standby current.

2.3.4 TRAM for Low-Power Storage

In a "big data" era, data-access with high speed and less power has the key importance in the storage systems as shown in Fig. 2.25. In a data center, IT equipment including servers and storage consume 1/3 of the power. The other portion of the power is consumed by the power delivery, UPS and the cooling system. The power of these is correlated to the power of the IT equipment. In a current storage-system hierarchy, SSD has already been used in tier-0 and 1. HDD is dominant in tier 2 and 3. In the future storage systems, SSD would replace the tier 2 and 3, but for tier 0, highly efficient next-generation storage-level memory is needed. This new-generation storage should have a more than 10-times higher data rate and much lower power dissipation as shown in Fig. 2.25c.

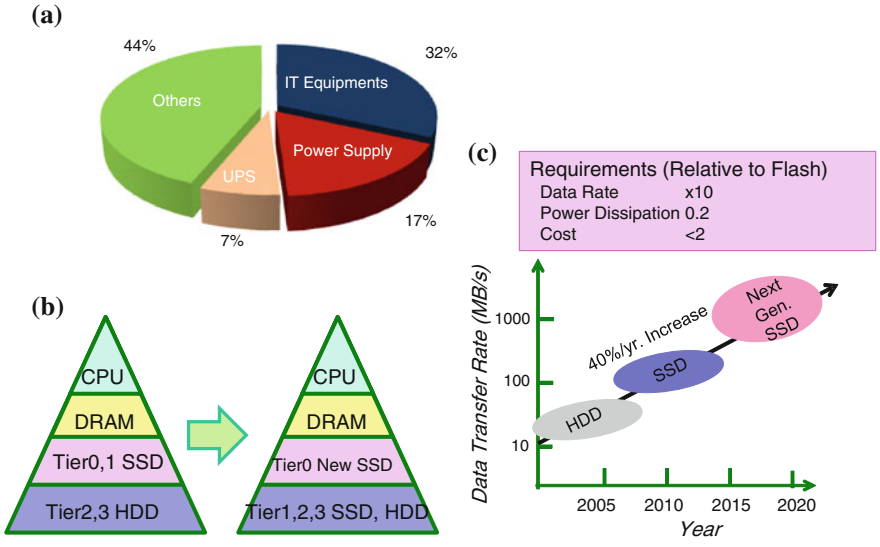
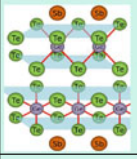
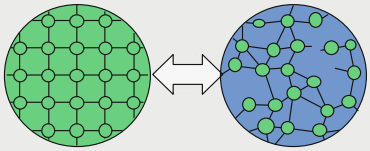


Fig. 2.25 Requirements for the storage-class memory in the era of "big-data" (© LEAP). **a** Power-dissipation in a data center. **b** Shift of hierarchy in storage systems. **c** Requirement for the future storage-class memory

Table 2.3 Comparison of the TRAM (topological switching RAM) and PRAM (© LEAP)

Memory	TRAM Topological-switching RAM	Conventional PRAM Phase Change Memory
Material	$GeTe/Sb_2Te_3$ Super-lattice	$Ge_2Sb_2Te_5$ Alloy
Memory Mechanism	Low Resistance  High Resistance	Low Resistance(Crystal)  High Resistance (Amorphous)
State Change	Non-Melting Process by a Short Range Site Change of the Ge Atom	Crystal-Amorphous Phase Change due to Melting Process by Joule Heating

New optical memory, interface phase-change memory using super-lattice material, was first proposed by Tominaga et al. [25]. A new electrical non-volatile memory called TRAM (Topological switching RAM) has been developed by LEAP by modifying the interface phase-change memory [26, 27]. As illustrated in Table 2.3, the TRAM consists of a $GeTe/Sb_2Te_3$ super-lattice. In the PRAM, set and reset is performed by the phase-change of the $Ge_2Sb_2Te_5$ alloy, in other words, state change between crystal-phase (low resistivity) and amorphous phase (high resistivity) through a melting and re-crystallizing process. In the TRAM, Ge atoms change sites by the electron- and the hole-injection. This state-change is the non-melting process, and requires relatively small energy. Furthermore, the state-change is much faster as compared to the usual melting phase change.

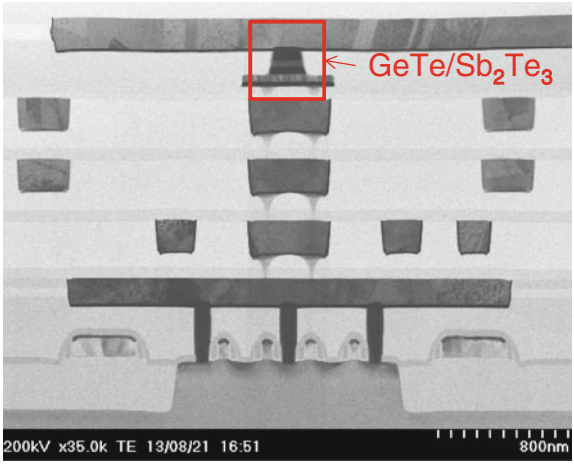


Fig. 2.26 Cross-section of the fabricated 1T-1R $GeTe/Sb_2Te_3$ Super-lattice TRAM cell [26] (© 2014 IEEE)

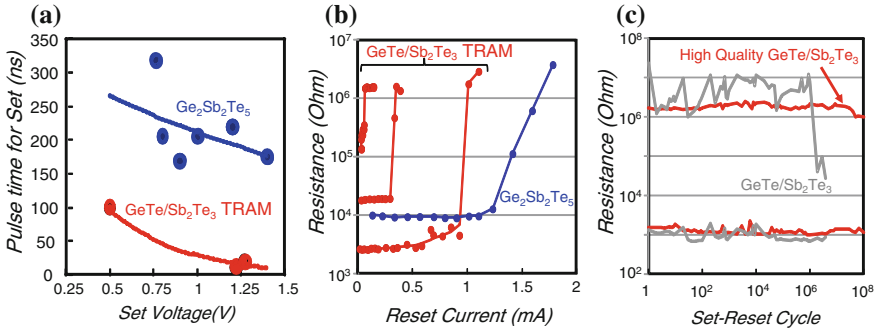


Fig. 2.27 Performance of the $GeTe/Sb_2Te_3$ Super-lattice TRAM [27] (© 2013 IEEE). **a** Pulse time as a function of the set-voltage. **b** Resistance as a function of the reset-current. **c** Set-reset cycle endurance

Figure 2.26 shows the cross-section of the fabricated 1Transistor-1Resistor (1T1R) $GeTe/Sb_2Te_3$ super-lattice TRAM cell. The TRAM cell is formed in the back-end process between metal 4 and 5 by PVD. Some of the performance data of the TRAM cell are compared with those in the PRAM cell in Fig. 2.27. The pulse-time for set is much smaller as compared to that of PRAM as shown in Fig. 2.27a. Resistance-change from low to high (reset) occurs at much lower reset current as shown in Fig. 2.27b. Set- and reset-cycles over 10^8 were observed. It was also demonstrated that the Ge_xTe_{1-x}/Sb_2Te_3 periodic layers, with $x < 0.5$, yield smaller set- and reset-current of 55 μA with less than 1 V set- and reset-voltages [28]. Storage-class memory using the TRAM cell is yet to be developed. These early results suggest that TRAM could be a promising candidate as a storage-class non-volatile memory that coexists with large-capacity flash memories in the storage system.

2.4 3D Integration

3D integration is regarded to be a solution in many applications. These include large-capacity flash memories, DRAM with wide bus interface, and high-performance processors. 3D integration can also realize hetero-integration consisting of power-delivery, analog and sensors, and digital signal-processing. This potential is covered broadly in Chap. 3.

3D flash memories comprising monolithically-integrated 3D memory-cell arrays were developed as shown in Fig. 2.28a [6]. Production of monolithically-integrated 3D flash memory has begun in 2013. This is an effective approach to solve the memory-capacity bottleneck in the flash memories. Since small-pitch interconnects and via with very high aspect-ratio are required in such applications, technology development to apply material other than Cu is now under way in many R&D projects. Metal interconnect such as Cu needs a barrier-metal. Due to the higher

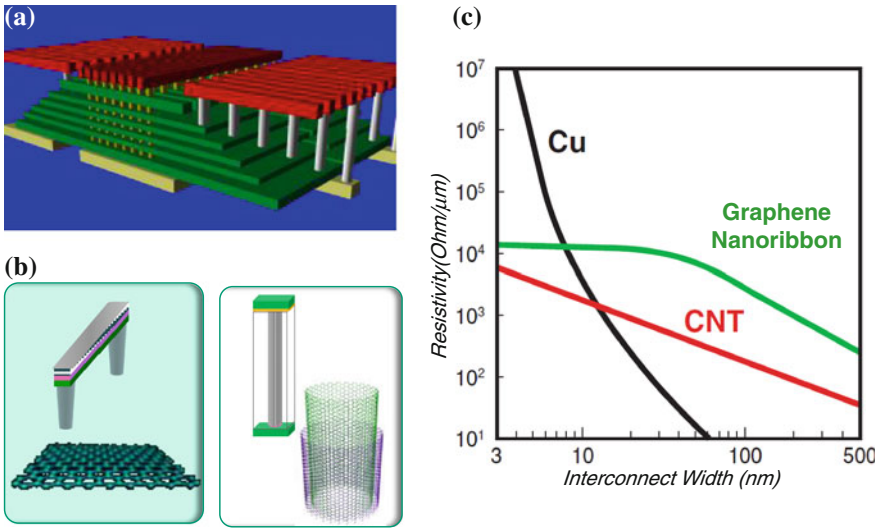


Fig. 2.28 Graphene and carbon-nanotube (CNT) as the candidate material for monolithically-integrated 3D flash memory. **a** Conceptual view of a BICS flash memory [6] (© 2007 IEEE). **b** Horizontal interconnect using graphene (*left*) and carbon-nanotube vertical via (*right*) (© LEAP). **c** Interconnect resistivity challenge in high-density integrated circuits [29] (© 2007 IEEE)

resistivity of the barrier-metal and surface scattering, metal-interconnects with small widths suffer from the increase of the resistivity, whereas graphene nano-ribbon is a promising material for narrow interconnect due to the low resistivity as shown in Fig. 2.28c [29]. Figure 2.28b illustrates a possible technology to solve the interconnect bottleneck, under development in LEAP using nano-carbon interconnect. Figure 2.29 shows the cross-sectional TEM photographs of the prototype

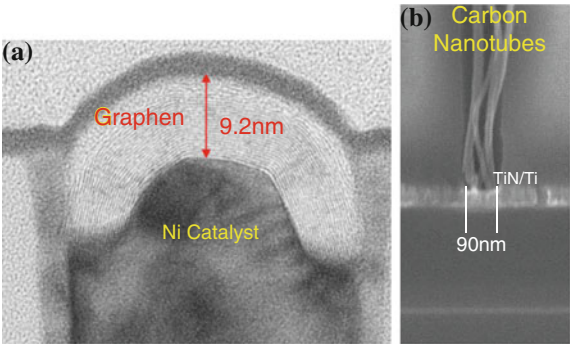


Fig. 2.29 Carbon interconnect technology under development for 3D flash memory [30, 31] (© LEAP). **a** CVD-grown multilayer graphene interconnect on Ni catalyst. **b** Carbon nanotubes grown in a via with aspect-ratio of 19

multi-layer graphene grown by CVD on a Ni catalyst at a temperature below 650 °C, and a carbon-nanotube via for vertical interconnection, both under development in LEAP [30, 31].

In video-data-processing of mobile equipment such as smart-phones or tablets, 3D-stacked DRAM is desirable to realize wide-bus data-transmission requirements between DRAM and processor with small footprint. It has been regarded as a candidate technology to solve several bottlenecks to realizing higher integration. The production of the 3D-stacked DRAM IC was already announced by several manufacturers. To achieve higher performance in high-end processors, 3D-chip stack approaches were also developed. There still remain a number of challenges. In high-end 3D-stacked microprocessors, heat-flux from a chip to the stacked chips causes performance degradation and thermal stress, and that may give rise to reliability problem. Therefore, effective dissipation of power of the 3D-stacked IC's is required. Another challenge is the integration of the chip-design and the chip-supply chain. If a 3D-stacked chip is designed and assembled with chips from different manufacturers, they need to be designed using the same design-rule for 3D-integration. It is also desirable that each chip is the tested known-good-die (KGD). The quality of the chips from different chip-manufacturers also needs to be assured. These challenges need to be solved in the supply-chain of the 3D-stacked chips.

An example of one of the promising chip-stack technologies is the chip-bonding to wafer by a self-assembly technique developed by Prof. M. Koyanagi's group, Tohoku University, as shown in Fig. 2.30. They demonstrated a 38-chip-stack by a

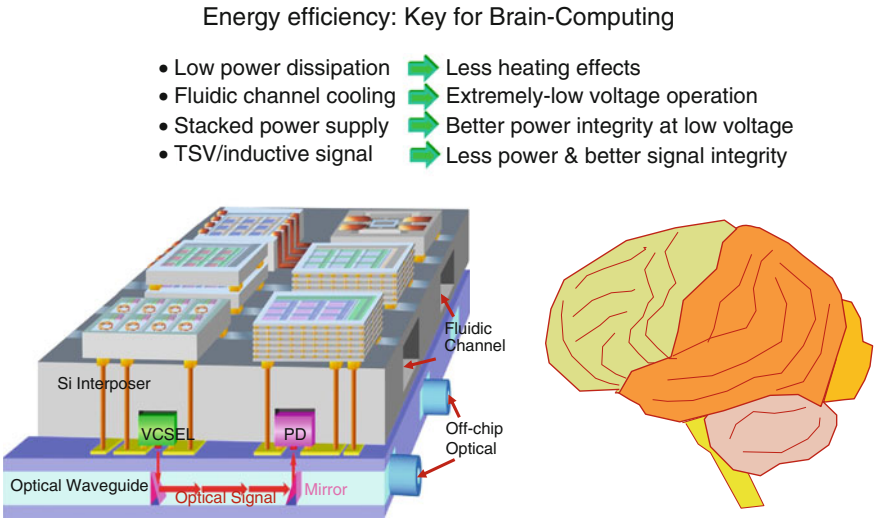


Fig. 2.30 Conceptual 3D stacked-chip integration drawn by Prof. M. Koyanagi. Combination of low-voltage, and energy-efficient chips and 3D stacked-chips could open ways for brain-computing [32] (Courtesy Koyanagi, © 2005 IEEE)

self-alignment technique [32]. Advantages of applying the 3D-integration to low-voltage stacked-IC's is illustrated in Fig. 2.30. If extremely low-power IC's are stacked with wireless power delivery from the stacked power-supply chips, metallic interconnections and wires for power-delivery and bulk heat-dissipation could be eliminated. It also makes possible an ideal low-temperature cooling through micro-fluidic channels to obtain a very steep sub-threshold slope. In the first demonstration of bulk-CMOS operation at 77 and 4.2 K, it was shown that the steep sub-threshold slope at low temperature makes possible low-V_{dd} operation [33]. If the V_{th} variation is minimized, this approach might realize extremely low-power operation. An ideal low-voltage and low-power processing might be possible in the future computing by using such technologies. 3D chip-stack technology is not only effective to be applied to traditional Von-Neumann architecture processors, but also to other types of emerging architectures, such as brain computing (Chap. 18) that require a lot of interconnections. Such an approach would open ways to a future computation paradigm.

2.5 The Future of Low-Power Integrated Circuits

Disruptive low-power IC technologies are required in the era of big data, IoT, and cloud-computing. In this chapter, some of the candidate technologies under development in LEAP were described. These include hybrid SOTB-CMOS, MRAM, CAS switch, TRAM, and nanocarbon-interconnect technology. Due to the explosion of data and transactions via internet, future data-centers require solutions utilizing energy-efficient processors and storages using low-voltage CMOS and non-volatile memories. Mobile terminals and robots also require performance/power efficiency. The future society depends on networked wireless IoT-sensors. They require wireless access and maintainable power-delivery means. These future devices, equipment, and systems are integrated by volume-efficient technologies such as monolithically-integrated 3D (Chap. 3) or 3D-stacked chips. Low-power post-fabricated programmable chips also provide cost-effective solutions for various kinds of applications.

Low-power electronics and IT technologies are also essential to establish a safe and sustainable human society. Past civilizations continuously over-consumed natural resources, and the current civilization is even accelerating the consumption. We expect that the world population would reach 8–10 billion sometime in the near future. In a closed system "earth", a catastrophe may occur to us if we continue our life-style of destroying the nature of earth. Although there have been continuing discussions on the direction of the climate-change, common consensus is that reducing energy-consumption, i.e. the exhaust of CO_2, and preserving forest and oceanic resources are the key issues for the future sustainability. Sensor networks and the advanced climate simulations may help monitoring and predicting the climate change.

The infrastructure of the modern society is formed by steel and steel-reinforced concrete with the lifetime of less than 200 years, much shorter than the Roman concrete used in Pantheon, Rome, built 1900 years ago. Life-cycle management and maintenance of the urban infrastructure have become key safety-issues. Sensor-networks may help monitoring and warning the deterioration and destruction. In such applications, energy-embedded or energy-harvesting (Chap. 19) sensors with wireless interface are the key components in the system.

Establishing a more resilient society against unusual catastrophes such as earthquakes, super-storms, floods, tsunamis, landslides, is also an urgent issue. The 2004 Indian Ocean Tsunami after the *M9.1* Richter-scale earthquake occurred near the west coast of Sumatra, and it claimed 230,000 lives in South-east Asia. In Japan, we experienced the East-Japan earthquake with a magnitude of *M9.0*, on Mar. 11, 2011, and the subsequent tsunami having a height of 14–20 m. This caused the loss of over 18,000 lives and the meltdown of the nuclear reactors in Fukushima. At that time, all the social systems, municipal, transportation, medical, energy and food supply, information, and communication did not function due to the loss of energy. In Philippine, over 6200 lives were lost by the super-typhoon Yolanda in 2013, and in the U.S., over 1800 lives were lost by Hurricane Katrina in 2005.

We have not yet experienced a super-volcanic eruption in the historical era. But geological evidences indicate that our prehistoric ancestors experienced catastrophes in Toba, Sumatra-Indonesia, 70,000 years ago, and in Kikai Island, south of Kyushu-Japan, 7300 years ago. If such super-volcanic activities occur in the future, only a society capable of forecasting the future and making sustainable and quick decisions, can function. Detection and handling of asteroids is also a big concern to the continuation of the human society. A worldwide safety-network is definitely required. Networked sensors, IT's, communication means, and electronics, utilizing low-power

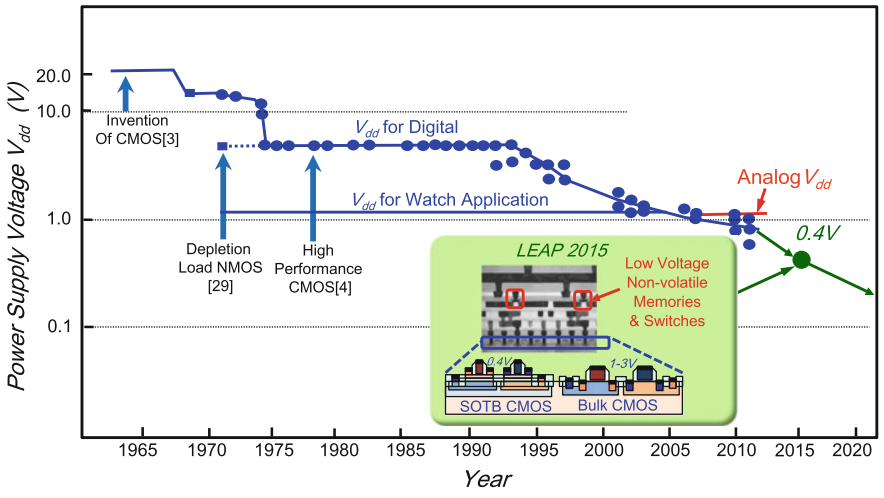


Fig. 2.31 Trend of the power-supply voltage of MOS-IC's in the past 50 years appeared in major circuit conferences (© LEAP)

integrated circuits, are essential elements to gather and analyze data, to perform simulations, to help leaders and to provide information to people in such a catastrophe.

Figure 2.31 illustrates the power-supply voltage in the past 50 years. PMOS-IC's, the major technology during the 1960s, and the first CMOS by Wanlass and Sah in 1963, were operated above 20 V. Then +5 V single-supply, depletion-load NMOS was developed [34], and +5 V became the major supply-voltage due to TTL compatibility and lasted for approximately 20 years. An exception was the low-voltage CMOS for watches and calculators that use 1.0–1.5 V battery. Gradual reduction of the supply-voltage occurred after the late 1990s. In the 2010s, near-threshold or sub-threshold operation has become popular particularly for low-power IC's. The technology developed in LEAP contributed to reduce the power-supply voltage to less-than-0.5 V in digital IC's. In the year 2020 and beyond, integrated circuits may require even lower supply-voltages of less than 100 mV. Transistors with much steeper sub-threshold slope and smaller variation are the key elements, and several candidate technologies, such as tunnel MOSFET (Chap. 1) or nanowire FETs, are under development. It should be noted that the new steep sub-threshold transistors must fulfill the requirement of small variation, controllability of V_{th}, enough I_{ON} (on-current) for digital circuits, good analog device parameters such as f_T, f_{max}, *Noise*, V_{offset}, distortion, and power-handling capability. A possible solution is the hybrid use of some new transistors and bulk-CMOS or SOTB-CMOS as the platform technology.

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