

# Contents

<b>1</b>	<b>Memristor Fundamentals</b>	<b>1</b>
1.1	Introduction	1
1.2	Memristor Defined by a State-Dependent Ohm’s Law	2
1.3	Fingerprints of Memristors	3
1.4	Memristor Defined by a “Pinched” Hysteresis Loop	4
1.5	The “Ideal” Memristor	6
	References	7
<b>2</b>	<b>Memristor Modeling</b>	<b>9</b>
2.1	Introduction	9
2.2	A Novel Threshold-Type Memristor Circuit Model	10
2.3	Modeling Memristors in SPICE	15
2.4	Model Verification	20
	2.4.1 Fitting to a Reference Model	20
	2.4.2 Testing in Complex Memristive Circuits	23
2.5	Overview and Comparison	25
	References	26
<b>3</b>	<b>Dynamic Response of Multiple Interconnected Memristors</b>	<b>29</b>
3.1	Introduction	29
3.2	Study of Composite Memristive Structures	31
	3.2.1 Memristors Connected in Series	31
	3.2.2 Memristors Connected in Parallel	41
3.3	Generalized Concept for the Construction of Composite Memristive Systems	47
	3.3.1 Circuit Examples Combining First/Second-Level Memristive Compositions	49
	3.3.2 Fine-Resolution Programmable Memristive Switches	53

3.4	Application of Composite Memristive Systems in Computing Circuits. . . . .	55
3.5	Overview and Discussion . . . . .	57
	References . . . . .	58
<b>4</b>	<b>Memristor-Based Logic Circuits . . . . .</b>	<b>61</b>
4.1	Introduction . . . . .	61
4.2	Switching Dynamics of Threshold-Type Memristors and Memristive Compositions . . . . .	62
4.3	Popular Logic Design Concepts Based on Memristors . . . . .	64
4.3.1	Material Implication (IMPLY)—Based Logic . . . . .	64
4.3.2	MRL—Memristor “Ratioed” Logic . . . . .	67
4.3.3	CMOS/Memristor Threshold Logic . . . . .	69
4.4	CMOS-like Memristor-Based Logic Circuit Design . . . . .	71
4.4.1	Implementation in Hybrid Nano-CMOS Memristive Crossbar . . . . .	74
4.4.2	Verification Using SPICE. . . . .	78
4.4.3	Application in Larger Combinational Circuits . . . . .	82
4.4.4	Overview and Comparison . . . . .	91
4.5	A Memristive Logic Family for Parallel Processing of Applied Input Signals. . . . .	92
4.5.1	Boolean Logic Operations Based on Threshold-Type Resistance Switching . . . . .	93
4.5.2	Verification Using SPICE. . . . .	96
4.5.3	Overview and Comparison . . . . .	97
	References . . . . .	98
<b>5</b>	<b>Memristive Crossbar-Based Nonvolatile Memory. . . . .</b>	<b>101</b>
5.1	Introduction . . . . .	101
5.2	Overview of Redox-Based RAM Device Technology. . . . .	104
5.2.1	Metal Oxide-Bipolar Filamentary ReRAM . . . . .	105
5.2.2	Metal Oxide-Unipolar Filamentary ReRAM . . . . .	106
5.2.3	Metal Oxide-Bipolar Non-filamentary ReRAM . . . . .	106
5.3	Memristive Memory Cell Operation Principles. . . . .	107
5.3.1	Anti-serial Memristive Switch (ASM) . . . . .	109
5.3.2	Anti-parallel Memristive Switch (APM) . . . . .	110
5.3.3	Pulse Properties of ASMs and APMs. . . . .	111
5.4	Sneak-Path Challenge in Memristive Crossbar-Based Memory. . . . .	113
5.4.1	Fundamentals of Memristive Crossbar Based Memory . . . . .	113
5.4.2	Estimation of Read Margins . . . . .	114
5.4.3	Sneak Path Negative Impact in Readout Performance. . . . .	117
5.4.4	ASM/APM-Based Crossbar Array . . . . .	119
5.4.5	Alternative Crossbar Topologies . . . . .	125

5.4.6	Simulation-Based Evaluation of Alternative Topologies . . . . .	126
5.4.7	Application of Alternative Topologies to ASM-Based Crossbar. . . . .	132
5.4.8	Overview and Discussion . . . . .	133
5.5	XbarSim—An Educational Simulation Tool for Memristive Crossbar-Based Circuits . . . . .	135
5.5.1	Details on the Simulated Circuit Topology . . . . .	137
5.5.2	GUI-Based Simulation Procedure. . . . .	140
5.5.3	Simulation Details—Crossbar Network Nodal Analysis . . . . .	141
	References . . . . .	144
<b>6</b>	<b>High-Radix Arithmetic-Logic Unit (ALU) Based on Memristors . . .</b>	<b>149</b>
6.1	Introduction . . . . .	149
6.2	Overall Layout of the Memristive Multi-level Memory System . . . . .	151
6.2.1	Multi-level Storage Cell . . . . .	152
6.2.2	Analysis of the Circuit Topology. . . . .	155
6.3	Enhanced Crossbar for Memristive ALU with Built-in Memory. . . . .	160
6.3.1	Parallel Creation of Partial Products for Fast Multiplication . . . . .	162
6.4	Simulation Results . . . . .	164
6.5	Overview and Discussion . . . . .	169
	References . . . . .	170
<b>7</b>	<b>Networks of Memristors and Memristive Components . . . . .</b>	<b>173</b>
7.1	Introduction . . . . .	173
7.2	Memristive Network-Based Computations. . . . .	175
7.2.1	Description of the Computing Platform and Its Function . . . . .	176
7.2.2	Memristive Circuits for Modeling Edges of Directed (Oriented) Graphs . . . . .	179
7.3	Path Computing and Maze-Solving with Ariadne’s Memristive Thread. . . . .	181
7.3.1	Fully Interconnected Network . . . . .	181
7.3.2	Defective Network. . . . .	185
7.3.3	Maze-Solving . . . . .	187
7.4	Mapping Problems Defined in Directed Graphs . . . . .	192
7.5	Overview and Discussion . . . . .	194
	References . . . . .	196

<b>8</b>	<b>Memristive Computing for NP-Hard AI Problems . . . . .</b>	<b>199</b>
8.1	Introduction . . . . .	199
8.2	Basics of Cellular Automata and Suitable HW Structures for Their Implementation . . . . .	200
8.3	Application Mapping Methodology to Memristive CA-Based Circuits . . . . .	203
8.4	Solving NP-Hard Artificial Intelligence Problems. . . . .	206
8.4.1	Shortest Path and Traveling Salesman Problems . . . . .	206
8.4.2	The Max Clique Problem . . . . .	213
8.4.3	The Sorting Problem . . . . .	217
8.4.4	The Bin Packing Problem. . . . .	222
8.4.5	The Knapsack Problem . . . . .	231
8.5	Overview and Comparison . . . . .	237
	References . . . . .	239

**Memristor-Based Nanoelectronic Computing Circuits  
and Architectures**

Foreword by Leon Chua

Vourkas, I.; Sirakoulis, G.

2016, XXV, 241 p. 117 illus., 100 illus. in color.,

Hardcover

ISBN: 978-3-319-22646-0