

Chapter 2

Memristor Modeling

2.1 Introduction

Since the exciting discovery of nonvolatile memristive behavior in Titanium dioxide (TiO_2)-based nano-films at Hewlett Packard (HP) Labs in 2008 [1], both academia and industry have been engaged in the search for novel memristive materials and manufacturing technologies. HP's version of the TiO_2 substrate memristor remains up to now the most generally recognized memristor type. It is based on two thin-layer TiO_2 films. The bottom layer acts as an insulator whereas the top film layer acts as a conductor via oxygen vacancies in the TiO_2 ; TiO_2 changes its resistance in the presence of oxygen. Voltage increment moves the oxygen vacancies from the top layer towards the bottom layer, thus changing its resistance. A great deal of ongoing work has been devoted to the development of mathematical models capable to capture the complex dynamics exhibited by these nanostructures. An appropriate descriptive model will not only lead to a better understanding of its behavior, but will also result to a better exploitation of its unique properties in novel systems and architectures combining data storage and data processing in the same physical location.

Currently there are several available device models which attempt to characterize both current–voltage (i – v) behavior as well as the device dynamics [2–9]. The HP group, in their first memristor implementation announcement, suggested a coupled variable-resistor model for memristors [1]. This model was later improved by Joklegar and Wolf [10], whereas several papers by HP [11, 12] reported on further developments of resistance switching theory for TiO_2 -based devices. Nevertheless, until nowadays there has been no direct connection between a model and the memristor physical properties. Only a few models were derived on the basis of material characterization and experimental electronic measurements, thus giving some hint on the physical mechanisms at the origin of the unique behavior of memristors [9, 13]. However, given the complexity of the physical processes that occur in the devices, the corresponding detailed mathematical descriptions are

usually far too complex to solve analytically and numerical solutions are too time consuming to include in a simulation. Moreover, since simulation with Simulation Program with Integrated Circuit Emphasis (SPICE) is common practice in circuit development, several models of memristors were also implemented in SPICE [2, 5–8, 14–20].

The study of some of the most noteworthy published memristor models has shown that simple models are able to reproduce most of the dynamics observed with more accurate models, whose far greater computational complexity may lead to convergence problems and instability issues in complex circuits [21]. For example, the original linear oxygen vacancy drift model proposed by HP is valid only for certain choices of input signals and initial state of the memristance. Furthermore, a common problem in most models is that there is no threshold consideration. Threshold-type switching, though, is an extremely important common feature of the majority of experimental memristive devices. Physical memristor devices demonstrate a threshold voltage where hysteresis is not seen unless the voltage across the memristor exceeds the threshold [22]. Another important feature concerns the switching speed of memristors during the “set” and “reset” operations which generally are not similar [9, 22]. According to characterization data from HP Labs, the motion of the memristor state variable depends both on its current state and on the polarity of the applied voltage [9], something which could be attributed to the interaction of the external applied field, the internal field of the concentrated defects (e.g. charge traps, mobile ions, oxygen vacancies, etc.), and the diffusion, all acting in the same or in the opposite directions according to the applied voltage.

In the rest of this chapter we present a SPICE-compatible device model [23] of a voltage-controlled memristor which explains memristive behavior while primarily attributing the switching effect to an effective tunneling distance modulation [24]. This model aims to address most of the aforementioned shortcomings; it satisfies the desired memristive fingerprints [25] and involves significantly low-complexity operation under an unlimited set of frequencies over a wide range of applied voltages. The SPICE simulation results are found in good qualitative and quantitative agreement with the theoretical formulation of the model [26]. Also, the model represents well the complex switching behavior of memristor when fitted to other widely used published models. Therefore, it can be used to provide accurate enough circuit simulations for a wide range of memristor devices and voltage inputs, while it can be incorporated as a circuit element in any current computer-aided memristor-based circuit design work.

2.2 A Novel Threshold-Type Memristor Circuit Model

Inspired from the original circuit model proposed by HP for TiO_2 -based devices, the equivalent circuit of the proposed memristor model is depicted in Fig. 2.1.

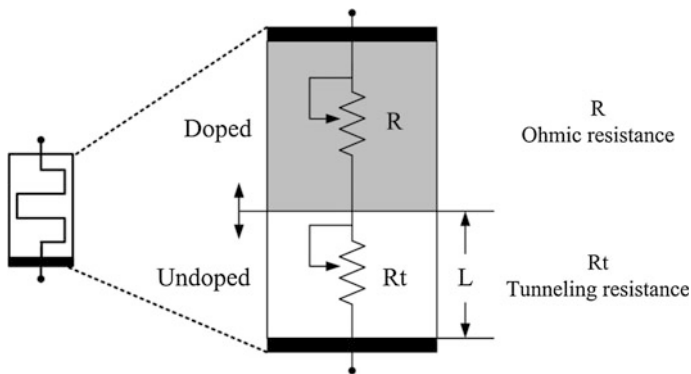


Fig. 2.1 Equivalent circuit of the coupled ohmic-tunneling variable-resistor circuit model

It concerns a threshold-type switching model of a two-terminal voltage-controlled electrical device that exhibits memristive behavior, whose general definition is given by the following equations:

$$I(t) = G(L, t)V_M(t) \quad (2.1)$$

$$\dot{L} = f(V_M, t). \quad (2.2)$$

Parameter L denotes the single state variable of the system (indicating the internal memristor state), which in our model is the tunnel barrier-width (e.g. the thickness of the free of oxygen vacancies dioxide layer), with the electrical current transport process being limited primarily by tunneling through it. G is the conductance (memductance) of the device, whereas I and V_M represent the flowing current and the applied voltage, respectively. In the coupled ohmic-tunneling variable-resistor equivalent circuit of Fig. 2.1, we consider an ohmic variable-resistor R and a tunneling variable-resistor R_t connected in series. R represents the resistance of the doped dioxide layer and R_t represents the tunneling resistance of the undoped layer of the device. The doped layer acts as a conductor whereas the undoped layer is a pure insulator. Therefore, there is a significant difference between the actual values of their resistances, with $R_t \gg R$, which is the reason why the model concentrates mainly on R_t .

The tunneling resistance R_t is expected to be proportional to the tunnel barrier width L , given the fact, that the larger the barrier width the higher the resulting resistance should be. Also, its value is anticipated to change according to the “movement” of the boundary between the two layers because of the transport of oxygen deficiencies under positive or negative applied voltage. Thus, any mathematical formulation for R_t could include at least a fitting parameter which would bound the effect of the varying geometry of the device on the actual concentration of the oxygen vacancies in either the doped or the undoped side of the film.

Furthermore, according to Schiff [24], Rt is inversely proportional to the product of the voltage-dependent tunneling transmission coefficient (T_0) and the electron effective density of states (N_{eff}), whereas it is exponentially proportional to the tunnel barrier-width (L). Therefore, its particular mathematical formulation is:

$$Rt(V_M) = \frac{1}{N_{eff}} \cdot \frac{e^{2k_{VM}L}}{T_{0,VM}}. \quad (2.3)$$

The voltage dependence of Eq. 2.3, due to the presence of the voltage-dependent parameters T_0 and k , can be translated into a corresponding variation of L ; it can be passed to a new voltage-dependent parameter $L_{V,t}$ with no significant error implication. In this model we define Rt to be described by the following equation:

$$Rt(L_{V_M,t}) = f_0 \cdot \frac{e^{2L_{V_M,t}}}{L_{V_M,t}}. \quad (2.4)$$

Equation 2.4 gives the resistance (memristance) of the device for a certain restricted range of the state variable L . All unknown material-specific and geometrical issues are contained into the model-fitting constant parameter f_0 . The qualitative agreement of Eqs. 2.3 and 2.4 verifies our assumption for the exponential dependence of Rt on L . Moreover, Pickett et al. in [9] reported on experimental results from the application of a dynamical testing protocol applied to a set of TiO_2 -based memristive devices. Through analysis of the switching dynamics that arise from ionic motion in the devices, it was concluded that electronic conduction in these devices is dominated by an effective tunneling barrier width that varies with time under the applied voltage. Thus, the switching effect is primarily attributed to an effective tunneling distance modulation, which is in line with the present assumptions for the Rt - L dependence.

A heuristic equation $L(V_M, t)$ that qualitatively gives the expected response of L as a function of the time t and the applied voltage V_M is given below:

$$L(V_M, t) = L_0 \cdot \left(1 - \frac{m}{r(V_M, t)}\right). \quad (2.5)$$

L_0 is the maximum value that L can attain. The term in parenthesis of Eq. 2.5, which contains a voltage-dependent parameter $r(V_M, t)$ and a fitting constant parameter m , determines the boundaries of the barrier width. By considering tunneling as the dominant physical mechanism, Eq. 2.5 introduces the initial as well as the current position of L which is limited within two boundary values. Parameter $r(V_M, t)$ defines both the device dynamics and the current state of the device. Its value is monitored and maintained within a valid range; i.e. when $r < r_{\text{MIN}}$ or $r > r_{\text{MAX}}$, it is set equal to r_{MIN} or r_{MAX} , corresponding to L_{MIN} and $L_{\text{MAX}} \approx L_0$, respectively. As a consequence, the memristance is correspondingly set to the most (R_{ON}) or the least

conductive state (R_{OFF}) via Eq. 2.4. Values for parameters m and r_{MIN} should be selected so that the fraction $(m/r_{\text{MIN}}) < 1$ (so, the tunnel barrier-width will never be zero).

Furthermore, since “set” and “reset” switching times can differ in many experimental memristive devices, this model is based on the assumption that the switching rate of L is small (fast) below (above) a threshold voltage (V_{SET} or V_{RESET}), which is viewed as the minimum voltage required to impose a change on the physical structure, and thus the memristance, of the device. This assumption is encapsulated in the use of the voltage-dependent parameter $r(V_M, t)$, whose time derivative is slow or fast depending on the applied voltage, as shown below:

$$\dot{r}(V_M, t) = \begin{cases} a_{\text{RESET}} \cdot \frac{V_M + V_{\text{RESET}}}{c + |V_M + V_{\text{RESET}}|}, & V_M \in [-V_0, V_{\text{RESET}}) \\ b \cdot V_M, & V_M \in [V_{\text{RESET}}, V_{\text{SET}}] \\ a_{\text{SET}} \cdot \frac{V_M - V_{\text{SET}}}{c + |V_M - V_{\text{SET}}|}, & V_M \in (V_{\text{SET}}, +V_0] \end{cases} \quad (2.6)$$

Equation 2.6 comprises one-parameter sigmoid functions for the regions above the thresholds (first and last branch), whereas a linear relation of the applied voltage is used for the region below the thresholds. Parameters a_{RESET} , a_{SET} , b , and c are fitting constants that are used to shape the intensity of the state variable dynamics, i.e. the rate of memristance change, with $a_x \gg b$ and $0 < c < 1$. Setting $b = 0$ imposes a hard switching behavior, i.e. there is no state change in the memristor unless a certain voltage threshold is exceeded. Different thresholds and switching rates can be programmed by tuning the shaping parameters of $r(V_M, t)$; a different set of values for the parameters $\{a_x, b, c, m\}$ defines a different set of boundaries for the tunnel barrier-width. The model parameters are certainly determined by material properties of the modeled memristor, such as the effective tunneling distance, etc. However, here they are regarded as fitting parameters that yield visibly different i - v curves. Note that Eqs. 2.4–2.6 are written in such a way that when $\{a_x, b\} > 0$ then a positive (negative) voltage applied to the top terminal with respect to the bottom terminal (denoted by the black thick line in the memristor circuit schematic), tends to decrease (increase) the memristance of the device.

Figure 2.2 qualitatively shows the simulation results for the response of a memristor under sinusoidal applied voltage according to the proposed model (the effect that the different frequencies of the applied voltage have on the switching behavior will be discussed later). In the graphical representation of Eq. 2.6 in Fig. 2.2e, the two separate sigmoid functions were included to facilitate visual correspondence. It is obvious that in the region $[-V_0, V_{th})$ the black line follows the green sigmoid graph whereas in the region $(V_{th}, V_0]$ it follows the red graph.

Figure 2.3 shows some calibration options offered by the model. More specifically, Fig. 2.3a, b show how the memristance range can be adjusted by modifying the L_0 and f_0 parameter values. A higher L_0 enlarges the $[R_{\text{ON}}, R_{\text{OFF}}]$ memristance range in an exponential manner, whereas different values for the parameter f_0

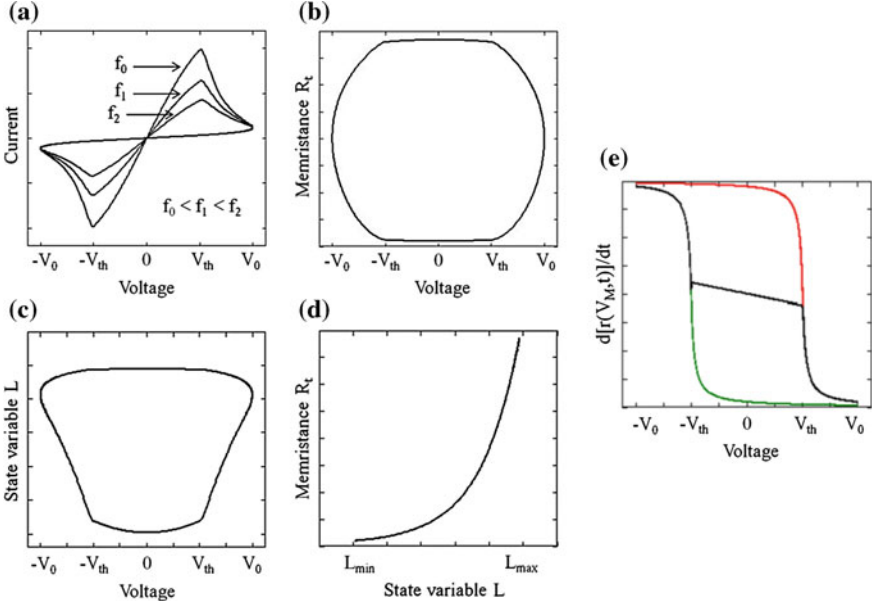


Fig. 2.2 **a** I - V characteristic of a memristor under AC voltage $V(t) = V_0 \cdot \sin(2\pi ft)$ for different frequencies $f_0 < f_1 < f_2$ of $V(t)$ with threshold voltages $V_{RESET} = V_{SET} = V_{th}$. **b** The memristance R_t with the applied voltage. **c** Response of the state variable L according to the applied voltage. **d** The memristance R_t for a restricted range of L according to Eq. 2.4. **e** Graphical demonstration of Eq. 2.6; in the regions above the thresholds the *black line* follows either the *green* (region $[-V_0, -V_{th})$) or the *red* (region $(V_{th}, V_0]$) sigmoid function

displace equally the above range so that $[R_{ON}, R_{OFF}]_{NEW} = (f_{0,NEW}/f_0) \times [R_{ON}, R_{OFF}]$. Except the threshold voltages V_{RESET} and V_{SET} which can be set asymmetric, since α is the max value for the rate of change of parameter r , different a_{RESET} and a_{SET} can lead to different switching times which depend on the polarity of the applied voltage.

The time derivative of the state variable in Eq. 2.2 is interpreted as the speed of movement of the barrier between the two layers due to the applied voltage. However, several memristive devices have been proposed using different material structures [22], so the resistance switching mechanism is not always due to the change in thickness of a specific material layer. This model has the potential to describe memristive functionality in a more generalized way if the state variable is normalized between 0 and 1. This can be done by dividing $L(V_M, t)$ with L_0 and by multiplying with L_0 the exponent and also the denominator of Eq. 2.4. Therefore, when $L \approx 0$ the memristor is in the most conductive state, whereas the least conductive state occurs when $L \approx 1$ (instead of $L \approx L_0$). This change in the state variable represents a generalization of the model so that it can represent more types of memristive devices.

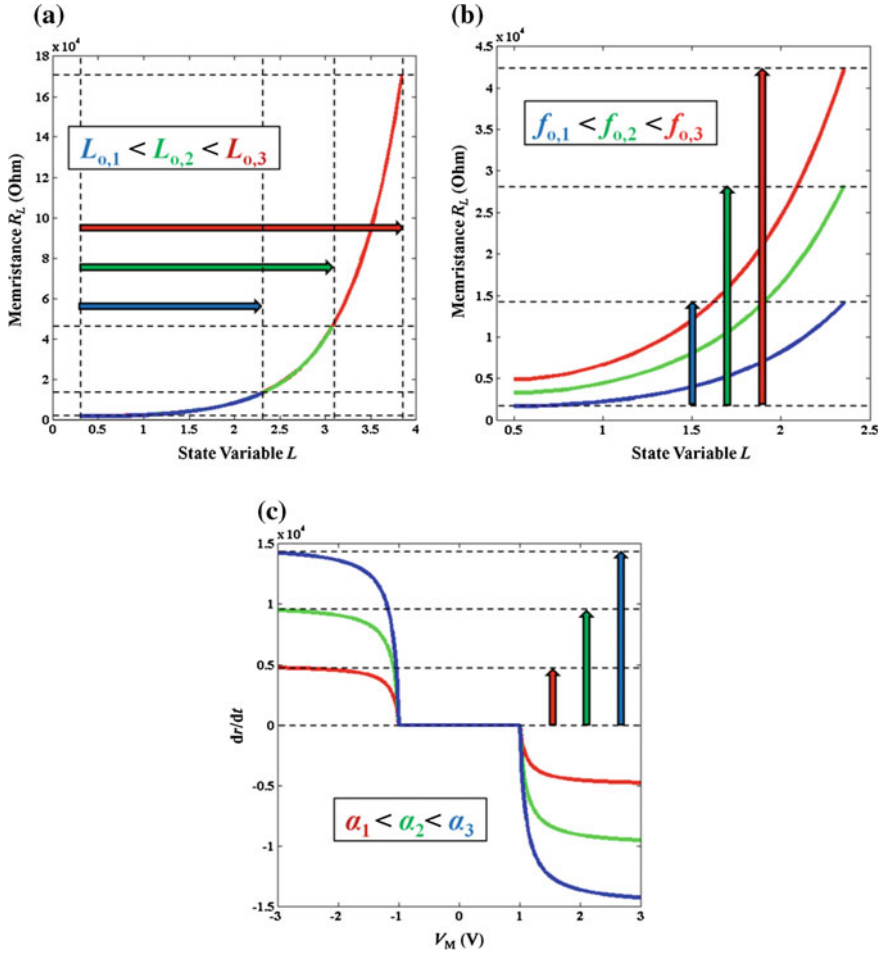
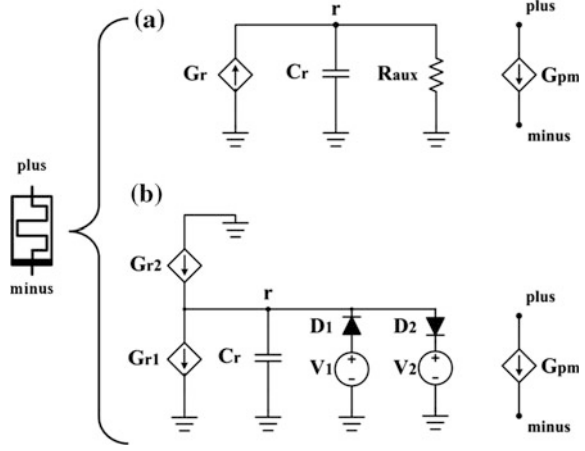


Fig. 2.3 Model calibration options. **a** The effect of different L_0 parameter values on the memristance range. **b** The effect of different f_0 parameter values on the memristance range. **c** The effect of different a parameter values on the rate of change of parameter r

2.3 Modeling Memristors in SPICE

We developed a behavioral model of a memristor at device level using the SPICE circuit description language by following the mathematical equations presented before [26]. We implemented the voltage-controlled memristor model into a simple netlist where the memristive device is realized as a sub-circuit consisting of several elements, thus making it easy to comprehend and ready to be used in memristor-based systems.

Fig. 2.4 Two different equivalent versions of the corresponding circuit schematic of the SPICE memristor model



The circuit layout for the SPICE model based on Eq. 2.1 and on Eq. 2.4 through Eq. 2.6 is shown in Fig. 2.4, where two different versions are presented. Memristor SPICE models have been previously proposed using a similar setup in [14]. In Fig. 2.4a the memristive system is realized as a sub-circuit combining two current sources G_{pm} and G_r , an integrating capacitor C_r (modeling the memory effect of the memristor) and a resistor R_{aux} . This is the most compact corresponding schematic. The current source G_r generates a current based on Eq. 2.6. The voltage across the capacitor (at node r : V_r) defines the value of parameter $r(V_M, t)$. In both versions the two terminals (*plus* and *minus*) of the additional current source G_{pm} , which plays the role of a behavioral resistor, represent the top and bottom electrodes of the device. The output of the current source G_{pm} is set using the voltage drop across the terminals of the device and the memristance given by Eq. 2.4. However, in this setup, $r(V_M, t)$ can step out of the valid interval, which would yield invalid and unstable solution. Therefore, an appropriate smoothing function, which takes this into account, is necessary to avoid convergence problems. The purpose of such function is to limit $r(V_M, t)$ inside the valid value interval between the defined boundaries r_{MIN} and r_{MAX} . The exact use of the aforementioned function can be seen in the respective SPICE netlist in Table 2.1.

In Table 2.1 the first lines briefly comment on the most important parameters of the model. Initialization of the parameters takes place in lines 3–4 and the selected values for the parameters $\{r_{MIN}, r_{MAX}, L_0, m, f_0\}$ provide a resistance ratio of two orders of magnitude with $\{R_{ON}, R_{OFF}\} = \{2, 200\}$ k Ω . In the first netlist, line 7 specifies the capacitor C_r with an initial condition. By setting the initial value of the voltage across the capacitor r_{init} equal to either of the boundary values (or to any valid value in between) we indicate the initial state of the device. The value of the current source declared in line 5 is equal to the right hand side of Eq. 2.6, where the smoothing function $st_f(\cdot)$ (step function) is used to define which branch of Eq. 2.6 applies each time according to the applied voltage at the terminals of the device. Line 10 describes the current source G_{pm} which defines the current running through

Table 2.1 Voltage-controlled memristor SPICE model netlists

```

* rmin,rmax : Boundary values for r
* rinit      : Initial value of f
* Lo         : Tunnel barrier width
* VtL,VtR    : Left and Right Threshold voltages
* alpha,
* beta,gamma: Parameters for modeling non-linear
*             threshold-based behavior
* m,fo       : Model's fitting parameters
* yo         : Smoothing function's parameter
*****
*Netlist corresponding to Fig. 2.4(a)
1 .subckt memristor plus minus PARAMS:
2 *Parameters' values
3 +rmin=100 rmax=390 rinit=390 alpha=1E15
  beta=10 gamma=0.1 VtR=1.5 VtL=-1.5 yo=0.0001
4 +m=82 fo=310 Lo=5
5 Gr 0 r value={dr_dt(V(plus)- V(minus))* (
  st_f(V(plus)-V(minus))*st_f(V(r)-rmin)+
  +st_f(-(V(plus)-V(minus))) *st_f(rmax-V(r))) }
6 Cr r 0 1 IC={rinit}
7 Raux r 0 1E12
8 *Current equation Imem = V / R(L)
9 Gpm plus minus value={ (V(plus)-
  V(minus)) / ((fo*exp(2*L(V(r)))) / L(V(r))) }
10 *Func. for non-linear threshold-based behavior
11 .func dr_dt(y)={-alpha*((y-VtL)/(gamma+abs(y-
  VtL)))*st_f(-y+VtL)-beta*y*st_f(y-VtL)*
12 +st_f(-y+VtR)-alpha*((y-VtR)/(gamma+abs(y-
  VtR)))*st_f(y-VtR)}
13 *Smoothing function
14 .func st_f(y)={1/(exp(-y/yo)+1)}
15 *L(V) function
16 .func L(y)={Lo-Lo*m/y}
17 .ends memristor

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*Netlist corresponding to Fig. 2.4(b)
1 .subckt memristor plus minus PARAMS:
2 *Parameters values
3 +rmin=100 rmax=390 rinit=390 alpha=1E15
  beta=10 gamma=0.1 VtR=1.5 VtL=-1.5 yo=0.0001
4 +m=82 fo=310 Lo=5
5 Gr1 0 r value={dr_dt(V(plus)-
  V(minus))*st_f(-(V(plus)-V(minus))) }
6 Gr2 0 r value={dr_dt(V(plus)-
  V(minus))*st_f(V(plus)-V(minus)) }
7 D1 k r Dbreak
8 V1 k 0 {rmin}
9 D2 r g Dbreak
10 V2 g 0 {rmax}
11 Cr r 0 1 IC={rinit}
12 *Current equation Imem = V / R(L)
13 Gpm plus minus value={ (V(plus)-
  V(minus)) / ((fo*exp(2*L(V(r)))) / L(V(r))) }
14 *Func. for non-linear threshold-based behavior
15 .func dr_dt(y)={-alpha*((y-tL)/(gamma+abs(y-
  VtL)))*st_f(-y+VtL)-beta*y*st_f(y-VtL)*
16 +st_f(-y+VtR)-alpha*((y-VtR)/(gamma+abs(y-
  VtR)))*st_f(y-VtR)}
17 *Smoothing function
18 .func st_f(y)={1/(exp(-y/yo)+1)}
19 * L(V) function
20 .func L(y)={Lo-Lo*m/y}
21 .ends memristor

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the device according to the applied voltage and the memristance given by Eq. 2.4. The resistor R_{aux} , described in line 8, has an auxiliary role. It is used to model the memory retention capability, which is an important aspect of experimental memristor realizations, thus taking into account the case where memristance can change over time even when no voltage is applied [27]. The desired changing pace depends on the particular value of the resistor. R_{aux} does not affect the switching behavior of the device when being accessed; hence it can be omitted if retention is not considered.

Figure 2.4b shows a more thorough way of modeling both the memristive effect as well as the control of the boundary conditions. Here, the current source G_r is replaced by two current sources G_{r1} and G_{r2} which have opposed polarities and operate in such a way so that G_{r2} is responsible for charging the capacitor, and G_{r1} for discharging it. Their operation is better understood in the corresponding netlist shown in Table 2.1, where the necessary step functions are used to determine which source is active each time, according to the applied voltage. Moreover, the problem of limiting the boundaries of $r(V_M, t)$ is here addressed by using elementary SPICE diodes and DC voltage sources. More specifically, two more circuit branches are added to the initial sub-circuit of Fig. 2.4a, each one comprising a diode with a specific polarity and a DC voltage source. Their role is summarized as follows: if the voltage across the capacitor V_r [i.e. the value of parameter $r(V_M, t)$] falls below V_1 (rises above V_2) then diode D_1 (D_2) is forward biased and thus V_r is maintained equal to V_1 (V_2). In this setup we have set the values of the DC sources equal to the boundary values of $r(V_M, t)$; i.e. $V_1 = r_{\text{MIN}}$ and $V_2 = r_{\text{MAX}}$. However, since there is a value for the forward voltages of the diodes, the user either has to adjust their corresponding internal parameters and threshold values, or has to accept a slightly shifted value for the modeled borderlines of V_r . In the corresponding netlist presented in Table 2.1, the current sources G_{r1} and G_{r2} are declared in lines 5–6, whereas the circuit elements responsible for controlling the boundary conditions are defined in lines 7–10.

The second version of the model does not have the auxiliary resistor, which however can be included in order to extend the modeling capabilities by taking into account state retention, as mentioned before. Both presented versions of the SPICE equivalent circuit were tested and the simulation results were found identical.

The SPICE implementation was tested using the Cadence PSPICE simulation environment. Figure 2.5 illustrates the presented model response to a 3 V and 100 Hz sinusoidal voltage applied for a set of consecutive waveform periods. Existence of thresholds is obvious at the hysteretic i - v graph, whereas the nonlinear conducting behavior is also noted in the i - t characteristic. The voltage across the capacitor V_r is successfully restricted within the desired boundaries, which guarantee the stable operation of the model within the valid memristive region defined in the range $\{R_{\text{ON}}, R_{\text{OFF}}\} = \{2, 200\} \text{ k}\Omega$.

Furthermore, we shortly remind here the fingerprints of all memristors and memristive devices [25, 28] which were described previously in Sect. 1.3 of Chap. 1. The first characteristic is the pinched hysteresis loop which must hold for all amplitudes, for all frequencies, and for all initial conditions of any periodic

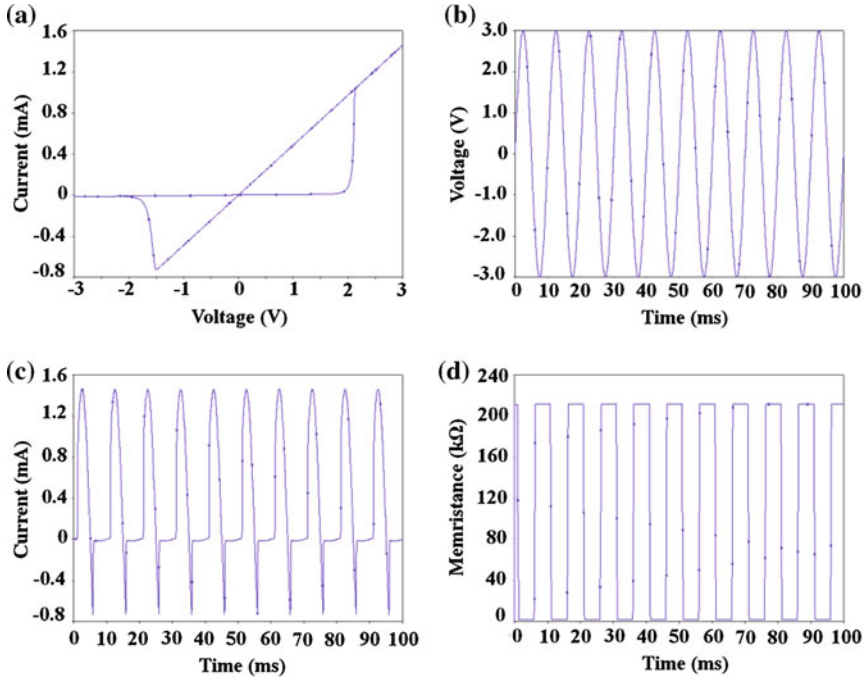


Fig. 2.5 SPICE model response to a 3 V and 100 Hz sinusoidal applied voltage. Values of the model parameters are used as given in Table 2.1 with $\alpha = 1e6$. **a** The i - v characteristic shows the existence of threshold voltages around $|1.5|$ V. The **b**, **c**, and **d** plots illustrate the applied voltage, the flowing current, and the memristance as a function of time

waveform which assumes both positive and negative values over each period (it is also pinched at the origin for any non-sinusoidal periodic waveform). The other fingerprint is that, for high frequencies of the applied periodic signal, the i - v loop collapses to a straight line. Thus, any considered memristor device model, based on an explicit memristive mechanism, should be capable of delivering such properties.

To this end, we include in Fig. 2.6 the dynamic response of the model to the application of voltage signals of different frequencies and also to the application of consecutive positive and negative pulses. Increasing the frequency of the external voltage leads to decreased hysteretic behavior of the memristor until it asymptotically passes over to the characteristic curve of a conventional resistor. The effect of the different frequencies (100, 110, 150 Hz) are depicted in sub-figure (a) where it can be seen that the memristive effect diminishes as the frequency grows. Thus, the i - v characteristic of a memristor degenerates to a straight line because the device is not given the necessary time to change its resistance while being biased. Also, sub-figure (b) shows the simulation results of the model when several consecutive sinusoidal voltage pulses are applied to the device in a stepwise manner. The input pulses are applied multiple times with the same polarity to study how the model switches to intermediate levels between the maximum and minimum resistance.

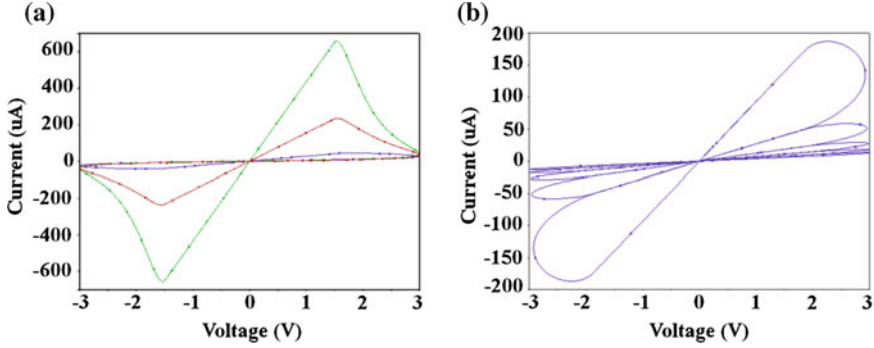


Fig. 2.6 Memristor SPICE model response to **a** a sinusoidal applied voltage of 3 V and 100 Hz (green), 110 Hz (red) and 150 Hz (blue), respectively, and to **b** the application of stepwise 3 V and 4 Hz consecutive sinusoidal voltage pulses. Parameter values are used as given in Table 2.1 with $\alpha_{ph} = 1e5$ in (a) and $\alpha_{ph} = 1e3$ in (b)

The first five positive voltage pulses correspond to the right half of the $i-v$ curve, where the memristance continually decreases. For the rest of the simulation the current is negative and the opposite trend is seen. Therefore, no matter which the initial condition is, the hysteretic $i-v$ loop is always pinched to the origin of the axes. So, the presented SPICE-compatible model complies adequately with the desired memristive fingerprints.

Another important issue, concerning the majority of existing modeling approaches being currently pursued by the design community, is that it is not always known how closely the SPICE models match the respective theoretical models on which they are based. The presented approach constitutes a highly parameterizable generalized model which has a direct correlation to the theoretical model that it was designed to match. Figure 2.7 indicates the $i-v$ hysteretic curves obtained both from the theoretical model implemented in MATLAB and from the corresponding SPICE implementation. The selected values for the set of adjustable parameters of the model, used to generate the simulation scenarios of Fig. 2.7, were taken equal in both cases to indicate compliance of the SPICE model with the theoretical model. Two simulation cases of a memristor under AC applied voltage of either low or high frequency, with symmetric or asymmetric thresholds, are shown. The simulation results are found in very good qualitative and quantitative agreement.

2.4 Model Verification

2.4.1 Fitting to a Reference Model

As it has been shown so far, the hysteretic $i-v$ curve obtained from simulation of a memristor under AC applied voltage using the proposed model, exhibits the expected

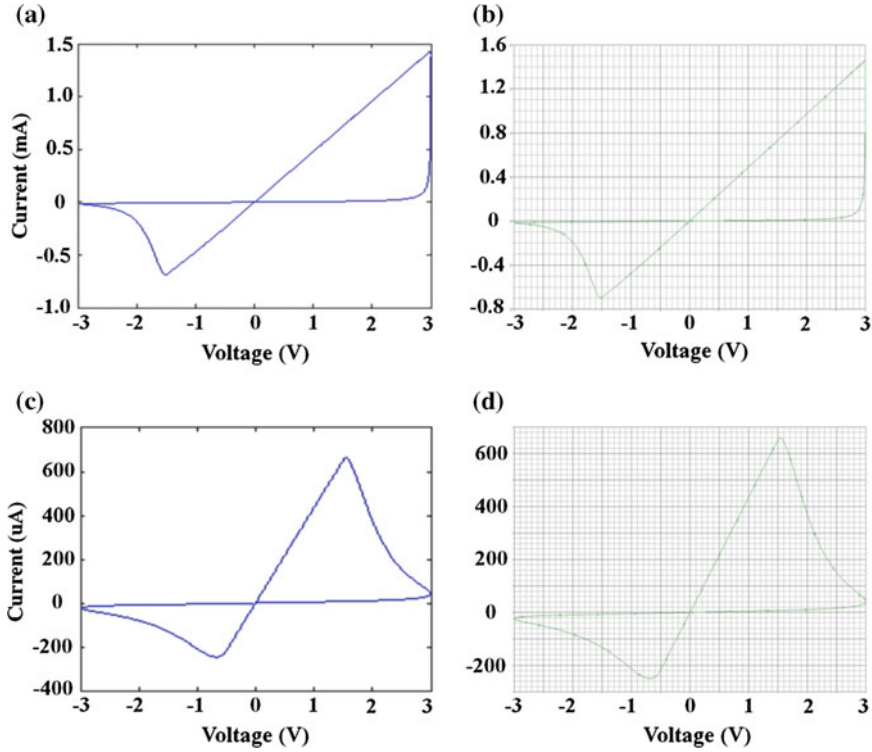


Fig. 2.7 SPICE implementation compliance with the theoretical model. **a, b** Comparison between **a** MATLAB and **b** SPICE implementations for the model parameters values as given in Table 2.1 with $\alpha = 1e3$ and signal frequency $f = 0.5$ Hz. **c, d** Comparison between **c** MATLAB and **d** SPICE implementations under different threshold voltages and frequency, with $\alpha = 1e6$ and $f = 1$ kHz

“bow tie” shape. In order to illustrate its versatility, in Fig. 2.8 we show the $i-v$ and $M-v$ (M -Memristance) characteristics calculated using the presented model and the model proposed in [10], which is used as a reference. The latter is a widely used extension of the linear ionic drift model proposed by HP [1], where a particular window function was incorporated to illustrate nonlinearities in ionic transport.

More specifically, the memristor is modeled as a thin oxide film of length D comprising a conductive layer of oxygen-deficient Titanium dioxide with length w (chosen as the state variable) serially connected with an insulating layer of stoichiometric Titanium dioxide of length $D-w$. The memristor input-output relation is modeled as:

$$v = M\left(\frac{w}{D}\right)i \quad (2.7)$$

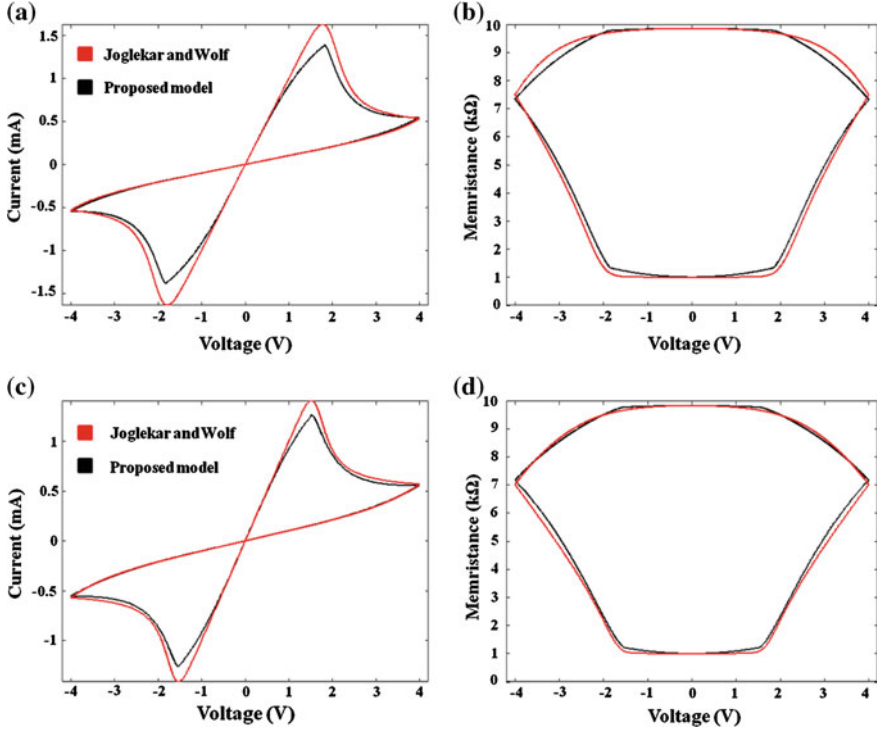


Fig. 2.8 Calculated i - v **a, c** and M - v **b, d** characteristics for memristors simulated using the presented model and the model of Joglekar and Wolf [10]. Our model successfully reproduces the characteristic responses of the selected reference model

where $M(\cdot)$ denotes the memristance function defined as:

$$M\left(\frac{w}{D}\right) = R_{OFF} - \Delta R \frac{w}{D} \quad (2.8)$$

where R_{ON} and R_{OFF} are the memristor boundary resistances when the whole nano-film is respectively enriched and depleted with oxygen vacancies, whereas $\Delta R = R_{OFF} - R_{ON}$. The equation governing the time evolution of the state is:

$$\frac{dw}{dt} = \mu \frac{R_{ON}}{D} f(w, i) i \quad (2.9)$$

where μ denotes the average mobility of the oxygen vacancies, whereas $f(w, i)$ is the window function which was introduced to take into account boundary behavior and various nonlinear dynamical effects such as nonlinear oxygen vacancy drift.

In [10] the window function $f(\cdot)$ takes values within $[0, 1]$, is independent of the current, and may assume its maximum unitary value when $w = \frac{1}{2} \times D$ according to

$$f(w, i) = f(w) = 1 - \left(\frac{2w}{D} - 1 \right)^{2p} \quad (2.10)$$

where p is a positive integer controlling the rate of decrease of the state variable as it approaches either of the boundaries.

In order to obtain a fairer comparison, wherever it applies we use the same parameters for both models. In specific, we use an 8 V peak-to-peak triangular AC voltage of period $T_1 = 2.6$ s and $T_2 = 5.5$ s to simulate memristors with total width $D_1 = L_{0,1} = 3$ nm and $D_2 = L_{0,2} = 5$ nm, respectively. We consider a $R_{\text{OFF}}/R_{\text{ON}}$ ratio of ≈ 10 , a dopant-mobility of 3×10^{-8} m²/(Vs) [29] and we set the exponent variable of the window function $p = 2$ [10]. Figure 2.8 summarizes the simulation results for both the first (a, b) and the second (c, d) memristor while fitting the presented model to the reference model. In each simulation scenario we set the parameters of our model $\{a_x, b, c, f_0, m, V_{\text{SET}} = |V_{\text{RESET}}|\}$ to the values $\{1000, 50, 0.1, 86.49, 56.06, 1.7 \text{ V}\}$ and $\{350, 20, 0.1, 2.67, 29.97, 1.5 \text{ V}\}$, respectively. In both cases our model delivers satisfying quantitative results which closely coincide with the results of the reference model. The small difference in the maximum observed currents is attributed to the slightly different moments when the maximum memristance is achieved, as particularly shown in Fig. 2.8b, d.

2.4.2 Testing in Complex Memristive Circuits

Up to this point we have thoroughly examined the dynamic behavior of the model when considering a single device under AC applied voltage. However, we have further studied the functionality of the model when simulating multiple memristive elements combined together. Using a single voltage-dependent current source between the memristor terminals (as shown in Fig. 2.4), which is a common practice also followed by other models in the literature (e.g. in [19]), might be problematic when trying to combine more than one memristors in complex resistive (ohmic) networks. As shown in Fig. 2.9a, when trying to connect two devices in the simplest in-series configuration, the resulting circuit branch contains two ideal current sources connected in series, which is not acceptable. In order to get over this shortcoming, we elaborated the presented model and replaced the single ideal current source with a real current source, i.e. a current source which has an additional parallel resistor. The value of the resistor must be high enough for the whole device to better approximate the ideal current source, affecting as less as possible the total current flowing through the memristor. During simulations this value is set to $1000 \times R_{\text{OFF}}$.

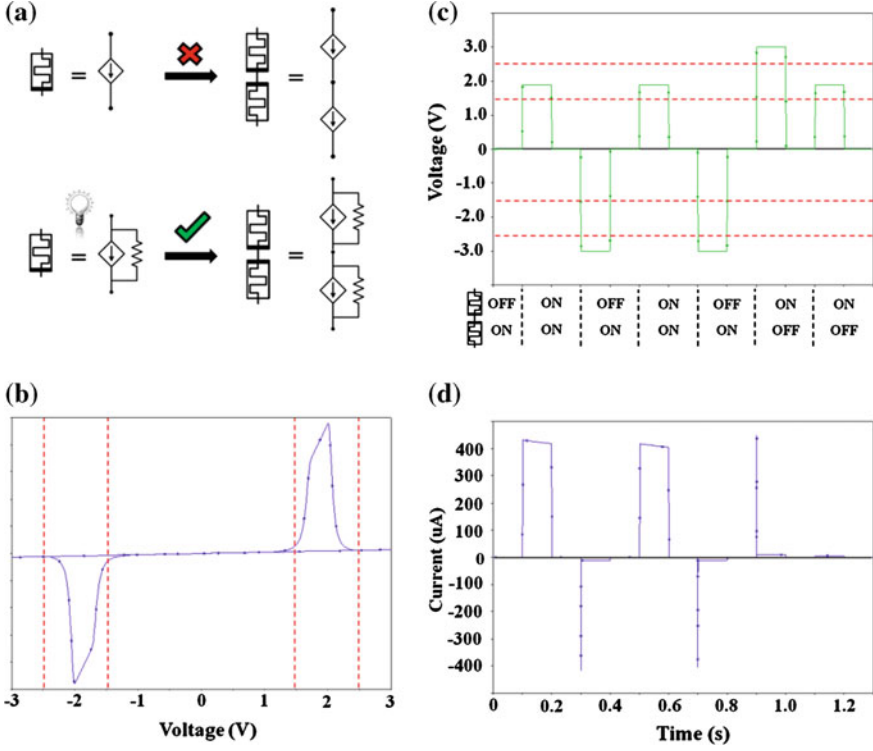


Fig. 2.9 SPICE simulation of a complementary resistive switch (CRS). **a** The model adjustment introduced to allow the in-series connection of memristors. **b** The CRS response to a 3 V and 100 kHz sinusoidal applied voltage. The red-dotted lines designate the area where the state-transitions take place. **c** The series of applied programming (± 3 V) and read-out (1.9 V) 100 ms duration voltage pulses. **d** The corresponding measured currents denoting the different resistive states of the CRS. In between **c** and **d** graphs there are the device transitions which take place every time a voltage pulse is applied. Values of the parameters of the model are the same as given in Table 2.1 with $\alpha = 1e7$ and threshold voltages $V_{SET} = |V_{RESET}| = 1$ V

We simulated a circuit branch comprising two memristors connected in-series with opposite polarities, forming a complementary resistive switch (CRS) [30]. In the CRS concept, a memory cell is formed by two bipolar memristive elements vertically stacked in an anti-serial manner. The unique aspect of this device combination is in using a series of R_{OFF} and R_{ON} states to represent a stored ‘0’ or a stored ‘1’. As an example, the memristance combinations $M_{UP}/M_{DOWN} = R_{ON}/R_{OFF}$ or R_{OFF}/R_{ON} are used to represent the aforementioned binary values. Figure 2.9b illustrates the i - v response of a simulated CRS, which comprises a forward-polarized memristor (FPM) and a reversely polarized memristor (RPM), after programming the individual devices into the state FPM/RPM = R_{OFF}/R_{ON} prior to further processing. Single memristors with opposite polarities demonstrate reversed behavior to the applied signals. During a single period of the applied AC

voltage, the complementary devices change their states in a reciprocal way, delivering this perfectly symmetric composite i - v curve.

Assuming the given initialization, a positive applied voltage creates the necessary conditions to first change the state of the FPM from R_{OFF} to R_{ON} and later that of the RPM from R_{ON} to R_{OFF} , resulting in a flipped resistive configuration. Next, the memristors exhibit an ohmic behavior until the voltage exceeds the respective negative thresholds and forces the memristors to successively switch to their initial states (first the RPM and then the FPM). In the resulting i - v characteristic, the current is linear with the voltage except in two finite voltage intervals.

In order to utilize a CRS as a memory cell, starting from Fig. 2.9b one has to select appropriate programming and reading voltages. The first must exceed the voltage limits where the state-transitions are completed, whereas the latter must lie within the region denoted by the red dotted lines, i.e. at a particular point where presence of high (low) current will determine reading a $R_{\text{OFF}}/R_{\text{ON}}$ ($R_{\text{ON}}/R_{\text{OFF}}$) state. In our simulations we program the device using ± 3 V pulses and read it using 1.9 V pulses. Figure 2.9c shows the series of applied voltage pulses and Fig. 2.9d includes the resulting measured currents, whereas in between the aforementioned graphs there are the state transitions happening each time a voltage pulse is applied. Whenever the less resistive combination occurs, i.e. the $R_{\text{ON}}/R_{\text{ON}}$, we observe an instant current peak which is characteristic of this transition.

Overall, the simulation results confirm the successful reproduction of the CRS operation with the presented graphs qualitatively matching the experimental results reported in [30]. Therefore we proved that the presented model can be readily used to simulate complex memristor-based circuits/networks.

2.5 Overview and Comparison

Using SPICE is common practice in all device level simulations and helps in the development of new circuit architectures applicable to novel emerging technologies. A variety of SPICE memristor models have been presented over the last few years and performing a fair comparison between them is definitely a rigorous task, given that the original papers often omit fundamental details and adjustments of secondary parameters.

Here we briefly comment on the most noteworthy, in our opinion, models of the literature, and we define a set of metrics while trying to characterize them. These metrics include: (i) the consideration of programming thresholds; (ii) the low complexity of the equations of the model; and (iii) the support for high working frequencies of the applied signals. The aforementioned selection is based on the fact that: (i) threshold-type switching is a common feature of experimental memristive devices; (ii) the desired memristor model should involve the lowest possible complexity capable of delivering efficient performance; and (iii) a versatile model should support a wide set of working frequencies to make possible the simulation of novel fabricated devices which present very fast switching times [31]. Table 2.2 presents

Table 2.2 Memristor SPICE model comparison

SPICE models	Programming thresholds	Support for high frequencies	Low complexity
[2]	■	■	
[5]	■	■	
[6]			■
[7]	■	■	
[8]	■	■	
[14]			■
[15]			■
[16]			■
[18]			■
[19]	■		
This work	■	■	■

■ Compliance with the property of the corresponding column

the summary of the comparison based on both our experience and on the material presented in the corresponding original works. From the ten selected SPICE models, only half of them permit threshold programming [2, 5, 7, 8, 19] whereas only four are capable of working under application of high-frequency signals [2, 5, 7, 8]. Possibly, these four could be the most accurate SPICE memristor models currently available, which explains the large number of equations and parameters that they include; hence none of these models involves low-complexity operation.

The presented generalized and versatile SPICE-compatible memristor model efficiently complies with all of the aforementioned metrics. It allows for multiple-threshold programming and has an unlimited set of working frequencies, whereas it is based on simple equations which guarantee low-complexity operation. In SPICE it is represented by a two-terminal sub-circuit, whose parameters can be setup at sub-circuit instantiation for each device. It can be easily parameterized to adequately match several types of memristive behavior and can be readily included in existing electronic circuit designs. All the simulation results presented throughout the rest of this book will be based on this model.

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