

Preface

When we started exploring the possibility of using Silicon Nanowire Transistors (SNT) for the next-generation VLSI technology, we were initially quite uncertain in its outcome. The early device simulations did not reveal superior device performance compared to FinFETs. Besides, there was an issue of channel doping. Even high concentrations of Arsenic (and Boron) were able to replace only several dopant atoms in the MOSFET body. This created a serious problem in three-dimensional device simulations. The sequence of failures and disappointing results motivated us to look at alternative device designs. We used intrinsic silicon for the body of the device and changed the gate material from conventional polysilicon to metal to be able to adjust the gate work function and the threshold voltage. This approach also helped to eliminate short channel effects of the transistor; however, it also made the device fabrication steps in simulations more difficult due to the metal gate. Previous annealing steps used after the gate deposition step could not be used once the metal gate was deposited. The heat management became a critical issue and required several changes in the fabrication in order to form the vertical gate structure.

It was not until we created the level 6 SPICE models for n- and p-channel SNTs and used them in basic digital gates, we could observe the real potential of SNTs in circuit performance and power consumption. Motivated primarily by the power consumption results, we subsequently replaced the level 6 models with the more accurate BSIMSOI models in the next phase of our research in designing analog and digital circuits.

The organization of chapters pretty much follows the progression of our five-year long research. Chapters 1 and 2 examine the device design and characteristics of SNTs with dual and single work-function metal gates. Each of these chapters studies and measures the circuit performance and power consumption of basic digital gates with extrinsic device parasitics. The layout area of each gate is also included in each chapter and compared with various digital gates built with FinFETs. Chapter 3 examines the BSIMSOI SPICE model and all the intrinsic and extrinsic parasitic components of SNTs. High-speed analog applications are

studied in Chapter 4 where SNTs are used in a single-stage amplifier, a differential pair, and a multi-stage operational amplifier. Chapter 5 examines the Radio Frequency (RF) applications. In this chapter, we presented the front end of an RF receiver and a Voltage-Controlled Amplifier (VGA). In Chapters 6 through 9, SNTs are used in various mega cells and complex digital systems. A complete Static Random Access Memory (SRAM) design and its layout are studied in Chapter 6. A Field-Programmable-Gate-Array (FPGA) architecture, circuit characteristics and layout in Chapter 7, an Integrate-and-Fire Spiking (IFS) neuron in Chapter 8, and a complete Direct Sequence Spread Spectrum (DSSS) baseband transmitter design in Chapter 9 are given to fully understand the implications of using SNTs in large-scale digital systems.

We firmly believe that SNTs are good candidates for the future of VLSI once the inherent complexities of device fabrication are overcome.

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