

## Chapter 2

# Thin-Film Transistors

**Abstract** Thin-film transistors (TFTs) are key elements for thin film electronics, being their most significant application the pixel switching elements on flat panel displays (FPDs). Semiconductor materials enabling faster TFTs, such as low-temperature polycrystalline silicon (LTPS) or transparent semiconducting oxides (TSOs), hold the promise of expanding TFT application to gate and data drivers or even full systems-on-panel, for increased reliability and lower production costs.

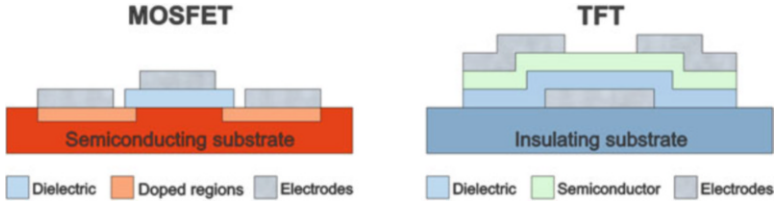
This chapter is an introductory background and a concise historical perspective related to TFTs. Additionally, taking into account that the devices explored in this work use an oxide semiconductor (indium-gallium-zinc oxide, IGZO) and an high- $\kappa$  dielectric (based on  $\text{Ta}_2\text{O}_5$  and  $\text{SiO}_2$ ), a brief overview and historical context regarding TSOs and high- $\kappa$  dielectrics is also provided.

### 2.1 TFTs Structure and Operation

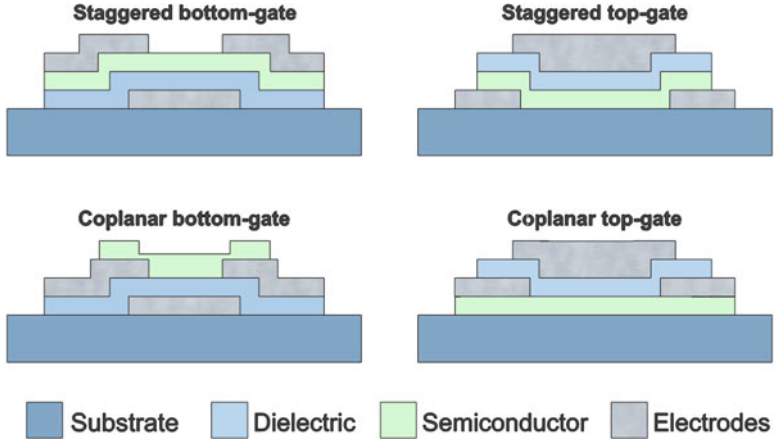
A TFT is a field-effect transistor (FET) comprising three terminals (gate, source, and drain) and including semiconductive, dielectric, and conductive layers. The semiconductor is placed between source/drain electrodes and the dielectric is located between the gate electrode and the semiconductor. The main idea in this device is to control the current between drain and source ( $I_{\text{DS}}$ ) by varying the potential between gate and source ( $V_{\text{GS}}$ ), inducing free charge accumulation at the dielectric/semiconductor interface [1].

TFTs can be seen as a class of FETs where main emphasis is on large area and low temperature processing, while metal oxide semiconductor field-effect transistors (MOSFETs) are essentially focused in high performance, at the cost of considerably larger processing temperature. As shown in Fig. 2.1, while in MOSFETs a silicon wafer is used, acting as substrate and semiconductor, TFTs use an insulator substrate, such as glass, that is not an active element for device operation. Furthermore, the operation mode is also different between MOSFETs and TFTs. While the former is based on inversion, the latter relies on accumulation.

Depending on the positioning of layers, four TFT structures are typically considered. They can either be staggered or coplanar (whether drain/source and gate are on opposite or on the same side regarding the semiconductor) and, inside



**Fig. 2.1** Comparison of typical structures of MOSFETs and TFTs

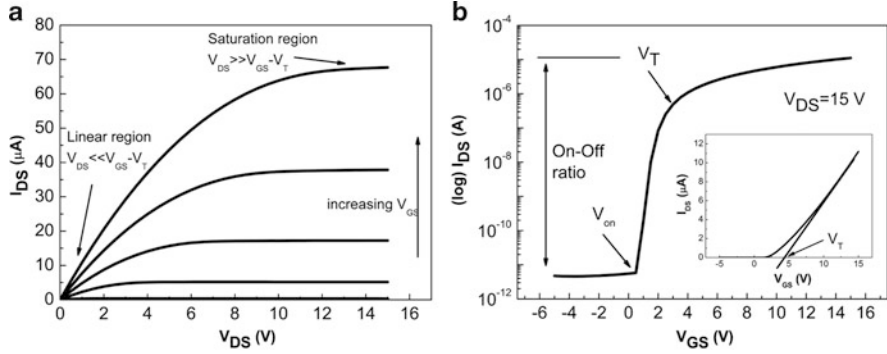


**Fig. 2.2** The most typical TFT structures depending on the positioning of layers

them, top or bottom gate (according to the location of gate) [2]. These structures are exhibited in Fig. 2.2. Very briefly, each one has advantages and drawbacks and in terms of fabrication the choice for one of these structures depends on the deposition processes and/or post-processing temperatures or number of lithographic masks involved. For instance, staggered bottom-gate structures are typically used when the dielectric layer requires high temperature, while coplanar top-gate ones are common for high temperature semiconductors, such as poly-Si.

Regarding operation and considering n-type TFTs, these can be designated by enhancement or depletion mode depending if threshold voltage ( $V_T$ ) is positive or negative. Enhancement mode is typically preferable because a gate voltage is not necessary to turn off the device (to achieve its *Off-state*) [3]. Still, depletion mode devices are also useful for circuit fabrication (e.g., as loads for nMOS logic circuitry).

When  $V_{GS} > V_T$ , a significant density of electrons is accumulated in dielectric/semiconductor interface and a large  $I_{DS}$  starts flowing, depending on the drain-to-source potential ( $V_{DS}$ ). This state is designated by *On-state* and involves two main regimes depending on the  $V_{DS}$  value:



**Fig. 2.3** Typical output (a) and transfer (b) curves for an n-type TFT

- if  $V_{DS} < V_{GS} - V_T$ , the TFT is in linear/triode mode and  $I_{DS}$  is described by:

$$I_{DS} = C_i \mu_{FE} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \quad (2.1)$$

where  $C_i$  is the gate capacitance per unit area,  $\mu_{FE}$  the field-effect mobility,  $W$  the channel width, and  $L$  the channel length of the device. For  $V_{DS} < V_{GS} - V_T$  the quadratic term is typically neglected.

- if  $V_{DS} > V_{GS} - V_T$ , the device is in saturation mode.  $I_{DS}$  is independent of  $V_{DS}$  and is described by:

$$I_{DS} = \frac{1}{2} C_i \mu_{sat} \frac{W}{L} (V_{GS} - V_T)^2, \quad (2.2)$$

where  $\mu_{sat}$  is the saturation mobility.

A typical characterization of TFTs involves static-current voltage measurements where output and transfer curves are obtained as shown in Fig. 2.3. While the output curve provides mostly a qualitative information regarding the effectiveness of channel pinch-off (hence saturation) and contact resistance, the transfer curve offers a more quantitative analysis where some electrical parameters can be determined:

- On-off ratio—This parameter is the ratio of the maximum to minimum  $I_{DS}$ . It is known that a higher “on” current offers better driving capability, while a lower “off” current results in low leakage current [2]. Consequently, a higher ratio is preferable;
- Threshold voltage ( $V_T$ )—Corresponds to the  $V_{GS}$  for which a significant charge is accumulated close to the dielectric/semiconductor interface. A possible methodology to determine this parameter is using a linear extrapolation of the  $I_{DS}$ - $V_{GS}$  at low  $V_{DS}$ ;
- Turn-on voltage ( $V_{on}$ )—Corresponds to the  $V_{GS}$  at which  $I_{DS}$  starts to increase. It is easily visible in the  $\log I_{DS}$ - $V_{GS}$  graph, as identified in Fig. 2.3b;

- Subthreshold swing (S)—this parameter indicates the  $V_{GS}$  required to increase  $I_{DS}$  by one decade, as seen in the subthreshold region. It is defined in V/decade:

$$S = \left( \frac{d \log(I_{DS})}{dV_{GS}} \Big|_{max} \right)^{-1} \quad (2.3)$$

A smaller S is preferable, resulting in lower power consumption and higher speed [2].

Regarding mobility ( $\mu$ ), it directly affects the maximum  $I_{DS}$  and the switching speed. There are different methodologies to determine  $\mu$ , most relevant are highlighted below:

- Effective mobility ( $\mu_{eff}$ )—It is considered as the most correct estimation of  $\mu$ , which includes the  $V_{GS}$  effect. It is determined by the conductance ( $g_{DS}$ ) at low  $V_{DS}$  and requires the previous determination of  $V_T$ :

$$\mu_{eff} = \frac{g_{DS}}{C_i \frac{W}{L} (V_{GS} - V_T)} \quad (2.4)$$

- Field-effect mobility ( $\mu_{FE}$ )—It is one of the most used methods to determine  $\mu$  in TFTs. It is obtained by the transconductance ( $g_m$ ) at low  $V_{DS}$ :

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_{DS}} \quad (2.5)$$

- Saturation mobility ( $\mu_{sat}$ )—The determination of this parameter is also common in TFTs and it describes a situation when the effective length is smaller than L [4]. As for  $\mu_{FE}$ , it is obtained by  $g_m$  but at high  $V_{DS}$ .

$$\mu_{sat} = \frac{\left( \frac{d\sqrt{I_{DS}}}{dV_{GS}} \right)^2}{\frac{1}{2} C_i \frac{W}{L}} \quad (2.6)$$

The mobility of the free carriers in the channel of device affects directly the maximum operating frequency or cut-off frequency ( $f_{co}$ ), a parameter extremely relevant to define the possible range of applications of a given TFT technology [4]. It can be defined by:

$$f_{co} = \frac{\mu V_{DS}}{2\pi L^2} \quad (2.7)$$

All these parameters are extremely relevant to evaluate the TFTs performance and understand if they can be integrated into more complex systems.

## 2.2 An Historical Perspective: From Conceptual Patents to Oxide TFTs

The twentieth century set the birth of electronics, bringing to world concepts as TFTs, integrated circuits (ICs), and complementary metal oxide semiconductor (CMOS) technology, which are of paramount importance nowadays.

The first works on TFTs were reported in 1930 when Lilienfeld described the basic principle, by means of a conceptual patent, of what is known today as metal semiconductor field-effect transistor (MESFET). Some years later, the author introduced the concept of what it nowadays called metal insulator semiconductor field-effect transistor (MISFET) [5]. In the next two decades, two discoveries set the pillars for the modern electronics world: the “Point contact transistor” in 1947 by Bardeen and Brattain and the junction field-effect transistor (JFET) proposed by Shockley in 1952. These were the first transistors that were actually fabricated, showing the switching capability of such devices and how they could be advantageous over the conventional tubes.

In the 60s the first TFT was demonstrated and high speed transistors, the MOSFETs, also emerged in this decade. In 1979 hydrogenated amorphous silicon (a-Si:H) was introduced as a semiconductor on TFTs. Despite its low mobility when compared with the (poly) crystalline materials being studied in that period, the amorphous structure allowed for large area fabrication, which together with the good switching capability of this technology was of great importance in defining a-Si:H TFTs as the main choice for the fabrication of active matrix liquid crystal displays (AMLCDs). Pursuing greater mobility devices, in the 80s, TFTs based on poly-Si were introduced, allowing for high performance circuit fabrication. However, poly-Si TFTs required high temperature processes and had high fabrication cost. Hence, in the 90s, LTPS at around 550 °C was suggested, but processing in large area was still not trivial. Organic TFTs also appeared in this decade with a fantastic advantage, low processing temperature, although their lack of stability and performance still remains an issue these days [5]. Hence, for the new millennium, there was still space for a new technology, combining large area uniformity, low processing temperatures, and good electrical performance. The answer to this emerged in the form of oxide TFTs, which besides these properties also offer the possibility of full transparency.

## 2.3 Oxide TFTs: Materials, Processes, and Comparison with Other Semiconductor Technologies

Transparent conducting oxides (TCOs) and TSOs, whose studies are reported to the beginning of the twentieth century, are key materials of transparent electronics, exhibiting optical transparency and tunable conductivities between those of conductors and semiconductors [4]. The idea behind them, is to have intrinsic

(structural defects) or extrinsic (substitutional elements) doping during and/or after film deposition. For instance, by varying stoichiometry, it is possible to obtain different free carrier concentrations normally in the  $10^{21} \text{ cm}^{-3}$  range for TCO and from  $10^{14}$  to  $10^{18} \text{ cm}^{-3}$  for TSO [4, 6, 7].

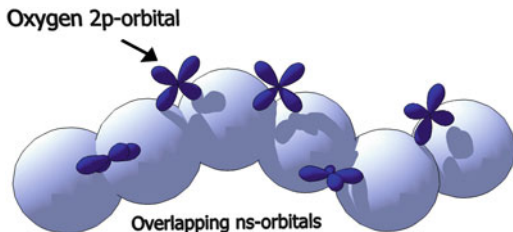
The first work using a TSO (in this case  $\text{SnO}_2$ ) as channel layer in a TFT appeared in the 60s. In the same decade, a work based on ZnO was suggested but with a small  $I_{\text{DS}}$  modulation by  $V_{\text{GS}}$  and no  $I_{\text{DS}}$  saturation was observed [8].

More recently, in the early 2000s, research groups proposed fully transparent ZnO TFTs, produced at  $450\text{--}600^\circ\text{C}$ , exhibiting a reasonable performance [3, 9, 10]. After that, it was shown that ZnO could be even sputtered at room temperature without degrading electrical properties of TFTs [11, 12].

In parallel with the “big-boom” of reports on binary compounds as ZnO for TFTs, an initial work by Nomura and co-workers on single crystalline IGZO started an era of incredible success for oxide semiconductors. This multicomponent material produced at  $1400^\circ\text{C}$  exhibited a high  $\mu_{\text{FE}}$  of  $80 \text{ cm}^2/\text{V s}$  when integrated in a TFT structure [13]. However, the more striking aspect was revealed in 2004, when an IGZO layer was fabricated by the same group at room temperature, resulting in an amorphous structure and a TFT with  $\mu_{\text{sat}} \approx 10 \text{ cm}^2/\text{V s}$  [14].

What is striking in this a-IGZO and others amorphous TSOs is that they exhibit high  $\mu$ , not dramatically different from their corresponding single crystals, which is not the case in conventional covalent semiconductors (e.g., a-Si:H typically has  $\mu < 1 \text{ cm}^2/\text{V s}$  against  $>1000 \text{ cm}^2/\text{V s}$  of Si single crystals). In these ionic materials, the conduction band is made by spherical isotropic  $ns$  orbitals of the metallic cations (Fig. 2.4). Hence, if the radii of these orbitals are larger than the distance between cations (verified for  $n > 4$ ), a “continuous path” can be created, improving carrier transport and, consequently,  $\mu$  [14, 15]. During the last years different combinations of cations have been studied, going from oxides including indium, such as IGZO, indium-zinc oxide (IZO), or indium-molybdenum oxide (IMO) [16–21], generally allowing for high  $\mu_{\text{FE}}$  at lower processing temperatures, to more sustainable approaches (regarding the use of non-critical raw materials) such as zinc-tin oxide (ZTO) [15]. All of them share reasonably high  $\mu$  (increased with In), low temperature processing, for most of them compatible with low cost flexible substrates, and an amorphous structure that is a great advantage when large area processing is envisaged, as it assures the best possible uniformity.

**Fig. 2.4** Schematic for the carries transport path for amorphous oxide semiconductors, proposed by Nomura et al. [14]

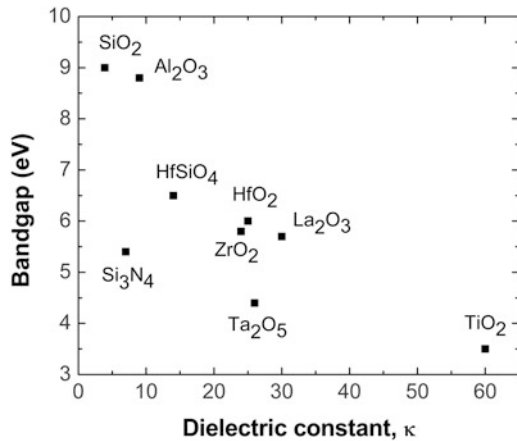


## 2.4 High- $\kappa$ Dielectrics for Oxide TFTs

Proper choice of a dielectric material is crucial to define the performance/stability of any TFT technology. Alternative dielectrics to  $\text{SiO}_2$  have been studied, mainly high- $\kappa$  as  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , and  $\text{Ta}_2\text{O}_5$ . The main advantage of high- $\kappa$  dielectrics is the possibility to maintain the capacitance per unit area of  $\text{SiO}_2$  but with thicker films. This is highly relevant not only for scaling down transistor sizes in c-Si MOSFETs, but also when low temperature technologies, such as oxide TFTs are considered. The importance of this is explained as follows: semiconductor films deposited by lower temperature processes are more prone to have higher densities of defects and reduced compactness, which can be compensated by the larger capacitive injection of high- $\kappa$  dielectrics. On the other hand, insulators with good capacitance per unit area can still be achieved even if their thickness is increased, compensating the degraded insulating properties of dielectrics fabricated at lower temperatures. The combination of these factors enables low temperature TFTs with low operating voltage, steep subthreshold regions, and large  $\mu$ , without neglecting the fundamental role of the dielectric as electrical insulator between gate and semiconductor.

High- $\kappa$  dielectrics typically exhibit a lower bandgap energy,  $E_G$ , than the more conventional  $\text{SiO}_2$  (Fig. 2.5), which can be problematic in terms of gate leakage current ( $I_G$ )—direct tunnelling across dielectric layer, by Schottky emission or Poole-Frenkel effect [22]. Additionally, one has to consider the large  $E_G$  of oxide semiconductors when compared to other semiconductor technologies, which turns the high- $\kappa$  choice for oxide TFTs narrower. Regarding material selection, one still has to consider that the band offset between semiconductor and dielectric should be at least 1 eV. For an n-type device this corresponds to the difference between the minimum of conduction bands of semiconductor and dielectric, while for a p-type device the offset should be analyzed in terms of the maximum of valence bands of both materials [23]. In this way, not all combinations of

**Fig. 2.5** Relation between bandgap and  $\kappa$  for the most relevant inorganic dielectrics



semiconductors and dielectrics are desirable. Regarding material structure, amorphous layers are preferable due to the better uniformity in large areas, smoother dielectric/semiconductor interface and suppression of grain boundaries that act as preferential paths for carriers' flow [24].

Nonetheless and despite the integration of these dielectrics in TFTs is highly promising to improve their performance, a trade-off between  $\kappa$  and breakdown field ( $E_B$ ) needs to be done [25]. Instability, off-current and hysteresis are seen as a problem, which can be solved using different configurations such as multilayers, or even multicomponent dielectrics, combining high  $E_G$  materials as  $\text{SiO}_2$ , which enables low  $I_G$ , high  $E_B$ , and good interface properties with most semiconductor technologies, with high- $\kappa$  ones as  $\text{Ta}_2\text{O}_5$ ,  $\text{HfO}_2$ , or even  $\text{Al}_2\text{O}_3$ , which assure a high capacitance to the overall structure [26–29]. It should also be noted that, as verified with oxide semiconductors, multicomponent dielectrics also potentiate increased structural disorder, hence amorphous structures.

## 2.5 Current Research Trends in Oxide TFTs

Despite the lack of maturity compared to the dominant TFT technology (i.e., a-Si:H), oxide TFTs are starting to assume a preponderant role in the display industry, with more and more announces of commercially available products integrating this technology, ranging from large area 4k OLED TVs to smartphones. Still, much more progress will certainly be done in the next years on oxide TFTs that will enable an ever more relevant presence in different markets, ranging from fully transparent displays to disposable products. The following paragraphs briefly summarize some of the current research trends in the area.

Research groups are studying new approaches in order to optimize processes, enhance TFT performance and reduce the involved costs. In line with this, there is a constant search for alternative and sustainable oxide semiconductors and dielectrics, both in terms of composing materials (eventually even hybrid inorganic/organic) and structures (where nanostructures as nanowires and nanoparticles are deserving increased attention for ultimate performance levels) [30]. Another important topic is the migration of vacuum processing to simpler solution processing, such as spin-coating or inkjet printing. Although the initial works on solution processed oxide TFTs were based on high temperature processes and yielded low performance [31–33], nowadays there are quite interesting reports on these devices processed at temperatures as low as 200 °C, reaching similar characteristics to their physically processed counterparts [34–36].

In terms of p-type oxide TFTs, required for CMOS architectures using oxide technology, materials as tin and copper oxide have been produced at room temperature and annealed at temperatures as low as 200 °C. However the device performance is far from the one achieved with n-type oxide TFTs [37–39].



As most of these oxide materials can be processed at very low temperatures, and given the great environmental concerns these days, research groups are considering new approaches such as introducing paper in electronics, envisaging a recyclable electronics concept. Flexible substrates and low power circuits have also been considered [24, 40].

Finally, demonstrations of increasingly more complex systems are required to show the potential of this new technology. The ADC presented in this work represents a significant step towards this end, being one of the most complex circuit implementations with oxide TFTs reported so far.

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A Second-Order  $\Sigma\Delta$  ADC Using Sputtered IGZO TFTs  
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