

# Preface to the Fourth Edition

Novel market segments such as intelligent transportation, revolutionary health care, sophisticated security systems, and smart energy have recently emerged, requiring increasingly diverse functionality such as RF circuits, power control, passive components, sensors/actuators, biochips, optical communication, and microelectromechanical devices. Integration of these non-digital functionalities at the board-level into system platforms such as systems-in-package (SiP), systems-on-chip (SoC), and three-dimensional (3-D) systems is a primary near- and long-term challenge of the semiconductor industry. The delivery and management of high-quality, highly efficient power have become primary design issues in these functionally diverse systems. Integrated in-package and distributed on-chip power delivery is currently under development across a broad spectrum of applications; the power delivery design process, however, is currently dominated by ad hoc approaches.

The lack of methodologies, architectures, and circuits for scalable on-chip power delivery and management is at the forefront of current heterogeneous system design issues. The objective of this book is to describe the many short- and long-term challenges of high-performance power delivery systems, provide insight and intuition into the behavior and design of next-generation power delivery systems, and suggest design solutions while providing a framework for addressing power objectives at the architectural, methodology, and circuit levels.

This book is based on the body of research carried out by the authors of previous editions of this book from 2001 to 2011. The first edition of the book, titled *Power Distribution Networks in High Speed Integrated Circuits*, was published in 2004 by Andrey V. Mezhiba and Eby G. Friedman. This first book focused on on-chip distribution networks, including electrical characteristics, relevant impedance phenomenon, and related design trade-offs. On-chip distributed power delivery, at that time an innovative paradigm shift in power delivery, was also introduced in the book. As the concept of integrated power delivery evolved, the important topic of on-chip decoupling capacitance was added to the book, which was released in 2008 with a new title, *Power Distribution Networks with On-Chip Decoupling Capacitors* by Mikhail Popovich, Andrey V. Mezhiba, and Eby G. Friedman. Later, this book was revised by Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba,

Selçuk Köse, and Eby G. Friedman to address emerging design and analysis challenges in on-chip power networks. This last edition was published with an identical title in 2011. Since the first book was published in 2004, the issue of power delivery has greatly evolved. The concept of on-chip distributed power delivery has been recognized as an important cornerstone to high-performance integrated circuits. A number of ultrasmall on-chip power supplies to support this on-chip focus have also been demonstrated.

While on-chip power integration has become a primary objective for system integration, research has remained focused on developing compact and efficient power supplies, lacking a methodology to effectively integrate and manage in-package and on-chip power delivery systems. The challenge has become greater as the diversity of modern systems increases, and dynamic voltage scaling (DVS) and dynamic voltage and frequency scaling (DVFS) become a part of the power management process. Hundreds of on-chip power domains with tens of different voltage levels have recently been reported, and thousand-core ICs are being considered. Scalable power delivery systems and the granularity of power management in DVS/DVFS multicore systems are limited by existing ad hoc approaches. To cope with this increasing design complexity and the quality and system-wide efficiency challenges of next-generation power delivery systems, enhanced methodologies to design and analyze scalable, hierarchical power management and delivery systems with fine granularity of dynamically controllable voltage levels are necessary. Updating the vision of on-chip power delivery networks, traditionally viewed as a passive network, is the primary purpose for publishing a new (fourth) edition of this book. Emphasis is placed on complex and scalable power delivery systems, system-wide efficiency, quality of power, and intelligent, real-time, fine-grain local power management. A framework that addresses various power objectives at the architectural, methodology, and circuit levels is described, providing a general solution for existing and emerging power delivery challenges and techniques. This book, titled *On-Chip Power Delivery and Management*, is authored by Inna P.-Vaisband, Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhibi, Selçuk Köse, and Eby G. Friedman as the fourth edition of this series of books.

The chapters of the book are now separated into eight parts. Power networks, inductive properties, electromigration, and decoupling capacitance within integrated circuits are described in Part I (Chaps. 1, 2, 3, 4, 5, and 6). In Part II (Chaps. 7, 8, 9, and 10), the design of on-chip power distribution networks and power supplies is discussed. Circuits for on-chip power delivery and management and integrated power delivery systems are described in Part IV (Chaps. 17, 18, 19, and 20). Closed-form expressions for power grid analysis, modeling and optimization of power networks, and the codesign of power supplies are presented in Part V (Chaps. 21, 22, 23, 24, 25, 26, and 27). Since noise within the power grid is a primary design constraint, this issue is reviewed in Part VI (Chaps. 28, 29, 30, 31, 32, 33, and 34). Multilayer power distribution networks are the focus of Part VII (Chaps. 35, 36, 37, 38, and 39). In Part III (Chaps. 12, 13, 14, and 15), the issue of placing on-chip decoupling capacitors is discussed. In Part VIII (Chaps. 40, 41, 42, and 43), multiple power supply systems are described. The focus of this part is on those integrated

circuits where multiple on-chip power supplies are required. In Part IX, some concluding comments, the appendices, and additional information are provided.

This revised and updated material is based on recent research by Inna P.-Vaisband developed between 2009 and 2015 at the University of Rochester during her doctoral studies under the supervision of Prof. Eby G. Friedman. The new chapters focus on design complexity, system scalability, and system-wide optimization of power delivery and management systems. The concept of intelligent power delivery is introduced, and a framework for on-chip power delivery and management is described that provides local power control and real-time management for sharing energy resources.

The book covers a wide spectrum of issues related to on-chip power networks and systems. The authors believe that this revised edition provides the latest information on a dynamic and highly significant topic of primary importance to both the industrial and academic research and development communities.

## Acknowledgments

The authors would like to thank Chuck Glaser for his sincere encouragement and enthusiastic support of the publication of this book. The authors would also like to thank Burt Price and Jeff Fischer from Qualcomm and Avinoam Kolodny from Technion – Israel Institute of Technology for their collaboration and support.

The research described in this book has been supported in part by the Binational Science Foundation under grant no. 2012139; the National Science Foundation under grant nos. CCF-1329374, CCF-1526466, and CNS-1548078; the IARPA under grant no. W911NF-14-C-0089 and by grants from Qualcomm, Cisco Systems, and Intel.

Rochester, USA  
San Diego, USA  
San Diego, USA  
Hillsboro, USA  
Tampa, USA  
Rochester, USA  
December 2015

Inna P.-Vaisband  
Renatas Jakushokas  
Mikhail Popovich  
Andrey V. Mezhiba  
Selçuk Köse  
Eby G. Friedman

<http://www.springer.com/978-3-319-29393-6>

On-Chip Power Delivery and Management

Vaisband, I.P.; Jakushokas, R.; Popovich, M.; Mezhiba,  
A.V.; Köse, S.; Friedman, E.G.

2016, XXXVII, 742 p. 426 illus., 89 illus. in color.,

Hardcover

ISBN: 978-3-319-29393-6