

# Preface

Nowadays computer systems are applied in safety critical areas such as military, aviation, intensive health care, industrial control, space exploration, etc. All these areas demand the highest possible reliability of functional operation. However, ionized particles and radiation, thermal instability, and various external factors—all impact on current semiconductor hardware and this leads inevitably to faults in the system. It is expected that such phenomena will be observed more often in the future because of the ongoing miniaturization of hardware structures.

In this book, we want to tackle the question of how system software should be designed to support, handle, and recover hardware in the event of such faults, and which fault tolerance schemes system software should provide for the highest reliability. We also show how the system software interacts with the hardware to tolerate these faults.

First, we analyze and further develop the theory of fault tolerance to understand the ways to increase the reliability of a system. Ultimately, the key is to use redundancy in all its different appearances. We revise and further develop the general algorithm of fault tolerance (GAFT) with its three main processes of hardware checking, preparation for recovery and recovery procedure, and explain how our approach to the design of fault-tolerant system fits this sequence. For each of the three processes, we analyze the requirements and properties theoretically and give possible implementation scenarios.

Based on the theoretical results, we derive an Oberon-based programming language with direct support of the three processes of GAFT making fault tolerance supported at language level, run-time system level and even at user level.

In the last part of this book, we analyze a simulator-based proof of concept implementation of an evolving reliable reduced instruction computer (ERRIC) and its newly developed run-time system in terms of reconfigurability and performance.

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