

Contents

1	Introduction	1
1.1	Microfluidic Biochips	1
1.2	mVLSI Technology	3
1.2.1	Application Areas	4
1.2.2	Motivation for Automated Physical Design and Testing Techniques	6
1.2.3	Motivation for Programming and Control of mVLSI Biochips	8
1.3	Overview	8
	References	10
 Part I Preliminaries		
2	Design Methodology for Flow-Based Microfluidic Biochips	15
2.1	Modeling and Simulation	17
2.2	Physical Design and Testing	20
2.3	Programming and Control	23
	References	25
3	Biochip Architecture Model	29
3.1	Microfluidic Valve	29
3.2	Component Design	31
3.2.1	Pneumatic Switches	31
3.2.2	Pneumatic Mixer	31
3.3	Illustrative Example	33
3.4	Component Model and Library	35
3.4.1	Component Model	35
3.4.2	Component Model Library	36
3.5	System-Level Architecture Model	36

3.6	On-Chip Control	40
3.6.1	Pneumatic Logical Components	44
3.6.2	Supportive Components	48
3.6.3	Logical Circuits	50
3.6.4	Logic Truth Tables	51
	References	51
4	Biochemical Application Modeling	53
4.1	High-Level Protocol Language: Aqua	53
4.1.1	Declarations	54
4.1.2	Statements	56
4.2	Biochemical Application Model	57
4.3	Benchmarks	59
4.3.1	Real-Life Benchmarks	60
4.3.2	Synthetic Benchmarks	62
	References	64
 Part II Compilation		
5	Compiling High-Level Languages	67
5.1	Problem Formulation	67
5.2	Application Model Synthesis	68
5.2.1	High-Level Language Grammar	70
5.2.2	Generating the Application Graph	73
5.3	Solving the Mixing Problem	80
	References	91
6	Application Mapping and Simulation	93
6.1	Application Mapping	94
6.1.1	Problem Formulation	96
6.2	Constraint Programming Strategy	96
6.2.1	Finite Domain Variables	97
6.2.2	Resource Binding Constraints	98
6.2.3	Resource Sharing Constraints	98
6.2.4	Precedence Constraints	99
6.2.5	Cost Function	99
6.3	List Scheduling Strategy	99
6.3.1	Route Generation	102
6.3.2	Optimization	103
6.4	Experimental Evaluation	103
6.5	Simulation	106
	References	109

7	Control Synthesis and Pin-Count Minimization	111
7.1	Biochip Control Synthesis	113
7.1.1	Control Logic Generation	116
7.1.2	Pin-Count Minimization	117
7.1.3	Problem Formulation	119
7.2	Synthesis Strategy	119
7.2.1	Control Logic Generation	119
7.2.2	Pin-Count Minimization	120
7.3	Experimental Evaluation	122
	References	124

Part III Physical Design

8	Allocation and Schematic Design	127
8.1	Problem Formulation	128
8.2	Allocation and Schematic Design	129
8.2.1	Allocation and Schematic Design	129
8.3	Synthesis Strategy	131
8.3.1	Allocation	131
8.3.2	Schematic Design	134
8.4	Experimental Evaluation	136
	References	144
9	Placement and Routing	145
9.1	Models, Component Library, and Design Rules	146
9.1.1	Connection Model	148
9.1.2	Grid Graph Model	148
9.1.3	Route Model	150
9.2	Problem Formulation	151
9.2.1	Formalization	152
9.3	Simulated Annealing	152
9.3.1	Concept	152
9.3.2	Implementation	153
9.4	Approximated Cost Function	157
9.4.1	Metrics	158
9.4.2	Computing the Cost Function	160
9.5	Routed Cost Function	162
9.5.1	Routing Algorithms	162
9.5.2	Metrics	166
9.5.3	Computing the Cost Function	169
9.6	Experimental Evaluation	175
9.6.1	Benchmarks	176
9.6.2	Placement Quality	176
9.6.3	Performance	180
	References	182

10 On-Chip Control Synthesis	183
10.1 Circuit Design	185
10.1.1 Ongoing Example	186
10.1.2 Two-Level Minimization	187
10.1.3 Multiple-Level Optimization	193
10.1.4 Library Binding	197
10.2 Control Synthesis	204
10.2.1 Component Control Logic Generation	204
10.2.2 Routing Control Logic Generation	206
10.3 Physical Synthesis	209
10.3.1 Placement	211
10.3.2 Routing	215
10.4 Evaluation	227
10.5 Benchmarks	228
10.5.1 Evaluation of the Circuit Design	229
10.5.2 Evaluation of the Placement Step	231
10.5.3 Evaluation of the Routing Step	232
10.6 On-Chip and Off-Chip Trade-Off	233
10.7 On-Chip Control Circuits	238
References	238
11 Testing and Fault-Tolerant Design	241
11.1 Fault Model and Testing	242
11.1.1 Fault Model	242
11.1.2 Testing	246
11.1.3 Fault-Tolerant Architecture Synthesis	246
11.1.4 Design Transformations	250
11.1.5 Simulated Annealing	251
11.1.6 GRASP	254
11.1.7 Architecture Evaluation	258
11.2 Experimental Evaluation	263
References	267
Index	269

Microfluidic Very Large Scale Integration (VLSI)
Modeling, Simulation, Testing, Compilation and Physical
Synthesis

Pop, P.; Minhass, W.H.; Madsen, J.

2016, XV, 270 p. 148 illus., 101 illus. in color.,

Hardcover

ISBN: 978-3-319-29597-8