

Contents

Invited Talks

The VINEYARD Approach: Versatile, Integrated, Accelerator-Based, Heterogeneous Data Centres	3
<i>Christoforos Kachris, Dimitrios Soudris, Georgi Gaydadjiev, Huy-Nam Nguyen, Dimitrios S. Nikolopoulos, Angelos Bilas, Neil Morgan, Christos Strydis, Christos Tsalidis, John Balafas, Ricardo Jimenez-Peris, and Alexandre Almeida</i>	
A Design Methodology for the Next Generation Real-Time Vision Processors	14
<i>Jones Yudi Mori, André Werner, Arij Shallufa, Florian Fricke, and Michael Hübner</i>	
EEG Feature Extraction Accelerator Enabling Long Term Epilepsy Monitoring Based on Ultra Low Power WSNs	26
<i>Evangelinos Mariatos, Christos P. Antonopoulos, and Nikolaos S. Voros</i>	

Video and Image Processing

Computing to the Limit with Heterogeneous CPU-FPGA Devices in a Video Fusion Application.	41
<i>Jose Nunez-Yanez</i>	
An Efficient Hardware Architecture for Block Based Image Processing Algorithms	54
<i>Tomasz Kryjak, Marek Gorgon, and Mateusz Komorkiewicz</i>	
An FPGA Stereo Matching Processor Based on the Sum of Hamming Distances	66
<i>Abiel Aguilar-González and Miguel Arias-Estrada</i>	
FPGA Soft-Core Processors, Compiler and Hardware Optimizations Validated Using HOG	78
<i>Colm Kelly, Fahad Manzoor Siddiqui, Burak Bardak, Yun Wu, Roger Woods, and Karren Rafferty</i>	
A Comparison of Machine Learning Classifiers for FPGA Implementation of HOG-Based Human Detection	91
<i>Masahito Oishi, Yoshiki Hayashida, Ryo Fujita, Yuichiro Shibata, and Kiyoshi Oguri</i>	

A Scalable Dataflow Accelerator for Real Time Onboard Hyperspectral Image Classification	105
<i>Shaojun Wang, Xinyu Niu, Ning Ma, Wayne Luk, Philip Leong, and Yu Peng</i>	

Fault-Tolerant Systems

A Redundant Design Approach with Diversity of FPGA Resource Mapping . . .	119
<i>Yudai Shirakura, Taisei Segawa, Yuichiro Shibata, Kenichi Morimoto, Masaharu Tanaka, Masanori Nobe, Hidenori Maruta, and Fujio Kurokawa</i>	
Method to Analyze the Susceptibility of HLS Designs in SRAM-Based FPGAs Under Soft Errors	132
<i>Jorge Tonfat, Lucas Tambara, André Santos, and Fernanda Kastensmidt</i>	
Low Cost Dynamic Scrubbing for Real-Time Systems.	144
<i>Leonardo P. Santos, Gabriel L. Nazar, and Luigi Carro</i>	

Tools and Architectures

Analytical Delay Model for CPU-FPGA Data Paths in Programmable System-on-Chip FPGA	159
<i>Mohammad Tahghighi, Sharad Sinha, and Wei Zhang</i>	
New Partitioning Approach for Hardware Trojan Detection Using Side-Channel Measurements	171
<i>Karim M. Abdellatif, Christian Cornesse, Jacques Fournier, and Bruno Robisson</i>	
A Comprehensive Set of Schemes for PUF Response Generation	183
<i>Bilal Habib and Kris Gaj</i>	
Design and Optimization of Digital Circuits by Artificial Evolution Using Hybrid Multi Chromosome Cartesian Genetic Programming	195
<i>Vitor Coimbra and Marcus Vinicius Lamar</i>	
A Multi-codec Framework to Enhance Data Channels in FPGA Streaming Systems	207
<i>Marlon Wijeyasinghe and David Thomas</i>	

Signal Processing

Reconfigurable FPGA-Based FFT Processor for Cognitive Radio Applications	223
<i>Mário Lopes Ferreira, Amin Barahimi, and João Canas Ferreira</i>	

Real-Time Audio Group Delay Correction with FFT Convolution on FPGA . . .	233
<i>Arthur Spierer and Andres Upegui</i>	

Comparing Register-Transfer-, C-, and System-Level Implementations of an Image Enhancement Algorithm.	245
<i>Markus Weinhardt</i>	

Multicore Systems

Evaluating Schedulers in a Reconfigurable Multicore Heterogeneous System	261
<i>Jeckson Dellagostin Souza, João Victor Gomes Cachola, Luigi Carro, Mateus Beck Rutzig, and Antonio Carlos Schneider Beck</i>	

Programmable Logic as Device Virtualization Layer in Heterogeneous Multicore Architectures	273
<i>Falco K. Bapp, Oliver Sander, Timo Sandmann, Hannes Stoll, and Jürgen Becker</i>	

Zynq Cluster for CFD Parametric Survey.	287
<i>Naru Sugimoto, Takaaki Miyajima, Ryotaro Sakai, Yasunori Osana, Naoyuki Fujita, and Hideharu Amano</i>	

Invited Paper on Funded RD Running and Completed Projects Posters

Fast and Resource Aware Image Processing Operators Utilizing Highly Configurable IP Blocks	303
<i>Konrad Häublein, Christian Hartmann, Marc Reichenbach, and Dietmar Fey</i>	

Performance Evaluation of Feed-Forward Backpropagation Neural Network for Classification on a Reconfigurable Hardware Architecture.	312
<i>Mahnaz Mohammadi, Rohit Ronge, Sanjay S. Singapuram, and S.K. Nandy</i>	

FPGA-Based Acceleration of Pattern Matching in YARA	320
<i>Shreyas G. Singapura, Yi-Hua E. Yang, Anand Panangadan, Tamas Nemeth, Peter Ng, and Viktor K. Prasanna</i>	

Efficient Camera Input System and Memory Partition for a Vision Soft-Processor.	328
<i>Jones Yudi Mori, Frederik Kautz, and Michael Hübner</i>	

A Lost Cycles Analysis for Performance Prediction using High-Level Synthesis	334
<i>Bruno da Silva, Jan Lemeire, An Braeken, and Abdellah Touhafi</i>	

A Dynamic Cache Architecture for Efficient Memory Resource Allocation in Many-Core Systems.	343
<i>Carsten Tradowsky, Enrique Cordero, Christoph Orsinger, Malte Vesper, and Jürgen Becker</i>	
Adaptive Bandwidth Router for 3D Network-on-Chips	352
<i>Stephanie Friederich, Niclas Lehmann, and Jürgen Becker</i>	
Reduced-Precision Algorithm-Based Fault Tolerance for FPGA-Implemented Accelerators	361
<i>James J. Davis and Peter Y.K. Cheung</i>	
Author Index	369

Applied Reconfigurable Computing

12th International Symposium, ARC 2016 Mangaratiba,

RJ, Brazil, March 22-24, 2016 Proceedings

Bonato, V.; Bouganis, C.; Gorgon, M. (Eds.)

2016, XIV, 370 p. 195 illus. in color., Softcover

ISBN: 978-3-319-30480-9