Preface

Reconfigurable computing technologies offer the promise of substantial performance gains over traditional architectures via customizing, even at runtime, the topology of the underlying architecture to match the specific needs of a given application. Contemporary configurable architectures allow for the definition of architectures with functional and storage units that match in function, bit-width, and control structures the specific needs of a given computation. The flexibility enabled by reconfiguration is also seen as a basic technique for overcoming transient failures in emerging device structures. The growth of the capacity of reconfigurable devices, such as FPGAs, has created a wealth of new research opportunities and intricate engineering challenges. Within the past decade, reconfigurable architectures have evolved from a uniform sea of programmable logic elements to fully reconfigurable systems-on-chip with integrated multipliers, memory elements, processors, and standard I/O interfaces. One of the foremost challenges facing reconfigurable application developers today is how to best exploit these novel and innovative resources to achieve the highest possible performance and energy efficiency. Recent developments in industry reveal a growing interest in the integration of configurable and reconfigurable technologies with more traditional processing devices. To face the programming challenges that this evolution has exacerbated, we have also witnessed the definition of programming languages and execution models aiming at enabling highly productive design methodologies for these emerging systems.

Over the last 11 years, the International Applied Reconfigurable Computing (ARC) symposium series (www.arc-symposium.org) has provided a forum for dissemination and discussion of this transformative research area. The ARC symposium was first held in 2005 in Algarve, Portugal. The second edition took place in Delft, The Netherlands, in 2006 and was the first edition to have its proceedings published by Springer as a volume of its *Lecture Notes in Computer Science* series. Subsequent ARC yearly editions were held in Rio de Janeiro, Brazil (2007), London, UK (2008), Karlsruhe, Germany (2009), Bangkok, Thailand (2010), Belfast, UK (2011), Hong Kong, SAR China (2012), Los Angeles, USA (2013), Algarve, Portugal (2014), and in 2015 in Bochum, Germany. This year the symposium (ARC 2016) returned to Rio de Janeiro, Brazil, during March 22–24, 2016, and was co-chaired by Prof. Vanderlei Bonato from the The Institute of Mathematical and Computer Sciences (ICMC), University of Sao Paulo (USP), Brazil, and Dr. Aravind Dasu from the Information Sciences Institute, University of Southern California (USC), USA. This year's edition included a series of international invited speakers from the areas of reconfigurable technology and evolutionary computing. They expressed their views on the future of this technology and also its application in evolutionary computing algorithms. The technical program also included mini-courses focusing on tools and applications of FPGA in areas such as

high-performance computing, streaming data, and data-flow computation and programming models and languages.

The technical program chairs for ARC 2016 were Dr. Christos Bouganis from Imperial College London, UK, and Dr. Marek Gorgon from AGH University of Science and Technology, Poland. A total of 47 papers were submitted to the symposium from 20 countries: Australia (1), Belgium (1), Brazil (6), China (2), Colombia (3), Ecuador (1), France (1), Germany (6), Hong Kong (1), India (2), Japan (3), Republic of South Korea (1), Mexico (2), Pakistan (1), Poland (1), Portugal (1), Romania (1), Switzerland (2), UK (7), and USA (4). All submissions were evaluated by at least three members of the Program Committee. After careful selection, 20 papers were accepted as full papers (acceptance rate of 42.5 %) and eight as short papers (global acceptance rate of 59.5 %). Those accepted papers formed very interesting symposium program, which we consider to constitute a representative overview of ongoing research efforts in reconfigurable computing, a rapidly evolving and maturing field. In addition the proceedings also included three invited papers as part of a special technical session on funded R&D projects in the area of configurable and embedded computing. Following the ARC's tradition, the Technical Program Committee chairs selected a limited set of regular papers for consideration for a special issue of the Elsevier journal *Microprocessors and Microsystems: Embedded Hardware Design* (MICPRO) devoted to this year's ARC.

Several people contributed to the success of the 2016 edition of the symposium. We would like to acknowledge the support of all the members of this year's Steering and Program Committees in reviewing papers, in helping with the paper selection, and in giving valuable suggestions. Special thanks also to the additional researchers who contributed to the reviewing process, to all the authors who submitted papers to the symposium, and to all the symposium attendees. Last but not least, we are especially indebted to Juergen Becker from the University of Karlsruhe and to Alfred Hoffmann and Anna Kramer from Springer for their support and work in publishing this book as part of the LNCS series.

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