

Chapter 2

Neural Signal Conditioning Circuits

Abstract The increasing density and the miniaturization of the functional blocks in these multi-electrode arrays presents significant circuit design challenge in terms of area, power, and the scalability, reliability and expandability of the recording system. In this chapter, we present a neural signal conditioning circuit for biomedical implantable devices, which includes low-noise signal amplification and band-pass filtering. The circuit is realized in a 65 nm CMOS technology, and consumes less than 1.5 μW . The fully differential low-noise amplifier achieves 40 dB closed loop gain, occupies an area of 0.04 mm², and has input referred noise of 3.1 μV_{rms} over the operating bandwidth 0.1–20 kHz. The capacitive-attenuation band-pass filter with first-order slopes achieves 65 dB dynamic range, 210 mV_{rms} at 2 % THD and 140 μV_{rms} total integrated output noise.

2.1 Introduction

Minimally invasive monitoring of the electrical activity of specific brain areas using implantable microsystems offers the promise of diagnosing brain diseases, as well as detecting and identifying neural patterns which are specific to behavioral phenomenon. Neural pattern classification and recognition require simultaneous recording from a large number of neurons (and recording the LFP and spike signals simultaneously). This, however, leads to the requirement of large dynamic range and signal bandwidth for the analog front-end. In the worst case, we assume that spikes with an amplitude of tens of μV added on LFPs with an amplitudes of about 2 mV appear at the input of a recording channel. If an input-referred noise of 2 μV is needed to meet the signal-to-noise ratio requirement of the spike signal, the dynamic range of the channel is around 60 dB, resulting in a 10-bit A/D conversion. Additionally, this sampling has to be done fast enough to capture the information in spikes, e.g. 32 kHz sampling rate. For a neural recording device with 100 channels this results in a data rate of 32 Mbs⁻¹. Furthermore, extensive

recording in vivo demands complying with severe safety requirements. For example, the maximum temperature increase due to the operation of the cortical implant in any surrounding brain tissue should be kept at less than 1 °C [1].

The limited total power budget imposes strict specifications on the circuit design of the low-noise analog front-end and high-speed circuits in the wideband wireless link, which transmits the recorded data to a base station located outside the skull. The design constraints are more pronounced when the number of recording sites increases to several hundred for typical multi-electrode arrays.

Front-end neural amplifiers are crucial building blocks in implantable cortical microsystems. Low-power and low-noise operation, stable dc interface with the sensors (microprobes), and small silicon area are the main design specifications of these amplifiers. The power dissipation is dictated by the tolerable input-referred thermal noise of the amplifier, where the trade-off is expressed in terms of noise efficiency factor [2]. For an ideal thermal-noise-limited amplifier with a constant bandwidth and supply voltage, the power of the amplifier scales as $1/v_n^2$ where v_n is the input-referred noise of the amplifier. This relationship shows the steep power cost of achieving low-noise performance in an amplifier.

In this chapter, we introduce a novel, low-power neural recording interface system with capacitive-feedback low noise amplifier and capacitive-attenuation band-pass filter. The capacitive-feedback amplifier offers low-offset and low-distortion solution with optimal power-noise trade-off. Similarly, the capacitive-attenuation band-pass filter provides wide tuning range and low-power realization, while allowing simple extension of the transconductors linear range, and consequently, ensuring low harmonic distortion. The low noise amplifier and band-pass filter circuit are realized in a 65 nm CMOS technology, and consume 1.15 μ W and 390 nW, respectively. The fully differential low-noise amplifier achieves 40 dB closed loop gain, and occupies an area of 0.04 mm². Input referred noise is 3.1 μ V_{rms} over the operating bandwidth 0.1–20 kHz. Distortion is below 2 % total harmonic distortion (THD) for typical extracellular neural signals (smaller than 10 mV peak-to-peak). The capacitive-attenuation band-pass filter with first-order slopes achieves 65 dB dynamic range, 210 mV_{rms} at 2 % THD and 140 μ V_{rms} total integrated output noise.

The chapter is organized as follows: Sect. 2.2 focuses on the signal conditioning circuit details, while Sect. 2.3 offers brief overview of the operational amplifier circuit concepts. Experimental results obtained are presented in Sect. 2.4. Finally, Sect. 2.5 provides a summary and the main conclusions.

2.2 Power-Efficient Neural Signal Conditioning Circuit

The neural spikes, typically ranging from 10 to 500 μ V and containing data up to ~20 kHz, are amplified with low noise neural amplifier (LNA) illustrated in Fig. 2.1, where V_{ref} voltage designates the node connected to the reference electrode. The amplifier A_1 is designed based on an operational transconductance

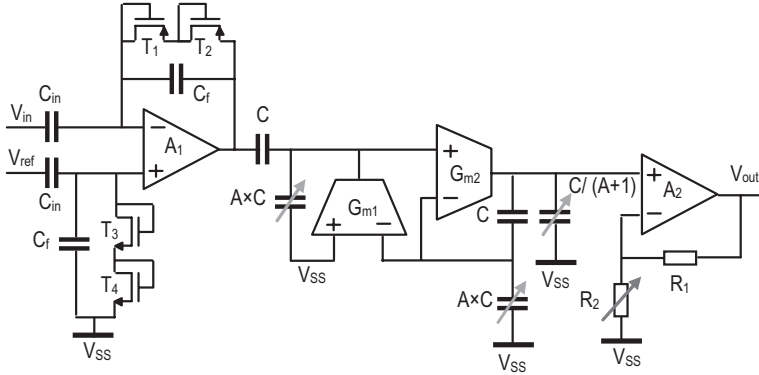


Fig. 2.1 Schematic of the signal conditioning circuit including low noise amplifier, band-pass filter and programmable gain amplifier

amplifier that generates a current proportional to the differential input voltage. The amplifier has a capacitive feedback configuration, which is adapted from [3] with minor modifications. Neural amplifiers typically employ two different feedback path structures, to realize a high-pass filter, i.e. with two subthreshold-biased transistors or with two diode-connected transistors. Two identical diode-connected transistors T_{1-2} and T_{3-4} act as a high value resistors R_h ($>10^{12} \Omega$) and adjust the low frequency high-pass cutoff of the amplifier at $((2\pi R_h C_f)^{-1} = 0.5 \text{ Hz})$ that blocks the dc offset induced by the electrode-tissue interface (typically around 1 V), and local field potentials (LFP), typically with 0.1–50 mV amplitude at 300 Hz and below. The mid-band gain A_{mb} is set by C_{in}/C_f , and the low-pass cutoff frequency is approximately placed at $g_{m,in}/A_{mb}C_L$, where $g_{m,in}$ is the transconductance of the input differential pair, and C_L is the effective load capacitance of the amplifier.

As neural recording involves the measurements of very small voltages, noise can become a limiting factor in the system performance. The total noise at the input of the neural interface is composed of the noise introduced by the electrodes and the input-referred noise of the electronic circuitry.

The former is determined by the material of the electrodes, the impedance and other characteristics of the electrode-electrolyte/tissue interface. The latter mainly includes thermal and flicker noise of every component in the circuit. The noise of the electronic system must be kept lower than the electrode noise ($10\text{--}20 \mu\text{V}_{\text{rms}}$ [4]). So that it has a minor contribution to the overall noise. In a multi-stage system, the noise of the first stage (input) has the largest effect on the circuit noise due to the amplification of the following stages. Therefore, the design of the input stage becomes critical and involves numerous trade-offs with other important specifications such as power consumption and area. If the input stage is an instrumentation amplifier, the ideal input-referred noise, assuming transistors in the subthreshold region and a first-order frequency response, can be expressed as $V_{\text{rms},ni} = \sqrt{[(4kT \pi U_T BW)/(\kappa^2 I_{\text{tot}})]}$ [5], where k is Boltzmann constant, T is the

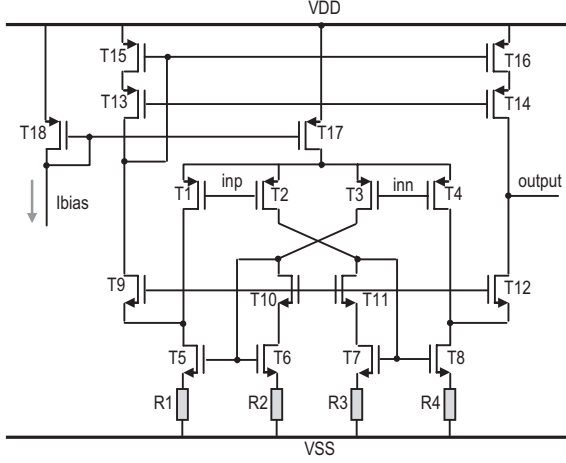


Fig. 2.2 Folded cascode LNA circuit

absolute temperature, U_T is the thermal voltage, κ is the subthreshold gate coupling coefficient, I_{tot} is total supply current and BW is the -3 dB bandwidth of the amplifier. Consequently, for a given bandwidth the noise is inversely proportional to the square root of the supply current, hence, there exists a trade-off between noise and power consumption (Appendix A-1).

Implemented low noise, low power LNA G_m folded cascode circuit is illustrated in Fig. 2.2. The topology is based on [6], where current splitting technique [7] to enhance the drain resistance of both input and bottom transistors without any additional cascading, is combined with the output-current scaling [5] technique to lower the OTA noise.

The noise contributions of the amplifier are minimized to be almost those of only its two input transistors, due to the use of cascoded resistive loading rather than current-source loads. The folded cascode G_m circuit realize a wide input common-mode range and a relatively high open-loop gain within one stage. The input-referred noise of the G_m circuit is reduced by increasing the g_m of input pair and cascode devices, and increasing the aspect ratio of the devices. The effect of the last method, however, is partially canceled by the increase in the noise excess factor. When referred to the G_m input, thermal noise voltages of the transistors used as current sources (and mirrors) are multiplied by the g_m of the device itself and divided by the g_m of the input transistor, which suggests that maximizing input pair g_m and minimizing g_m of the current sources (and mirrors) minimizes noise. The transistors of the output stage have two constrains: the g_m of the cascading transistors T_9 , T_{12} must be high enough, in order to boost the output resistance of the cascode, allowing a high enough dc gain. Secondly, the saturation voltage of the active loads T_{5-8} and T_{13-16} must be maximized, in order to reduce the extra noise contribution of the output stage. By making the cascading transistors larger

than the active loads the g_m of the cascading transistors is maximized, boosting the dc gain, while their saturation voltage is reduced, allowing for a larger saturation voltage for the active loads, without exceeding the voltage headroom. The bias current of the LNA can be varied to adapt its noise per unit bandwidth.

To keep the overall bandwidth constant when the bias current of the gain stage is varied, a band-pass filter [8] (Fig. 2.3) is added to the output of the LNA. High gain provided by the LNA stage alleviates noise floor requirements of this bandwidth-limiting stage. The total integrated output voltage noise of the filter depends on the linear range of the transconductors G_{m1} and G_{m2} (Fig. 2.4), the ratio of the attenuator capacitances A and the unit capacitance C . The linear range of the G_m is effectively improved by attenuating the input. In the high-pass stage, the signal is attenuated by a factor of $A+1$ and the full capacitance of $(A+1)C$ is then utilized for filtering with G_{m1} . In the low-pass stage, a gain of $A+1$ is applied to signals in the pass-band. A capacitance $C/(A+1)$ is added in parallel with the attenuating capacitances to increase the filtering capacitance.

2.3 Operational Amplifiers

Operating on the edge of the performance envelope, op amps exhibit intense trade-offs amongst the dynamic range, linearity, settling speed, stability, and power consumption. As a result, accuracy and speed are often dictated by the performance of these amplifiers.

Amplifiers with a single gain stage have high output impedance providing an adequate dc gain, which can be further increased with gain boosting techniques. Single-stage architecture offers large bandwidth and a good phase margin with

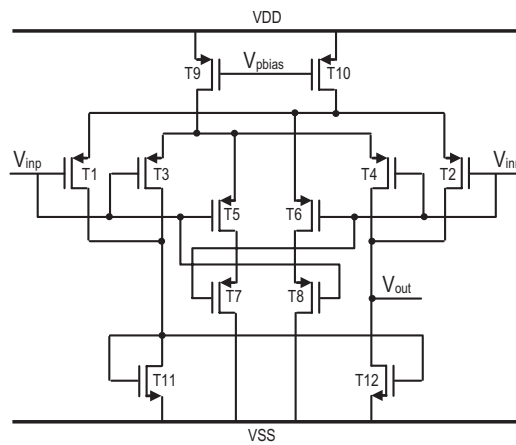


Fig. 2.3 Band-pass filter G_{m1} cell

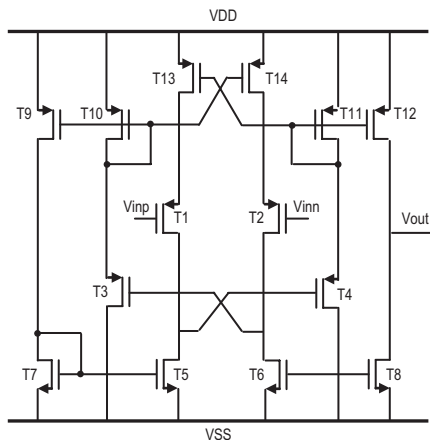


Fig. 2.4 Band-pass filter G_{m2} cell

small power consumption. Furthermore, no frequency compensation is needed, since the architecture is self-compensated (the dominant pole is determined by the load capacitance), which makes the footprint on the silicon small. On the other hand, the high output impedance is obtained by sacrificing the output voltage swing, and the noise is rather high as a result of the number of noise-contributing devices and limited voltage head-room for current source biasing.

The simplest approach for the one-stage high-gain operational amplifier is telescopic cascode amplifier [9] of Fig. 2.5. With this architecture, a high open loop dc gain can be achieved and it is capable of high speed when closed loop gain is low. The number of current legs being only two, the power consumption is small. The biggest disadvantage of a telescopic cascode amplifier is its low maximum output swing, $V_{DD} - 5V_{DS,SAT}$, where V_{DD} is the supply voltage and $V_{DS,SAT}$ is

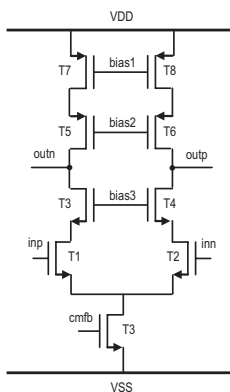


Fig. 2.5 One-stage amplifiers: telescopic cascode

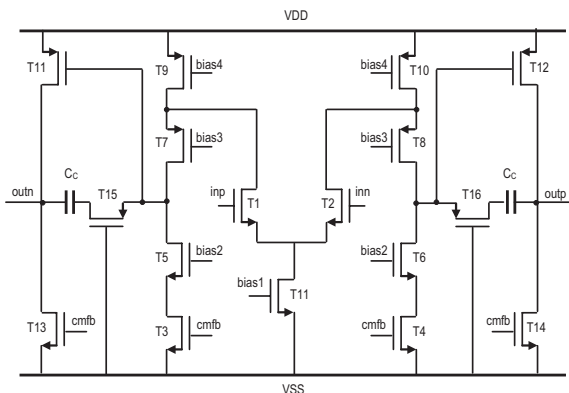


Fig. 2.9 Two-stage amplifiers: folded cascode amplifier with a common-source output stage and Miller frequency compensation

amplifier are comparable to those of the telescopic cascode and better than those of the folded cascode amplifier. The speed of a Miller-compensated amplifier is determined by its pole-splitting capacitor C_C . Usually, the position of this non-dominant pole, which is located at the output of the two-stage amplifier, is lower than that of either a folded-cascode or a telescopic amplifier.

Thus, in order to push this pole to higher frequencies, the second stage of the amplifier requires higher currents resulting in increased power dissipation. Since the first stage does not need to have a large output voltage swing, it can be a cascode stage, either a telescopic or a folded cascode. However, the current consumption and transistor count are also increased. The advantages of the folded cascode structure are a larger input common-mode range and the avoidance of level shifting between the stages, while the telescopic stage can offer larger bandwidth and lower thermal noise.

Figure 2.9 illustrates a folded cascode amplifier with a common-source output stage and Miller compensation. The noise properties are comparable with those of the folded cascode amplifier. If a cascode input stage is used, the lead-compensation resistor can be merged with the cascode transistors. An example of this is the folded cascode amplifier with a common-source output stage and Ahuja-style compensation [15] shown in Fig. 2.10. The operation of the Ahuja-style compensated operational amplifier is suitable for larger capacitive loads than the Miller-compensated one and it has a better power supply rejection, since the substrate noise coupling through the gate-source capacitance of the output stage gain transistors is not coupled directly through the pole-splitting capacitors to the operational amplifier output [15].

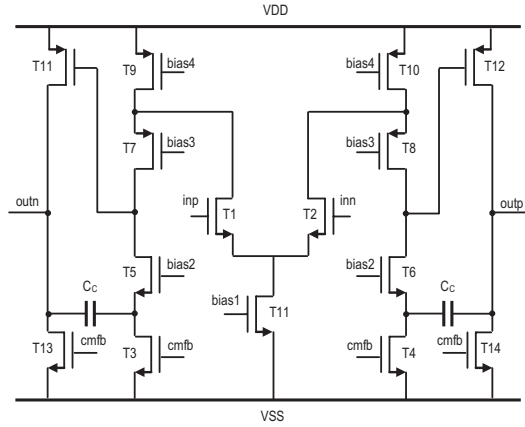


Fig. 2.10 Two-stage amplifiers: folded cascode amplifier with a common-source output stage and Ahuja-style frequency compensation

2.4 Experimental Results

Design simulations on the transistor level were performed at body temperature (37 °C) on Cadence Virtuoso using industrial hardware-calibrated TSMC 65 nm CMOS technology. The analog circuits operate with a 1 V supply, while the digital blocks operate at near-threshold from a 400 mV supply. The test dataset (Fig. 2.11) is based on recordings from the human neocortex and basal ganglia. The signal quality in neural interface front-end, beside the specifics of the electrode material and the electrode/tissue interface, is limited by the nature of the bio-potential signal, dictating system resource constraints (power, size, bandwidth, and thermal dissipation i.e. to avoid tissue damage). When a neuron fires an action potential, the cell membrane becomes depolarized by the opening of voltage-controlled neuron channels leading to a flow of current both inside and outside the neuron. The time series representation of an neuron signal at the preamplifier's input (Fig. 2.12) are composed of a spike burst, plus additive Gaussian white noise (grey area with 1000 randomly selected neural channel compartments and black area with filtered out predicted bias from the estimated variance σ^2).

Since extracellular media is resistive [16], the extracellular potential is approximately proportional to the current across the neuron membrane. Hence, by maintaining a constant current density, the relative uncertainty of the current becomes inversely proportional to the square of the interface area. The membrane roughly behaves like an RC circuit and most current flows through the membrane capacitance. In typical electrode-tissue interface, we are relying on the current measurement to sense these neural signals. Hence, by maintaining a constant current density, the relative uncertainty of the current becomes inversely proportional to the square of the interface area. The electrode noise spectral density has an

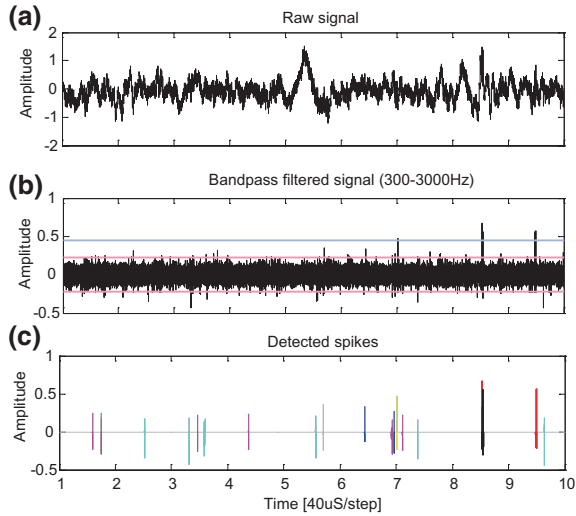


Fig. 2.11 Test data set, the y axis is arbitrary; **a** top: raw signal after amplification, not corrected for gain, **b** bandpass filtered signal, and **c** detected spikes

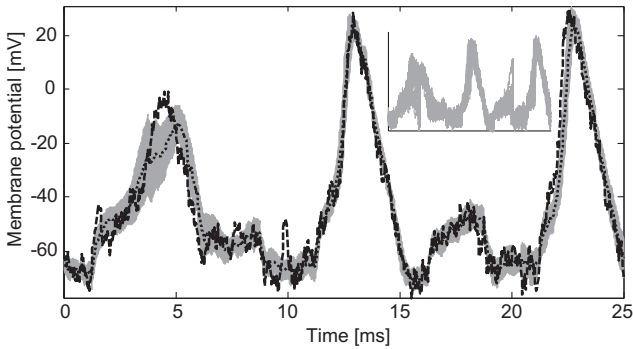


Fig. 2.12 Statistical voltage trace of neuron cell activity; *Grey Area*—Voltage traces from 1000 randomly selected neural channel compartments, *Black Area*—Expected voltage trace

approximate dependence of -10 dB/dec for small frequencies. However, for frequencies higher than 1 – 10 kHz, capacitances at the interface form the high-frequency pole and shape both the signal and the noise spectrum; the noise is low-pass filtered to the recording amplifier inputs.

Due to the small amplitude of neural signals and the high impedance of the electrode tissue interface, amplification and low-pass filtering of the extra-cellular neural signals is performed before the signals can be digitized. An

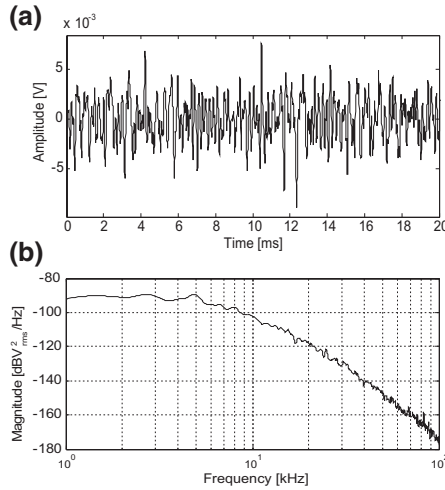


Fig. 2.13 **a** Noise amplitude in time-domain at the output of the low-pass filter; **b** noise PSD at the output of the low-pass filter

example of the time-domain noise estimation and noise power spectral density at the output of the low-pass filter is illustrated in Fig. 2.13. For frequencies higher than ~ 10 kHz, capacitances at the interface form the high-frequency pole and shape both the signal and the noise spectrum; the noise is low-pass filtered to the recording amplifier inputs. The interface's input equivalent noise voltage decreases as the gain across the amplifying stages increases, i.e. the ratio of the square of the signal power over its noise variance can be expressed as $SNR = F_{\Sigma}^2 / (\sigma_{neural}^2 + \sigma_{electrode}^2 + \Sigma_i (\Pi_j G_j^{-1}) \sigma_{amp,i}^2)$, where F_{Σ} is the total signal power, $\sigma_{amp,i}^2$ represents the variance of the noise added by the i th amplification stage with gains G_j , $\sigma_{electrode}^2$ is the variance of the electrode, and σ_{neural}^2 is variance of the biological neural noise. The observed SNR of the system also increases as the system is isomorphically scaled up, which suggests a fundamental trade-off between SNR and speed of the system.

The fully differential low-noise amplifier achieves 40 dB closed loop gain, and occupies an area of 0.04 mm^2 . Input referred noise is $3.1 \mu\text{V}_{\text{rms}}$ over the operating bandwidth 0.1–20 kHz. Distortion is below 2 % total harmonic distortion (THD) for typical extracellular neural signals (smaller than 10 mV peak-to-peak). The common-mode rejection ratio (CMRR) and the power-supply rejection ratio (PSRR) exceed 75 dB.

The capacitive-attenuation band-pass filter with first-order slopes achieves 65 dB dynamic range, $210 \text{ mV}_{\text{rms}}$ at 2 % THD and $140 \mu\text{V}_{\text{rms}}$ total integrated output noise. Total harmonic distortion of the V/I converter is 0.04 % at 20 kHz. Table 2.1 compares the state of the art neural recording systems to this work.

Table 2.1 Neural interface comparison with prior art

Interface	[17]	[18]	[19]	[20]	[this work] ^a
Technology	0.18	0.13	0.18	0.065	0.065
V_{DD} [V]	0.45	1.2	1.8	1	1
Gain [dB]	52	54–60	30–72	52.1	65
INF [μ V _{rms}]	3.2	4.7	3.2	4.13	3.1
Bandwidth [Hz](k)	10	10–5	300–6	1–8.2	20
P/channel [μ W]	0.73	3.5	5.4	2.8	2.1
A/channel [mm ²]	0.2	0.09	0.08	0.042	0.036

^aSimulated data

2.5 Conclusions

Bio-electronic neural interfaces enable the interaction with neural cells by recording, to facilitate early diagnosis and predict intended behavior before undertaking any preventive or corrective actions, or by stimulation, to prevent the onset of detrimental neural activity such as that resulting in tremor. Multi-channel neural interfaces allow for spatial neural recording and stimulation at multiple sites. To evade the risk of infection, these systems are implanted under the skin, while the recorded neural signals and the power required for the implant operation is transmitted wirelessly. The maximum number of channels is constrained with noise, area, bandwidth, power, which has to be supplied to the implant externally, thermal dissipation i.e. to avoid necrosis of the tissues, and the scalability and expandability of the recording system. Very frequently an electrode records the action potentials from multiple surrounding neurons. Subsequently, the ability to differentiate spikes from noise is governed by, both, the discrepancies between the noise-free spikes from each neuron, and the signal-to-noise level of the recording interface. After the waveform alignment, a feature extraction step characterizes detected spikes and represent each detected spike in a reduced dimensional space. The feature extraction and spike classification significantly reduce the data requirements prior to data transmission (in multi-channel systems, the raw data rate is substantially higher than the limited bandwidth of the wireless telemetry).

In this chapter, we introduce a low-power neural signal conditioning circuit with capacitive-feedback low-noise amplifier and capacitive-attenuation band-pass filter. The capacitive-feedback amplifier offers low-offset and low-distortion solution with optimal power-noise trade-off. Similarly, the capacitive-attenuation band-pass filter provides wide tuning range and low-power realization, while allowing simple extension of the transconductors linear range, and consequently, ensuring low harmonic distortion.

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