Chapter 2
Defining the Optimal Architecture

2.1 Introduction

The basic modern communication system comprises a large array of mobile equipment into a wireless network. The communication between all these equipment is regulated by various communication standards, depending on the type of wireless network in which they are connected.

In order to maximize the potential of wireless communications, the latest wireless standards converge towards a "one size fits all" solution. As an example, the W-LAN standard, IEEE 802.11ac, uses almost all basic digital modulation schemes (i.e., BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, and 1024-QAM) on OFDMA carrier support with variable modulation depths, while it still maintains compatibility with the earlier IEEE 802.11 lower data rate standards.

Hence, the latest developments in standardization point to a software re-configurable hardware solution for the radio front-end as the best way to trade-off backwards compatibility with future trends. This observation is critical as we move on towards the 5G deployment.

The main target of this chapter is to determine the optimum architecture choice suited for the SDRX. The analysis starts with an overview of the standard receiver architectures in Sect. 2.2 and, subsequently in Sect. 2.3, and determines the quadrature direct conversion topology suits best the envisaged purpose. For such receiver architectures, regardless of the communication wireless standards, the received signal is downconverted directly to baseband and the digital signal processor (DSP) software demodulation scheme is changed accordingly such as it can handle it. Hence, the possibility of implementing a "universal receiver" is revealed [1].

The chapter continues, in Sect. 2.4, by constructing the solutions that make direct conversion receivers ready for monolithic integration. *The presented solutions are realized without introducing particular analog tricks to satisfy the needs of only one of the standards, as the SDRX must represent a "universal receiver,"*

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and not be turned into a "multi-standard Application Specific Integrated Circuit (ASIC)."

Further on, Sect. 2.4 presents the natural architectural evolutions due to the increased power consumption efficiency of modern ADCs.

2.2 Overview of Receiver Architectures: Following the Image Rejection

2.2.1 Superheterodyne Receivers

Single Conversion

The superheterodyne architecture was developed in 1918 by Edwin Armstrong as a viable alternative to the regenerative receiver with respect to the technical issues of vacuum tubes implementation [1]. The basic block schematic of this concept is depicted in Fig. 2.1. The original superheterodyne uses only one downconverter mixer, *single conversion* superheterodyne, and mixes the Radio Frequency, RF, input signal with the Local Oscillator, LO, signal.

The resulting signal frequency is shifted down to an Intermediate Frequency, IF, equal to the difference between the RF carrier and LO signal frequencies.

Intrinsically the mixing process will render at the mixer output also the sum frequency component. For most applications this component represents an unwanted signal and is filtered by the band-pass filter following the mixer and/or in the mixer output stage.

The major issue of superheterodyne topology is the image frequency rejection. The problem resides in the fact two symmetrical signals with frequencies spaced apart by twice the IF frequency are downconverted by LO mixing to the same IF frequency, as shown in Fig. 2.2.

If the communication is dual sideband, meaning both RF signals convey the same useful information, there is the no problem, since spectrum overlapping in the IF band is beneficial. However, this is not the case for the vast majority of applications, which are employing single side band communication. Thus, the unwanted image signal rejection becomes critical.

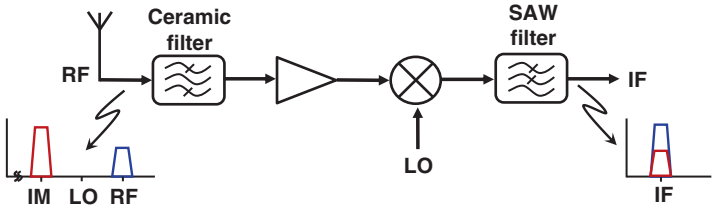

Fig. 2.1 Single conversion superheterodyne receiver block schematic

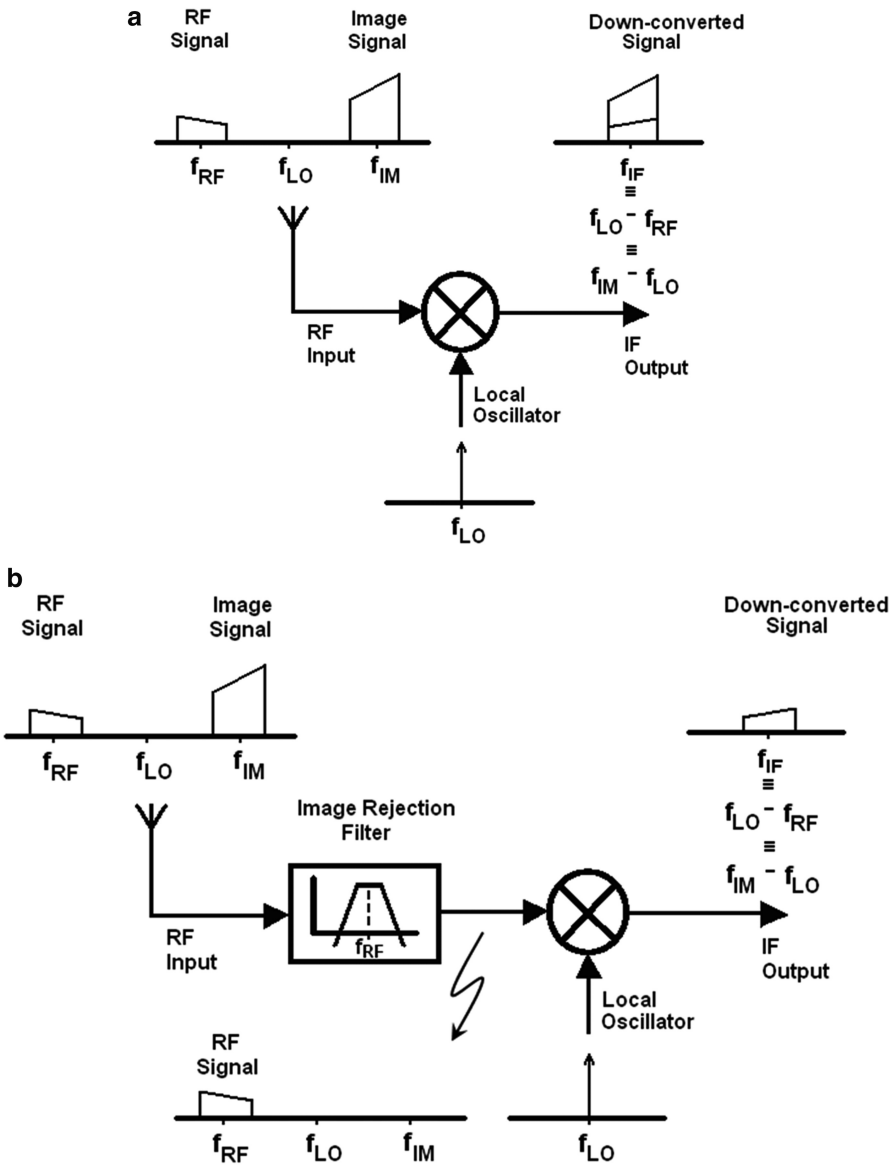

Fig. 2.2 Downconversion: (**a**) without Image Rejection and (**b**) with Image Rejection

The superheterodyne architecture solves the issue by filtering the image signal before it enters the mixer, or more precisely, immediately after the antenna. The image rejection filter specifications depend on the IF value and they are more relaxed as the image frequency is larger, respectively, as the distance between the RF carrier and its image is larger.

Signal conditioning constraints, set by the channel selection filter—the second band-pass filter of Fig. 2.1, prevent the choice of a very large IF, thus toughening image filtering requirements. In practice, ceramic filters satisfy the constraints, although they possess two major drawbacks: they are quite expensive and by far not compatible with monolithic integration.

Channel selection is also demanding, as for many applications channel bandwidth is fairly small compared with IF. In such context, bandpass Surface Acoustic Wave (SAW) filters are used for analog channel selection. However, these types of filters are unattractive to SoC ICs for the same two reasons as the ceramic antenna filters: incompatibility with monolithic integration and high cost.

In conclusion, single conversion superheterodyne receiver design is driven by the trade-off between antenna and channel filtering, which imposes the optimum IF frequency.

Dual or Double Conversion

For *Single Conversion* superheterodyne, the choice of a low IF leads to tough specifications for the antenna filter but does not affect the ones for the channel filter, while a high IF constraints the channel filtering and relaxes the antenna filter specifications. Either way, for most wireless applications, the antenna filtering requirements lead to choosing a cumbersome ceramic filter as the image filter and the IF filtering requirements impose a SAW filter for analog channel selection.

The *Dual Conversion* superheterodyne, which principle schematic is depicted in Fig. 2.3, uses two IFs to ease the image filtering and channel selection, respectively, to relax the antenna and channel filters specifications. The idea is to first up-convert the incoming RF signal to a high IF, relaxing image filtering requirements, while the downconversion mixing is made to a low IF, simplifying channel selection. Still, for most applications, the antenna and image filters will require implementation by ceramic filters.

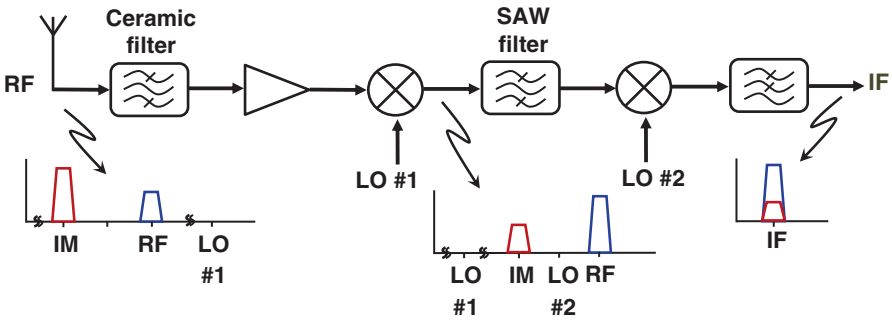

Fig. 2.3 Dual conversion superheterodyne receiver block schematic

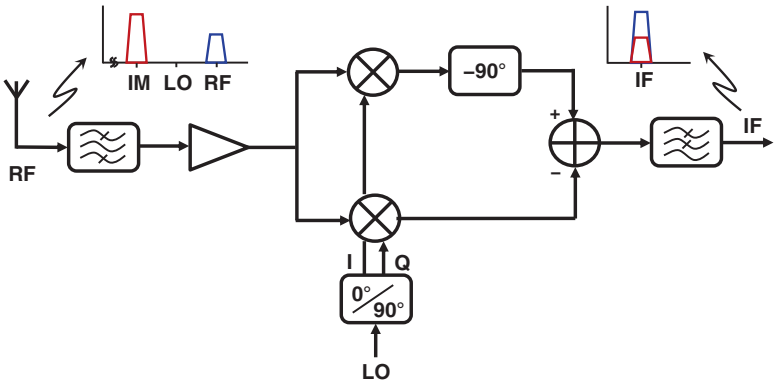

Fig. 2.4 Image rejection receiver

Hence, superheterodyne architectures cannot solve the image rejection problem monolithically.

2.2.2 Image Rejection Receivers

So far, the design of superheterodyne receivers has been optimized to alleviate image rejection rather than optimizing RF performance.

An image rejection receiver uses a "*complex*" mixer to cancel out the unwanted image signal, removing the lock on architecture and allowing the system design to optimize RF performance. The principle schematic of such a receiver is depicted in Fig. 2.4.

The "*complex*" mixer is made out of two mixers which share the same RF input, while the LO port is controlled by two quadrature signals. By adding a 90° delay line in one signal path, the downconverted image signals will be in-phase, while the useful signals will be 180° delayed. Hence, by considering the difference between the two paths the image signal is cancelled, while the useful signal is added.

The major advantage of this approach is the antenna filtering becomes less critical. Thus, the use of expensive and bulky, external (off-chip), ceramic filters is no longer required. On the other hand, the image rejection now depends on the quadrature accuracy of both gain and phase of the LO and IF paths. If the two LO signals exhibit exactly 90° phase delay and have the same amplitude, while the gain of the two paths are perfectly matched, the unwanted image signal is completely rejected.

Hence, image rejection receivers cancel out the image signals by subtracting two potentially very large signals, and resulting in a difference that is theoretically equal to zero. However, any gain or phase error between the two signal paths will result in incomplete cancelation of the image signal. Thus, the image rejection is given by [2]:

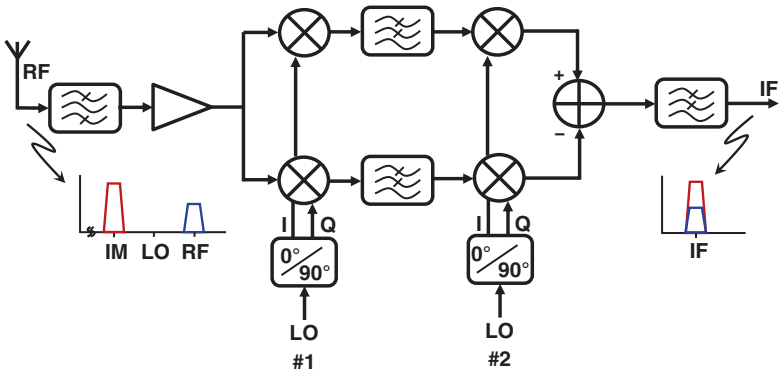

Fig. 2.5 Weaver receiver

$$\text{Image Rejection} = -20\log\left\{\frac{1}{2}\left[\frac{Gain_{I-Q\ \ err}}{Gain} + tg\left(Phase_{I-Q\ \ err}\right)\right]\right\}\ \ [\text{dBc}] \quad (2.1)$$

where *Gain* represents the receiver's gain, $Gain_{I\text{-}Qerr}$ is the I-Q gain mismatch, and $Phase_{I\text{-}Qerr}$ is the I-Q phase mismatch.

Since accurate wide-band quadrature phase shifters are difficult to design, Weaver receivers of Fig. 2.5 are preferred. To cancel the need for 90° phase shifter on signal path, an extra pair of mixers and quadrature LO signals are required.

Still, the LO signals quadrature accuracy, of both gain and phase, and the gain matching of the quadrature downconverted channels set the image rejection performance as described by (2.1).

For both image rejection approaches, if a low IF is chosen then the IF filtering requirements are relaxed, as well as subsequent A/D conversion or baseband processing. The image rejection can typically be lowered to about −35 dB with quadrature generators like Poly Phase Filters or divide-by-2 Johnson Counters.

2.2.3 Direct Conversion Receivers

All receiver architectures presented so far have to fight image rejection. In general, a signal and its image are spaced apart by twice the Intermediate Frequency (IF). To reject the image, superheterodyne receivers require the use of expensive off-chip SAW filters, while dual-conversion architectures trade-off the SAW filter for a standard, but still bulky and expensive, ceramic filter, at the expense of an extra up-converter mixer.

In Fig. 2.6 the typical block schematic of a quadrature direct conversion receiver is depicted. Quadrature LO drive enables the receiver to demodulate the RF signal regardless of the phase relation between the LO and incoming RF signals [1].

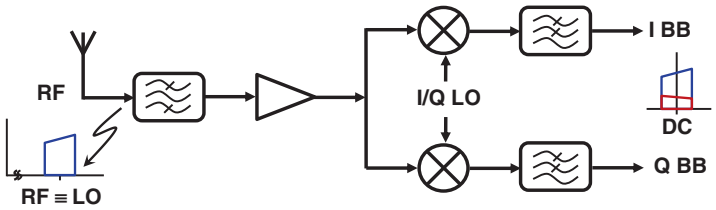

Fig. 2.6 Quadrature direct conversion receiver

In direct conversion receivers, also known as homodyne or zero-IF, the IF frequency is zero. Hence, the useful signal is its own image. *Therefore, in a zero-IF system the image signal has an amplitude comparable to the useful signal, and thus, image rejection requirements are drastically relaxed.* Furthermore, all baseband processing, like analog baseband signal conditioning, analog-to-digital conversion and the digital demodulation, take place at the lowest possible frequency.

These features make the direct conversion receiver an ideal candidate for monolithic integration and open the possibility of creating a "*universal*" receiver, compatible with all wireless standards. However, although direct conversion receivers monolithic integration seems straightforward, there are several drawbacks to this approach.

First of all, the zero-IF architecture is extremely sensitive to DC offset and 1/*f* noise. As the signal is directly converted to baseband, receiver noise figure is affected by 1/*f* noise and its output risks of being overloaded even for small values of the DC offset, in the order of a few tens of μV. Such low DC offset, or 1/*f* noise, values are not easily achievable in practice. Regular AC coupling will not be solving the issue, as receiver settling will be severely affected by a low cutoff frequency, in the order of a few hundred Hz.

Some of these problems have been already addressed at protocol level, as the latest wireless standards tend to use modulation schemes that minimize the baseband signal low frequency spectral energy. Also, for Time Division Multiple Access (TDMA) systems, a dedicated time slot for calibration is foreseen: the guard band. Hence, static offset cancelation is possible before each actual receive burst.

The second major issue of direct conversion architecture is that even-order distortions generate a signal-dependent DC offset. Handling dynamic offset, to the extent required by almost all commercial wireless standards, implies the usage of a differential architecture for the whole receiver chain, starting with its Low Noise Amplifier (LNA).

Another issue of such architecture is self-mixing. The LO signal, which in most cases is orders of magnitude larger than the RF signal, leaks to the RF port of the mixer and is mixed down to baseband. If the LO leaking signal is phase shifted with respect to the real LO, this almost always being the case in practice, the DC offset caused by self-mixing dominates the mixer output. Hence, very good isolation between RF and LO mixer ports is required for good receiver performance.

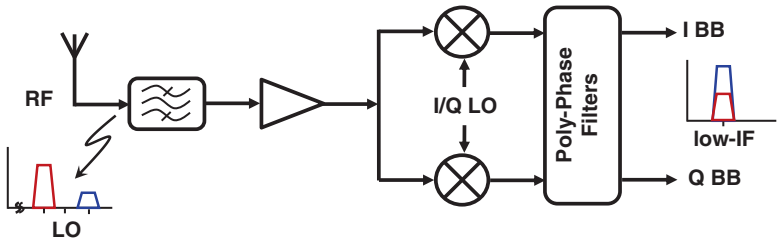

Fig. 2.7 Low-IF receivers

Also, because the large gain of the direct conversion receiver is focused at one frequency, the isolation between input and output of the receiver is critical, as any parasitic feedback loop may lead to system instability.

2.2.4 Low-IF Receivers

Finally, although direct conversion architecture has very relaxed image rejection specifications, it has to fight with DC offset, 1/f noise, and self-mixing.

Hence, the low-IF architectures (see Fig. 2.7) become attractive. Essentially, the RF signal will now be downconverted to a low-IF frequency (i.e., up to a few hundred kHz) and thus, the issues of direct conversion receivers are alleviated.

However, the image rejection requirements are again heavily constricted. This stresses the implementation of the active poly-phase filter that follows the complex mixer and is used for image rejection and channel selection.

2.3 Final Decision: w/ IF vs. w/o IF (Zero-IF)

The main features of a SDRX must be a versatile architecture and the ability to be reconfigured on-the-fly as the communication burst requires.

From the perspective of SoCs, the optimization of the chip power dissipation and die area is mandatory. As the SDRX will be embedded in an SoC, this trade-off must be the main guideline in sizing the SDRX design, as well as in choosing its architecture, as a first and, very important, starting point. *The SDR architectures of choice are superheterodyne* (*w/ IF*)*, either single or dual conversion, low IF* (*w/ IF*) *or direct conversion* (*w/o IF*).

From area perspective the cumbersome image rejection filters of superheterodyne topology are not so attractive for monolithic integration. On the other hand, for direct conversion the image rejection requirements are much smaller than for any other receiver architecture.

Furthermore, the IF selection for superheterodyne architectures is fairly cumbersome and cannot be extrapolated in a systematic way to all standards, as it would be required for a true SDRX [3]. Basically, the IF should be chosen to avoid the in-band downconversion of strong interferers. In most applications the nearest strong interferers are located three channels apart from the RF carrier. As the channel bandwidth differs even within the same wireless standard, it is not possible to select intermediate frequencies which will lead to reuse of same image filters for a multi-bandwidth environment compatible receiver.

From the power consumption perspective, the direct conversion topology has even more advantages.

First of all, the baseband signal processing takes place at the lowest possible frequency.

Secondly, this topology is not tributary to the 3 dB noise penalty of superheterodyne architectures [2]. Basically, direct conversion quadrature receivers are using the information from both sidebands, as the image is actually the useful signal. While, for most commercial applications, the superheterodyne receivers are using only one sideband, as the image signal is not a useful signal (see Fig. 2.8).

By using an additional bandpass ceramic filter after the LNA, the single sideband superheterodyne receivers noise penalty is reduced. However, this makes the overall system even more unattractive for monolithic integration.

So far the zero-IF architecture had presented overwhelming advantages to the heterodyne approach, including also here the low-IF architecture, in terms of image rejection, and thus, for monolithic integration purposes.

It is true that the direct conversion has some issues with DC offset and 1/f noise that the low-IF architecture can overcome. However, these issues can be overcome as discussed in detail in Sect. 2.4, whereas the low-IF systems still have to fight very tough image rejection specifications.

Hence, it becomes clear that direct conversion receivers are the only ones capable of satisfying the requirements of a true SDRX.

Table 2.1 summarizes the advantages and disadvantages of the three architectures with respect to monolithic integration in a SDRX SoC.

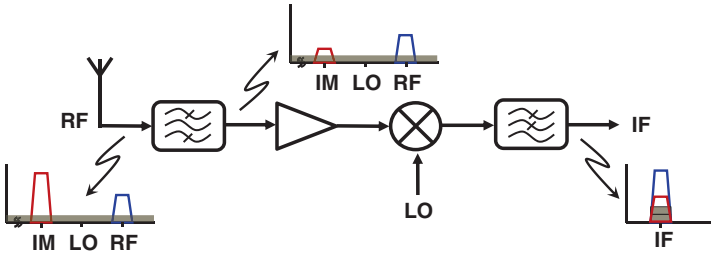

Fig. 2.8 Superheterodyne 3-dB noise penalty

Table 2.1 Heterodyne and low-IF vs. direct conversion receivers comparison regarding SoC integration—PROs and CONs

Superheterodyne		Low IF		Direct conversion	
PROs	CONs	PROs	CONs	PROs	CONs
☺ Well known	☹ **High image rejection requirement**	☺ No DC Offset	☹ **High image rejection requirement**	☺ **Low image rejection requirement**	☹ DC Offset
	SAW Filter	☺ Reduced 1/f noise	SAW Filter	No SAW Filter	☹ 1/f noise
	☹ IF selection	☺ Reduced self-mixing		☺ Image is wanted signal mirror	
	Difficult to mitigate the multi-standard environment			Mirror signal is not a strong interferer	
	☹ Power consumption			☺ Power consumption	
	Baseband signal conditioning is done at IF			Baseband signal conditioning is done at lowest frequency	
	☹ 3 dB noise penalty			☺ No 3 dB noise penalty	
	Image frequency band degrades receiver SNR by 3 dB			Quadrature receiver	

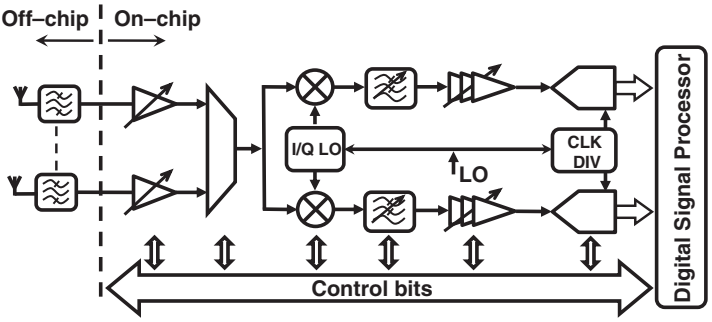

Fig. 2.9 SDRX block diagram

2.3.1 Receiver Block Schematic

The block schematic of a true multi-standard re-configurable receiver, including the final ADC, is depicted in Fig. 2.9.

The main tasks of a radio receiver consist in isolating the wanted, useful signal from other electromagnetic signals arriving at the antenna, amplifying and converting it from a (high) radio frequency (RF) to baseband (BB).

The incoming RF signal is picked up by the receiver's antenna and is amplified by one of its LNAs. Multiple LNAs can be integrated, depending on the envisaged use.

The *amplified* RF signal is then converted to current in the mixer input gm-stage and downconverted directly to baseband by mixing with a local oscillator signal of equal frequency. Hence, at the mixing stage output the signal has a spectrum spanning from DC to a maximum frequency that is dependent on the wireless communication standard, as detailed in Sect. 3.1.

After mixing, the signal is conditioned by a low-pass filter (LPF) and a variable gain amplifier (VGA), before its conversion to digital spectrum by an ADC.

Through digital control the SDRR blocks main characteristics (e.g., bandwidth, noise, and linearity) can be changed dynamically depending on the particular standard requirements or even on the particular communication burst necessities.

Basically, the receiver chain of Fig. 2.9 is split into a high-frequency (HF) part, comprised by the LNA and the gm stage of the downconverter and a remaining baseband low-frequency (LF) part, following the mixer's switching stage.

The receiver design is a result of noise-linearity trade-offs under power consumption constraints. The key trade-off shaping its design is the one between the LPF order and ADC power consumption, as detailed in Chap. 4. The receiver's high-frequency part is shaped mainly by noise requirements, while its baseband blocks must enforce a linear channel selection to prevent the RF useful signal distortion, as is detailed in Chap. 5.

2.4 Making Direct Conversion Receivers Ready for Monolithic Integration

2.4.1 Key Issues

As detailed in Sect. 2.2 and in-depth analyzed in [4], due to intrinsic operation of zero-IF systems, they exhibit a large sensitivity to DC offset, either static or dynamic, and 1/*f* noise. Also, self-mixing issues can dramatically reduce performance of receivers implemented with direct conversion architectures.

First of all, direct conversion architecture is extremely sensitive to static DC offsets and 1/*f* noise. As the signal is directly converted to baseband, receiver noise figure is affected by 1/*f* noise. Generally the mixer output is DC coupled to the LPF, since a major part of the received signal baseband spectral energy is located at low frequency (i.e., the GSM standard). Regular AC coupling will not solve the issue, as receiver settling will be severely affected by a low cutoff frequency in the order of a few hundred Hz. Also, given the large VGA gain, usually larger than 60 dB, the receiver output risks of being overloaded even for small values of the DC offset, in the order of a few hundred μV.

The second major issue of the zero-IF receiver architecture is even-order distortions generate a signal-dependent DC offset. As the received input power can change dynamically, since other transmitters may start to communicate, a dynamic offset component is generated due to the receiver second-order nonlinearity.

Also, the self-mixing process, determined by the LO mixing with the LO signal leaking from the Voltage Controlled Oscillator (VCO) to the receiver input, can generate a large DC offset overloading the receiver output.

The section main goal is to determine the architectural changes in Fig. 2.9 receiver, required to compensate the abovementioned issues. Section 2.4.2 covers the architecture sensitivity to static DC offsets and 1/*f* noise and explains the dynamic offset generation in the presence of second-order distortions. In Sect. 2.4.3, the best method to avoid self-mixing process is presented. Finally, Sect. 2.4.4 presents the updated SDRX block schematic, while Sect. 2.4.5 presents the natural evolution of Fig. 2.9 receiver.

2.4.2 DC Offset Compensation

Static Offset Removal

Low DC offset and 1/*f* noise values are required for proper signal demodulation during the receiving phase. In practice these low values are not easy to get without calibration.

Wireless communications are burst communications and a dedicated time slot for calibration is foreseen: the guard band. Thus, static offset cancelation is possible before each actual receive burst.

While the LNA is AC coupled to the mixer, the mixer output is DC coupled to the baseband part of Fig. 2.9 receiver. One of the possibilities to calibrate the receiver static DC offset is the use of the correlated double sampling technique [5]. This offset compensation technique is preferred to chopper stabilization [6] as there is no risk of spurs overwhelming the receiver output spectrum.

This analog technique, described by Fig. 2.10, implies in a first phase (i.e., *Offset_meas* control signal @ "High"—switches closed) sampling the baseband chain DC offset on a capacitor, via the additional transimpedance amplifier, while the antenna input is shorted to ground [7].

During normal operation, the second phase (i.e., *Offset_meas* @ "Low"—switches open), the RF input is connected again to the antenna and the signal flows through the receiver, while the DC offset is inherently cancelled out. The frequency of two phases alternation is set by the baseband signal bandwidth: the smaller the baseband signal bandwidth, the higher is the duration of the DC offset sampling (see Table 3.1).

The advantage of this technique is the 1/*f* noise is also reduced, next to the static offset cancelation; the drawback is the white noise level doubling because of the aliasing. Hence, in order to reduce the increase of the wideband noise, for standards

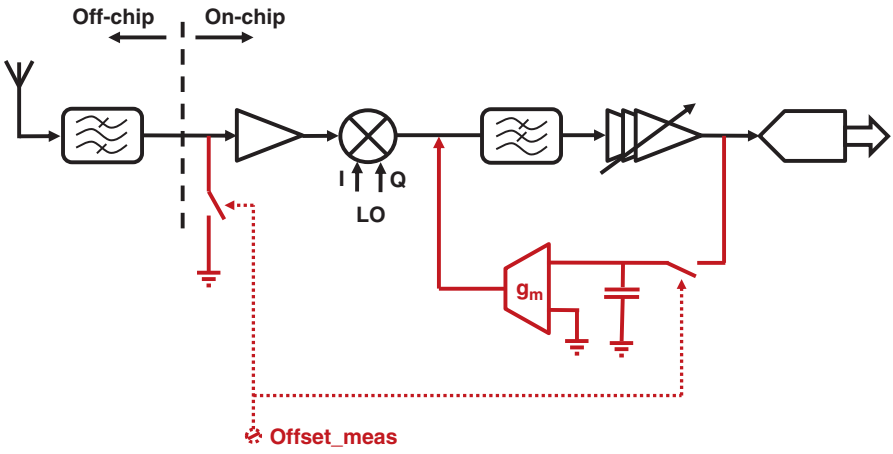

Fig. 2.10 Receiver block schematic with analog offset compensation (only one baseband channel is shown)

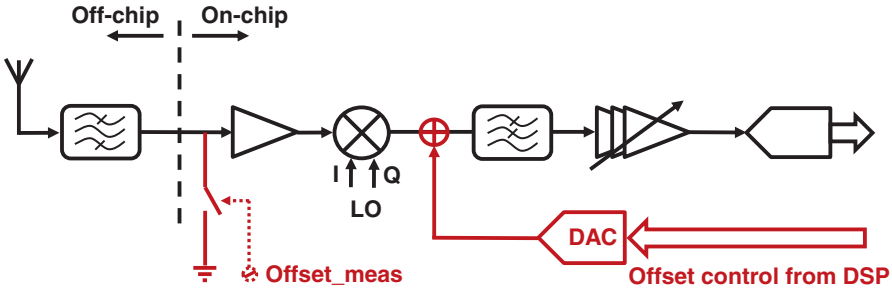

Fig. 2.11 Receiver block schematic with digital offset compensation (only one baseband channel is shown)

with a larger baseband bandwidth, regular AC coupling can be used for the LPF, while the DC offset compensation can be applied only to the VGA.

Another possibility for offset compensation is to measure the offset in the digital domain, and then correct it in the analog domain through a digital-to-analog converter (DAC). An example is shown in Fig. 2.11.

Handling Dynamic Offset

During the receiving period, the RF input power may change significantly, as the other transmitters in the receiver's neighborhood begin to transmit. The receiver's even-order distortions will change the received signal DC offset component. This *dynamic offset* effect disturbs the received signals demodulation, especially if the

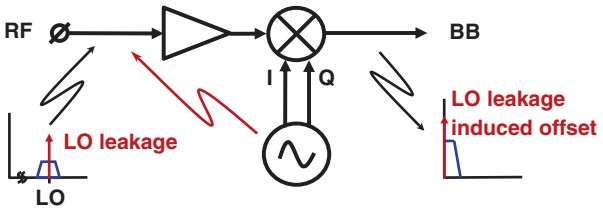

Fig. 2.12 DC offset generation due to self-mixing

envisaged modulation concentrates a large part of the symbol spectral power at low frequency.

Although the latest wireless standards use modulation schemes that do not require the preservation of the signal DC energy, this is not the case for older standards (i.e., GSM). Hence, handling dynamic offset implies the receiver must embed a fully differential signal conditioning chain that offers a high second-order input intercept point ($IIP2_{RX}$). The worst case scenario is met for the GSM standard which requires an $IIP2_{RX}$ of +46 dBm.

2.4.3 Reducing Self-Mixing

The self-mixing process occurs when the large swing LO signal, originating directly from the VCO, leaks to the antenna input, gets amplified by the LNA, and gets mixed with itself in the downconverter, as shown in Fig. 2.12. Hence, a large DC offset is produced at the mixer output. Subsequently, this may eventually clip the receiver output due to the large gain of the receiver baseband chain.

In order to overcome this issue, the VCO must not oscillate at the same frequency with the RF carrier frequency. Hence, the quadrature LO signals driving the downconverter mixer must be obtained by dividing down the VCO frequency. In order to generate good quality quadrature LO signals over a wide frequency band, the best option, relative to a multi-standard implementation, is to use a Johnson counter (e.g., [8]). For such quadrature generators, the VCO frequency must be at least twice of the desired LO frequency.

Thus, since the VCO is not oscillating at the wanted RF carrier frequency, the self-mixing offset is reduced considerably. There is still some residual self-mixing offset, as the divided quadrature LO signal leaks through the mixer switches gate-to-drain capacitance to its input. This offset is of same nature with the static offset, since it is only conditioned by the presence of the LO signal and not by the input signal. Thus, it can be calibrated out if the DC offset compensation loop is applied to the mixer's baseband stage as well.

2.4.4 Enhanced Receiver Schematic

Based on analysis presented in this section, Fig. 2.13 depicts the zero-IF radio receiver block schematic ready for monolithic integration in a re-configurable

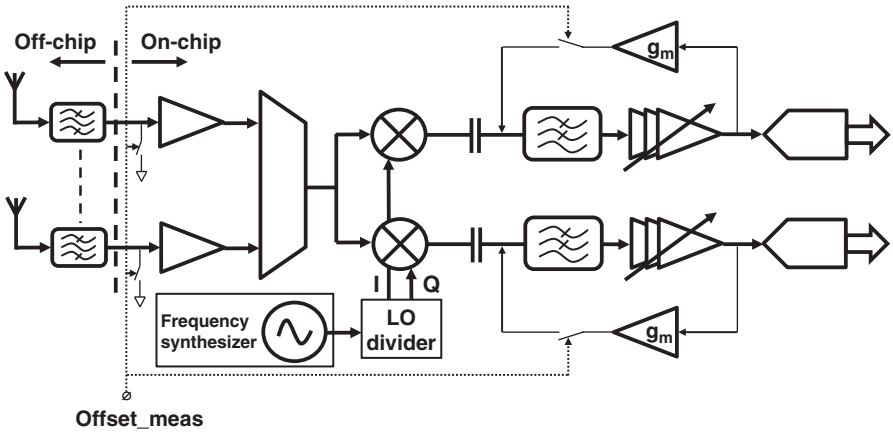

Fig. 2.13 SDRX block schematic embedding DC offset compensation and LO dividers

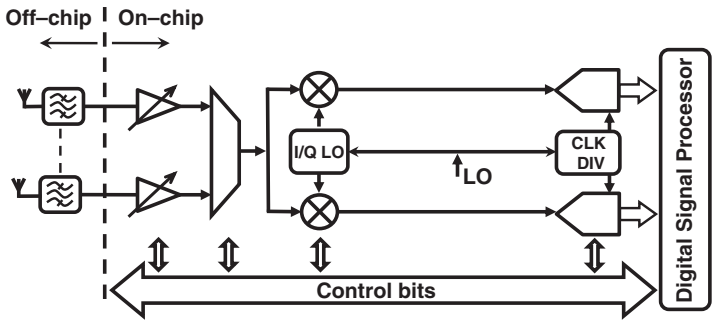

Fig. 2.14 Filter-less SDRX front-end

multi-standard radio transceiver. The schematic is the extension of the SDRX represented by Fig. 2.9. Moreover, the SDRX of Fig. 2.13 has the general characteristics specific to a true multi-standard solution.

2.4.5 Architectural Evolutions: Filter-Less and Mixer-Less Front-Ends

Given the latest trends in ADC dynamic range, sampling speed, and power efficiency improvement [9, 10], the first step in the evolution of Fig. 2.13 receiver is the elimination of the analog signal conditioning baseband chain, comprised by the LPF and VGA. Figure 2.14 depicts the filter-less SDRX front-end.

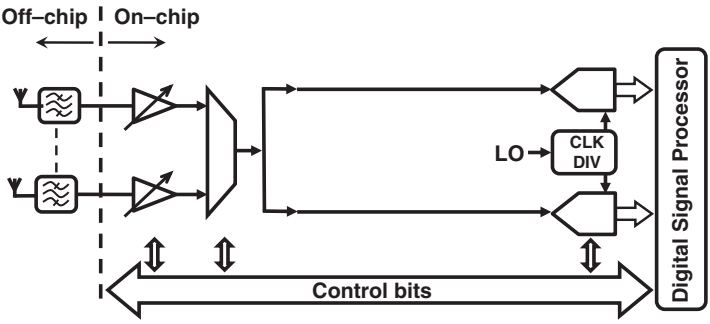

Fig. 2.15 Filter-less SDRX front-end

Of course, once the ADC conversion is performed, the filtering takes place in the digital domain.

Finally, there is another natural step to the evolution of Fig. 2.14 SDRX: the ADC engulfing the mixer as well. Thus, Fig. 2.15 depicts the direct sampling or mixer-less receiver. In this case, all signal processing takes place in the digital domain.

Hence, the designer is faced with three options:

(1) Mixer-based w/ analog baseband signal conditioning (Fig. 2.13)
(2) Mixer-based w/o analog baseband signal conditioning (Fig. 2.14)
(3) Mixer-less or direct sampling (Fig. 2.15)

Considering a given area and power budget, the optimal choice between the 3 options is given by the key trade-off shaping the SDRX design: the trade-off between the ADC power consumption and LPF area. This trade-off is evaluated in Chap. 4.

2.5 Conclusions

This chapter overviewed most common receiver architectures and concluded that direct conversion is the most suited option for a true SDRX. The major advantage is that it allows monolithic integration, since, unlike heterodyne and low-IF architectures, it has much lower image rejection requirements. Moreover, there is another significant advantage that simplifies the implementation from a multi-standard point of view, because the direct conversion topology has always the same IF: zero. Not to mention, in the case of direct conversion-based receiver, all baseband signal processing is done at the lowest possible frequency, and thus it has the lowest power consumption.

Further on, the direct conversion receiver architecture issues relative to the monolithic integration in a SDRX were analyzed. By implementing a DC offset compensation loop, the receiver static DC offset, and inherently $1/f$ noise, are calibrated out during the guard band. The dynamic offset is made negligible by implementing a fully differential receiver chain which offers a high $IIP2$. The self-mixing effects are alleviated by using a VCO oscillating at a different frequency than the RF carrier frequency, and wide-band frequency dividers to generate the quadrature LO signals.

Figure 2.13 depicts the enhanced SDRX schematic with DC offset compensation and wide-band quadrature dividers. Given the ADC performance increase, the natural trend leads to the ADC engulfing the analog baseband signal conditioning chain (see Fig. 2.14), and even the mixer (Fig. 2.15). The optimal choice between the 3 SDRX options is given by the key trade-off shaping the SDRX design: the trade-off between the ADC power consumption and LPF area. This trade-off is evaluated in Chap. 4.

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