

Chapter 1

Silicon Optical Interposers for High-Density Optical Interconnects

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Abstract One of the most serious challenges in the information industry is bandwidth bottlenecks in inter-chip interconnects. We proposed a photonics–electronics convergence system in response to this issue, demonstrated silicon optical interposers integrated with all optical components on a silicon substrate, and achieved a high bandwidth density of 30 Tbps/cm², which is sufficient for the needs of the late 2010s.

1.1 Introduction

1.1.1 Trends and Requirements of Computing Systems in Data Centers

First, we give an overview of the trends in computing systems mainly used in data centers, and point out requirements led by these trends. In the application layer, the most significant trend is data explosion. According to a report from IBM, 90 % of data in the world was created in the last 2 years alone [1]. This is a simple and impressive fact to understand the speed of the recent data explosion. The data explosion speed is expected to become faster due to the penetration of data analytics using “big data” and Internet of Things (IoT), because these applications will

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handle much bigger data sets than conventional web-searching or video-casting. Data centers are facing serious challenges to catch up with this data explosion. These trends are encouraging a shift to data-centric computing in data centers.

In the system layer, we believe that “disaggregation” of computing resources such as processors, memories, storages, and networks to make the system more flexible, scalable, and efficient is a notable new trend, as well as data-centric computing [2]. These trends require wider bandwidth and longer reach for interconnects between devices. The appearance of mega data centers also requires longer reach interconnects.

In the device/module layer, we point out three trends. First, although transistor size is still shrinking based on Moore’s law, its clock frequency has already hit the ceiling [3]. This trend is consequently requiring enhanced performance from many-core processors (MCPs) by means of parallelism. As a result, data quantity handling within a processor die is still growing. The second trend is three-dimensional (3-D) packaging, which has been mainly introduced for stacked memory modules such as Wide I/O 2 [4], high bandwidth memory (HBM) [5], and hybrid memory cube (HMC) [6], and successfully provides large capacity and wide bandwidth for inter-die (intra-module) interconnects by using through-silicon vias (TSVs). The 3-D packaging can be also applied to increase the capacity of non-volatile memory such as flash memory used as a solid-state drive (SSD), for data storage. As a result, data quantity handling within a memory module is also increasing. The third trend is system in a package (SiP) or multi-chip module (MCM), which consists of multiple chips in a single package and provides multiple functions with higher flexibility and shorter developing time than system on a chip (SoC). Generally, SiP can be implemented by 2.5-D packaging, where some bare dice are stacked vertically and some single chips or stacked dice are mounted side-by-side on an interposer. All of these three trends also require wider bandwidth for inter-chip interconnects.

1.1.2 Problems with Electrical Interconnects

Although wider bandwidth for inter-chip interconnects is required from application, system and device/module layers, the bandwidth of conventional inter-chip interconnects with electric wires is limited due to their low channel line rate and low input/output (I/O) pin density, namely low bandwidth density. For example, we estimate the required inter-chip bandwidth will be several tens of Tbps in the late 2010s, while LSI I/O pad pitches, such as flip-chip pad pitches, are expected to remain large at around 100 μm [7]. This is why the required line rate for inter-chip interconnects is estimated to exceed 40 Gbps by the late 2010s, and there are currently no known solutions to achieve the line rate with electrical interconnects on a printed circuit board (PCB) [7]. The reach of electric wires with a high channel line rate is also limited due to their high transmission loss on the PCB and reflections at connectors.

1.1.3 Optical Interconnects with Silicon Photonics

Optical interconnects with silicon photonics are potential candidates for solving the bandwidth bottleneck and limited reach problem and have been investigated [8–11]. We believe they have three major advantages. The first is the intrinsic properties of optical signals, such as wide bandwidth, low latency, low power consumption, and low mutual interference, compared with those of electrical signals. The second is the industrial advantages of silicon with which we can share the huge amount of existing resources in the electronics industry in terms of design, fabrication, testing, and supply chain. For example, we can use electronic design automation (EDA) tools and foundry services with 300-mm wafers for silicon photonics as with electronics. The common platforms between photonics and electronics also lead to high adaptability to photonics–electronics convergence. The third is the compactness due to their optical waveguides (OWs) with high refractive index contrast. The device compactness also leads to high performance in terms of speed and power consumption.

1.1.4 Vision for on-Chip Servers

Based on the examination of the above-mentioned trends, requirements, and problems of computing systems in data centers, we have propose a concept of an on-chip server in which the functions and performance of a present on-board server will be integrated on a substrate in the 2020s, as shown in Fig. 1.1 [12]. It is a kind of SiP or MCM. A 3-D MCP, 3-D memory (3-D Mem), and 3-D SSD are integrated on an interposer. While the vertical interconnects between stacked dice are electrical through TSV, horizontal interconnects between modules that consist of the stacked dice are mainly optical with silicon photonics. We call this system the photonics–electronics convergence system. More details are given in the following sections.

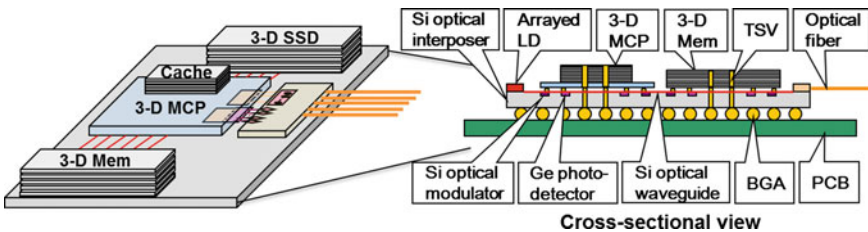


Fig. 1.1 On-chip servers based on silicon optical interposers

1.1.5 Photonics-Electronics Convergence System Technology (PECST) Project

To develop interconnects for future on-chip servers in Japan, the Photonics-Electronics Convergence System Technology (PECST) project was started in March 2010 as one of the 30 Funding Programs for the World-Leading Innovative R&D on Science and Technology (FIRST) projects supported by the Council for Science and Technology Policy in the Cabinet Office. This project was carried out for 4 years, mainly involving the University of Tokyo, Photonics Electronics Technology Research Association (PETRA), and Advanced Industrial Science and Technology (AIST). The PECST aimed to establish chip-to-chip interconnect technologies with a bandwidth density of 10 Tbps/cm². This chapter mainly describes the vision, methods, and achievements of the PECST project.

In Sect. 1.2 of this chapter, we first introduce our proposed photonics–electronics convergence system based on silicon optical interposers and in Sect. 1.3, we explain the configuration and characteristics of optical components for silicon optical interposers. Then, we discuss the evaluation of these optical interposers for high bandwidth density and wide temperature range operation in Sects. 1.4 and 1.5. Furthermore, we discuss the 25-Gbps data links using silicon optical interposers in Sect. 1.6 and the advanced fabrication and optical components for wider bandwidth in Sect. 1.7. Finally, we provide a perspective on inter-chip interconnects in Sect. 1.8 and conclude the chapter in Sect. 1.9.

1.2 Photonics–Electronics Convergence System for Inter-chip Interconnects

1.2.1 Optical Interconnects for Short Reach

Figure 1.2 shows the building blocks of optical interconnects, which consist of a light source, light distributor, electrical-to-optical (E/O) signal converter, optical wire, optical to electrical (O/E) signal converter, transmitter (Tx) circuits, and receiver (Rx) circuits. The photos in the figure show our optical components for examples of an arrayed laser diode (LD), silicon optical splitter (OS), silicon optical modulator (OM), silicon OW, and germanium photodetector (PD). With this system, light is not modulated directly by the light source, so the light source is not required to have high-speed operation but high output power is required for multichannel distribution. To build the integrated optical interconnects, we have to examine two integration methods, photonics–electronics integration and light source integration.

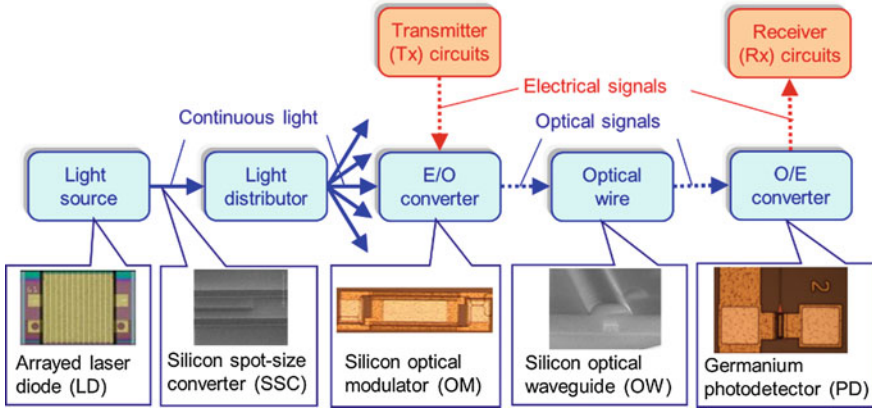


Fig. 1.2 Building blocks of optical interconnects

1.2.2 Integration Between Photonics and Electronics

Because the performance of electrical interconnects generally declines more rapidly with their distance than does that of optical interconnects, it is important to place optical transceivers (E/O and O/E signal converters) as close to large-scale integration (LSI) chips as possible for wide-bandwidth inter-chip interconnects with photonic wiring. Silicon photonics is the most suitable technology for these applications because of its compactness and compatibility with LSIs.

Generally, there are three types of integration methods between photonic and electronic circuits with silicon photonics. Their schematic cross sections are shown in Fig. 1.3: front-end integration, back-end integration, and flip-chip bonding. In front-end integration, both electronic and photonic circuits are integrated near the surface of a silicon substrate by a front-end process. In back-end integration, photonic circuits are integrated on the wiring layer by a back-end process. In flip-chip bonding, electronic and photonic chips are fabricated separately then stacked by flip-chip bonding. The first two are monolithic integrations and the last is a hybrid integration. The characteristics of these integrations are compared in Table 1.1. Monolithic integration, especially front-end integration, is expected to provide higher speed and lower assembling cost than hybrid integration, but it requires very strict CMOS compatibilities in terms of design, fabrication, and testing. We believe that it will be a long time before the technology is mature enough. In contrast, hybrid integration enables us to individually choose the most suitable technology nodes for photonic and electronic circuits, to design, fabricate and test them separately, and then combine their good dies. This scheme can improve product yields and stimulate horizontal specialization between electronics and photonics or between LSI chips and their inter-chip interconnects. Therefore,

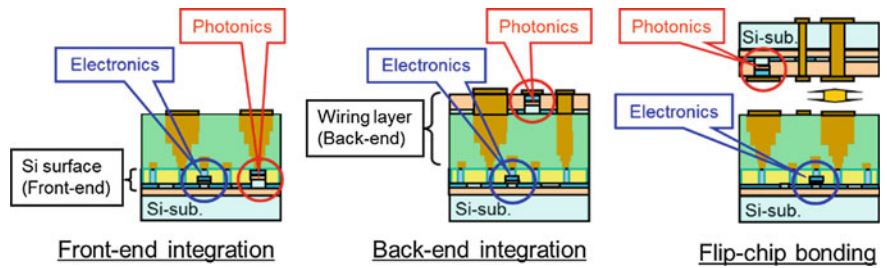


Fig. 1.3 Schematic cross sections of integration between photonic and electronic circuits

Table 1.1 Comparison of photonics–electronics integration methods

Integration type	Monolithic		Hybrid
	Front-end integration	Back-end integration	Flip-chip bonding
Operation speed	Higher	Lower	Lower
Assembly cost	Lower	Lower	Higher
Wafer process cost	Higher	Intermediate	Lower
Challenge for integration	Harder	Harder	Easier
Available waveguide	SOI, bulk-Si	SiN, a-Si	SOI

since we believe that hybrid integration is the most practical choice both now and in the near future, we have taken the hybrid-integration route to photonic–electronic integration for inter-chip interconnects.

1.2.3 Light Source Integration

Generally, light sources for high-density inter-chip interconnects are classified, as shown in Fig. 1.4. First, when considering the light source arrangement in our inter-chip optical interconnects, we have to choose between off-chip or on-chip sources. Although off-chip light sources are the more flexible of the two, they require highly precise optical connectors and care regarding polarization dependence to deliver optical power from the off-chip light sources into the substrate via optical fibers. Because we believe that this is not practical for large-scale interconnects, we chose on-chip light sources, which require neither optical connectors nor special care regarding polarization dependence. Although on-chip light sources are often affected by heat generated by LSIs mounted near the light sources, we

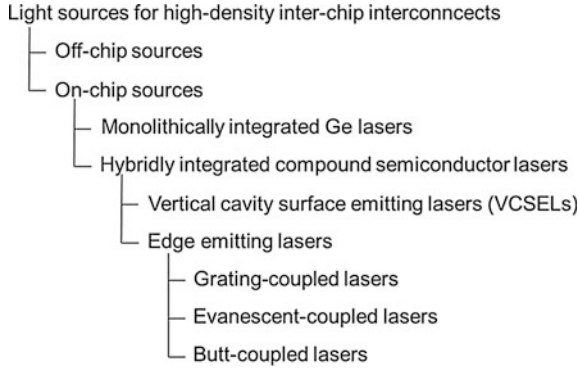


Fig. 1.4 Classification of light sources for high-density inter-chip interconnects

introduce a solution for this problem, as mentioned in Sect. 1.5. There are two types of integration for on-chip light sources: monolithic integration with germanium lasers and hybrid integration with compound semiconductor lasers. Because the efficiency and output power of monolithically integrated Ge-on-Si lasers are still low for inter-chip interconnect applications [13], we chose hybridly integrated lasers. There are two types of compound semiconductor lasers for optical interconnects: edge-emitting lasers and vertical cavity surface emitting lasers (VCSELs). Because VCSELs cannot maintain single-mode operation when the optical output is high, we chose edge-emitting lasers. There are also three types of edge-emitting lasers in terms of optical coupling structures between active OWs in the LDs and silicon OWs: grating-coupled lasers [14], evanescent-coupled lasers [15], and butt-coupled lasers [16]. The grating-coupled laser is a subassembly module, in which an LD, ball-lens, isolator, and 45° mirror are packaged in a hermetic silicon housing [14]. Although this method is highly reliable and tolerant of optical feedback, the module is much bigger than bare LD chips in the following methods. It is difficult to apply an arrayed LD chip for scale-out. The evanescent-coupled lasers have higher tolerance against alignment error when the compound semiconductor chips are mounted on the silicon substrate than the butt-coupled lasers do. However, we found that the bandwidth density and power consumption per channel in LDs can be improved using a branching configuration, in which the light from a single LD is divided and distributed to many channels [17], and we believe the efficiency and output optical power of the evanescent-coupled lasers are not high enough for the branching configuration. We therefore chose to use butt-coupled hybrid lasers for inter-chip interconnect applications and developed spot-size converters (SSCs) between LDs and silicon OWs to relax the alignment tolerance, as mentioned later.

1.2.4 Photonics–Electronics Convergence System with Silicon Optical Interposers

Based on the above examinations, we propose a photonics–electronics convergence system for inter-chip interconnects [12, 18]. A conceptual model of the system is shown in Fig. 1.5. This model is designed to provide optical interconnects among four LSI bare chips on a silicon substrate. The upper-left LSI chip on the silicon substrate has been removed to enable the substrate surface area that it covered to be seen. OMs and PDs are monolithically integrated on the silicon substrate under the LSI bare chips. Since high-speed I/O ports of an LSI are usually laid out near edges of the LSI die, OMs and PDs are laid out in the corresponding areas on the silicon substrate. The LSI bare chips are mounted on the substrate using flip-chip bonding and are electrically connected to the OMs and PDs. Arrayed LDs are hybridly integrated on the substrate. The LDs, OMs, and PDs are optically linked to each other by silicon OWs and OSs. We call the silicon substrate a “silicon optical interposer.”

The inter-chip interconnects with the silicon optical interposers operate as follows. Arrayed LDs are driven simultaneously by direct currents (DCs). The CW light from each LD is divided by an OS and launched into an OM. OMs are directly driven by Tx circuits in one LSI. The modulated optical signals propagate along inter-chip OWs and are the input for PDs under another LSI. The electrical signals from those PDs are the input for Rx circuits in the LSI that the PDs are under.

This system enables us to replace conventional electronic wires on a PCB with the optical interconnects on a silicon substrate, which is about one hundredth the size of a PCB. Such silicon optical interposers have wide-bandwidth capabilities due to the properties of their optical signals. Since the silicon substrates can be fabricated using a CMOS-compatible process, they have quite high density and are low in cost. Furthermore, because this system is optically complete and closed without any optical inputs or outputs, users do not have to worry about optical issues, such as optical coupling, optical reflection, or polarization dependence. The hybridly integrated LDs are capable of high optical output power and a

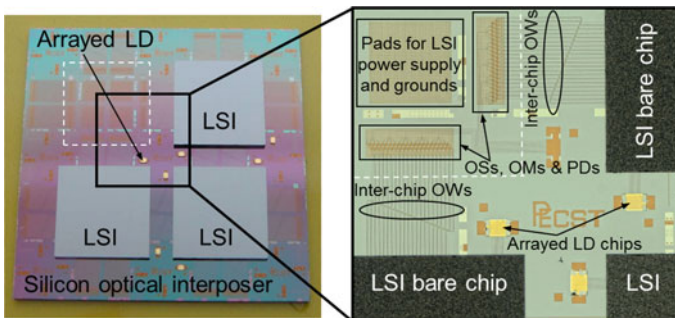


Fig. 1.5 Conceptual model of photonics–electronics convergence system

multichannel distribution. The hybrid integration between photonics and electronics allows us to individually choose the most suitable technology nodes for the photonics and electronics, respectively.

1.3 Configuration and Characteristics of Optical Components for Silicon Optical Interposers

To confirm the feasibility of our photonics–electronics convergence system, we discuss high-density silicon optical interposers that mainly consist of silicon OWs, hybridly integrated on-chip light sources, silicon OMs, and germanium PDs. The configurations and characteristics of these optical components were investigated as follows.

1.3.1 Silicon Optical Waveguides

Generally, there are two types of silicon OWs in terms of their core cross-section shapes: rib-shaped and rectangular. Their cross sections and characteristics are compared in Table 1.2. The propagation loss of the rib-shaped OWs is lower than that of the rectangular ones, but the rib-shaped OWs pose difficulties in the fabrication process in that we have to stop etching the silicon layer to leave a precisely thin silicon slab. We believe this issue is critical in terms of yields in mass production, especially (as will be explained later) for yields of OMs. We therefore chose rectangular core OWs for our silicon optical interposers.

To reduce the relatively high propagation loss of the rectangular core OWs, we developed fine fabrication processes that mainly consist of a multiple exposure technique in variable-shaped-beam (VSB) electron beam (EB) lithography, and optimization of EB resist and etching processes. By applying these techniques, the field stitching error and line edge roughness (LER) are drastically reduced to 7.9 and 1.9 nm, respectively [19]. Figure 1.6 shows the core width dependence of the propagation loss for the TE-like mode at 1550-nm wavelength. The core height is 220 nm. The propagation losses are nearly constant and less than 2 dB/cm

Table 1.2 Comparison of silicon optical waveguides

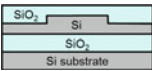
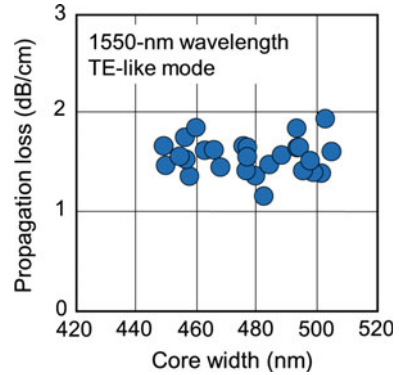
Core type	Rib-shaped	Rectangular
Core cross section		
Propagation loss	Lower	Higher
Etching process	More difficult	Easier
Spot-size converter	More difficult	Easier

Fig. 1.6 Core width dependence of propagation loss



regardless of their core width. Such small core width dependence implies that the scattering loss caused by the side-wall roughness is negligible in our rectangular core OWs. The losses are comparable to those of rib-shaped OWs.

1.3.2 Hybridly Integrated On-Chip Light Sources

1.3.2.1 Arrayed Laser Diodes

Figure 1.7a shows a microscope image of a 13-channel arrayed LD chip (bottom side) to be mounted on the silicon optical interposers. It is an InGaAsP quantum-well LD array emitting 1530-nm wavelength light. Each channel is a Fabry–Perot-type LD with a spot-size converter [16]. The cavity length is 400 μm . The arrayed LD chip has a single common pair of electrodes for all 13 channels that simultaneously emit light by a single input current. This common electrode structure enables a narrow channel pitch of 30 μm . The chip also has a pair of alignment marks used for a passive alignment technique [20]. The near field pattern and output intensity of the 13-channel arrayed LDs are shown in Fig. 1.7b. The output power uniformity across all channels is better than 0.7 dB.

The measured wall-plug efficiency (WPE) of the LDs at room temperature is shown in Fig. 1.8. When the LD output is low enough, power consumption under a lasing threshold is dominant, and the efficiency is low. On the other hand, when the LD output is high enough, the output is saturated by heat and the efficiency decreases. As a result, the highest WPE of 35 % is obtained around 14 dBm of output power per channel. Therefore, we set the LD output power around 14 dBm to maximize the WPE in the data link experiments mentioned in Sect. 1.4.

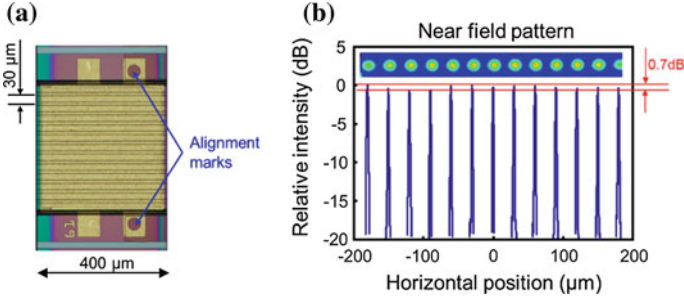
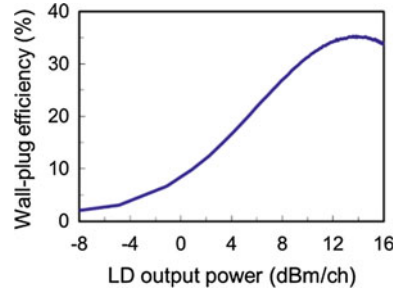


Fig. 1.7 13-channel arrayed laser diodes. **a** Microscope image of bottom side. **b** Near field pattern and output intensity

Fig. 1.8 Measured wall-plug efficiency of laser diodes at room temperature



1.3.2.2 Spot-Size Converters

Spot-size converters between the LDs and silicon OWs are key components for the silicon optical interposers in terms of their optical power budget and fabrication process simplicity. We previously used three types of SSCs: tapered silicon OW, inversed taper silicon OW, and SiON OW. Although the first two did not require additional processes, the first had a large coupling loss [18] and the second had a very small process margin, as will be discussed later. The third type had a low coupling loss but required additional processes [16]. We subsequently introduced a novel SSC called a trident [21], the schematic structure and scanning electron microscope (SEM) images of which are shown in Fig. 1.9. It consists of only three narrow silicon OWs fabricated without additional processes.

The measured coupling losses of the trident SSCs and a conventional inversed taper SSCs with various tip widths are shown in Fig. 1.10a. The coupling loss of the trident SSCs is low and insensitive to its tip width, unlike the inversed taper SSCs. This is because the spot size of the trident SSCs does not mainly depend on its tip width but mainly on its tip pitch. The line pitch is usually less sensitive to fabrication errors than the line width. Therefore, the trident SSCs are tolerant of fabrication errors. The measured coupling losses between the LDs and trident SSCs with various alignment deviations in the horizontal and vertical directions are plotted in

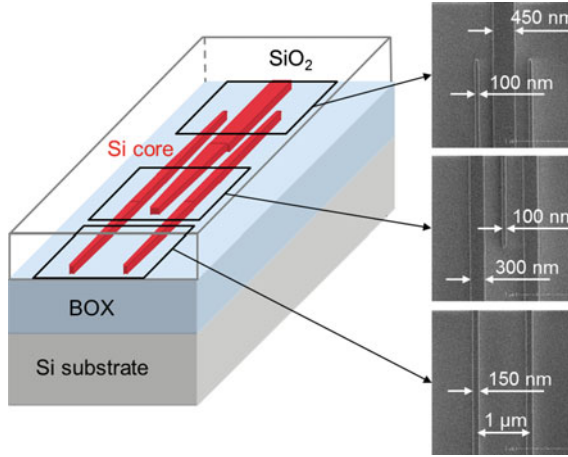


Fig. 1.9 Schematic structure and scanning electron microscope images of trident spot-size converters

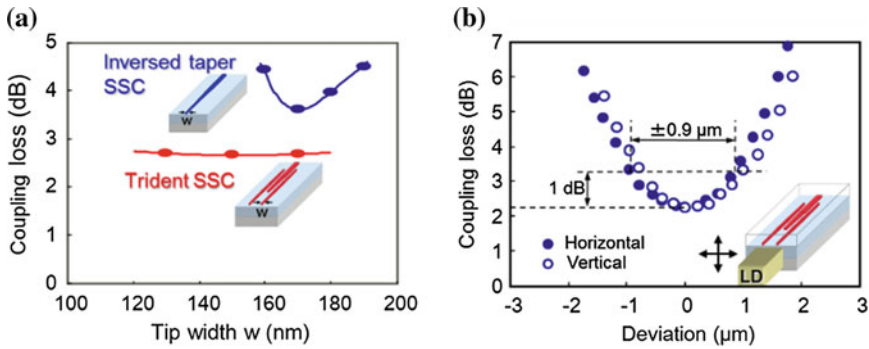


Fig. 1.10 Measured characteristics of trident spot-size converters (SSCs). **a** Coupling losses of trident SSCs and conventional inversed taper SSCs with various tip widths. **b** Alignment tolerance between laser diodes and trident SSCs in horizontal and vertical directions

Fig. 1.10b. The minimum coupling loss is as low as 2.3 dB, and the alignment error tolerance up to a 1-dB loss increase is about $\pm 0.9 \mu\text{m}$ in both directions, which is large enough for our alignment precision ($\pm 0.5 \mu\text{m}$) with a passive alignment technique [20].

1.3.2.3 Flip-Chip Bonding of Arrayed LD Chip

To form a hybridly integrated on-chip light source, an arrayed LD chip is flip-chip bonded to a silicon substrate with a passive alignment technique, as schematically shown in Fig. 1.11. The LD chip is vertically aligned just by mounting it on the

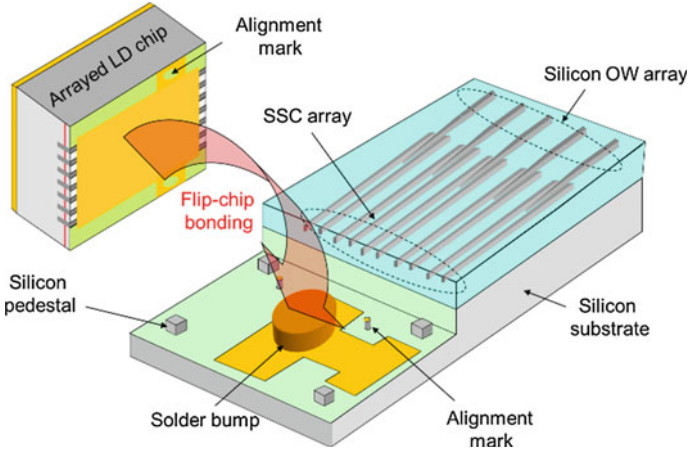


Fig. 1.11 Flip-chip bonding of arrayed laser diode chip to silicon substrate with passive alignment technique

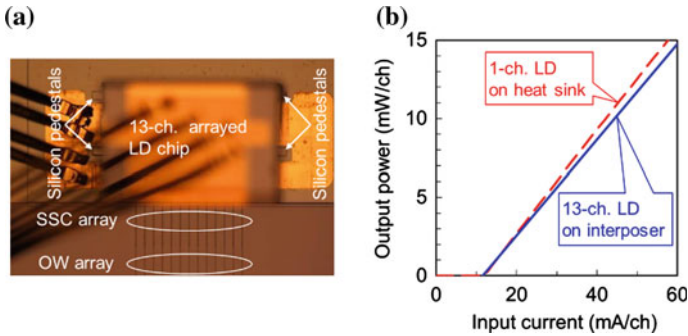


Fig. 1.12 Thirteen-channel arrayed laser diodes (LDs) mounted on silicon optical interposers. **a** Microscope image of *top*. **b** Measured per-channel I - L characteristics of 13-channel arrayed LD mounted on interposer and one-channel LD mounted on heat sink. Both were measured without temperature control

silicon pedestals, and it is horizontally aligned by overlapping the alignment marks on the bottom of the LD chip and the silicon substrate. Then the LD chip is fixed and electrically and thermally contacted to the substrate with the AuSn solder bumps. This structure enables low thermal resistance between the LD chip and silicon substrate [22]. As a result, the LD array is butt-coupled to the silicon OW array via the SSC array.

Figure 1.12a shows a microscope image of a 13-channel arrayed LD flip-chip mounted on a silicon optical interposer. The measured per-channel I - L characteristics of the LDs without temperature control are plotted in Fig. 1.12b, where the solid line indicates the I - L characteristics of the 13-channel arrayed LD hybridly integrated on

the interposer and the broken line indicates those of a 1-channel LD mounted on a heat sink. Since all 13 channels are driven simultaneously, the actual current injected into the whole arrayed LD chip is 13 times the value in the horizontal axis. Although the heat generation in the 13-channel LD is 13 times as high as that in the 1-channel LD, both I - L characteristics have about the same threshold currents and slope efficiencies, and there are no output power saturations up to 15 mW or higher per channel. This suggests that the hybridly integrated arrayed LD exhibits no degradation due to its high-density array and quite a high heat dissipation capability. We consider these high output power and high heat dissipation capabilities to indicate the superiority of our butt-coupled hybrid lasers over evanescent-coupled ones [22].

1.3.3 Silicon Optical Modulators

There has been extensive research on silicon OMs using the carrier plasma effect in PIN or p-n diodes, most of them focused on using a doped silicon slab in the rib-shaped OWs to make electric contact between the OW core and metal electrodes [23–25]. In these cases, the gaps between P- and N-doping areas should be wider than the width of the optical mode profiles to prevent optical absorption loss due to the highly doped carriers. The optical mode profiles in these rib-shaped OWs extend to the slab areas, and a thicker slab causes a wider mode profile and P-N gap. The wider P-N gaps increase resistivity and decrease modulation efficiency and modulation speed. Because OM characteristics such as optical loss, modulation efficiency, and speed are sensitive to the slab thickness in this way, we have to stop etching the silicon layer to leave a precisely thin silicon slab. To overcome these design and fabrication difficulties, we propose a novel structure for the electric contact between the OW core and electrodes to be used instead of the silicon slab. Figure 1.13a shows a schematic of the structure of our proposed OM [26], which is a Mach–Zehnder interferometer (MZI) composed of phase shifters and multimode

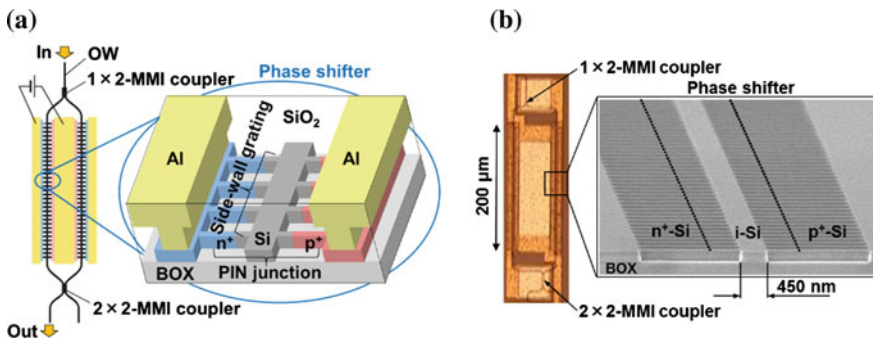
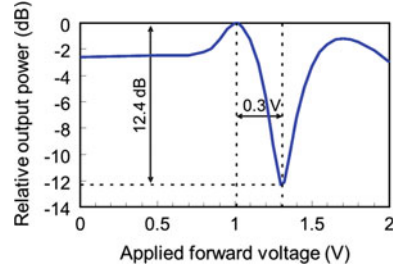


Fig. 1.13 Silicon optical modulators (OMs) with side-wall gratings. **a** Schematic structure. **b** Microscope and scanning electron microscope images of fabricated OMs

Fig. 1.14 Measured direct current response of optical modulators



interference (MMI) couplers. The phase shifters, which have side-wall gratings on both sides of the OW core to enable electric contact between the core and metal electrodes, can change their refractive indices by the carrier plasma effect in lateral PIN diode structures. Figure 1.13b shows microscope and SEM images of the fabricated OM. Because the OWs and side-wall gratings have a uniform thickness of silicon over the entire OM, the etching process to form the OWs and side-wall gratings is much easier than that to form rib-shaped OWs. Moreover, this structure enables stronger lateral optical mode confinement, narrower optical mode profile, narrower P-N gap, lower resistivity, higher efficiency, and higher speed than the OMs with rib-shaped OWs. The pitch of the side-wall gratings is 285 nm, which is designed so that their stop-band wavelength is much shorter than the operation wavelength to prevent diffraction by the gratings. The interaction length of the phase shifter (L) is 200 μm .

The measured DC response of our OM is plotted in Fig. 1.14. The π -phase shift voltage ($V\pi$) is 0.3 V and the modulation efficiency ($V\pi \cdot L$) is 0.006 Vcm, which is twice as high as the efficiency of our previous OM with rib-shaped OWs [18]. The extinction ratio is 12.4 dB. Since the frequency response of the OM is similar to that of a series resistor–capacitor (RC) circuit, we used pre-emphasis to compensate for the frequency response. The 3-dB bandwidth with pre-emphasis is estimated to be 12.5 GHz [26].

1.3.4 Germanium Photodetectors

There are generally two types of germanium PDs that we can monolithically integrate on a silicon substrate: PIN-PDs and metal-semiconductor-metal (MSM) PDs [27]. The MSM-PDs require fewer fabrication steps but finer patterning and alignment than PIN-PDs. For this work we chose PIN-PDs for the silicon optical interposers. Figure 1.15a shows a schematic cross section of our germanium PIN-PDs and Fig. 1.15b shows an SEM image. The measured frequency responses of the PDs with 0-, 1-, and 2-V biases are plotted in Fig. 1.16. The 3-dB cutoff frequencies are 10 GHz with a 0-V bias voltage and 26 GHz with a 1-V bias voltage. The dark current is about 1 μA with a 1-V bias voltage.

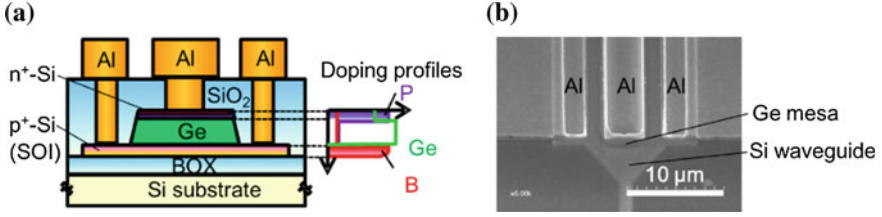
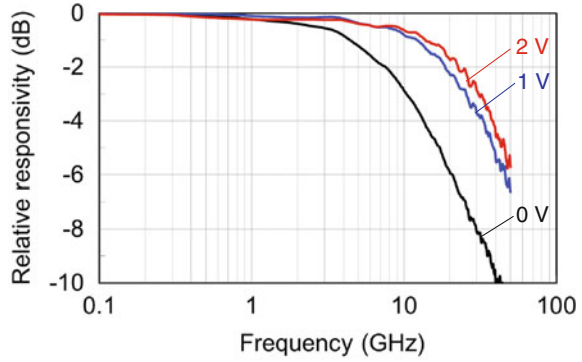


Fig. 1.15 PIN-type germanium photodetectors. **a** Schematic cross section. **b** Scanning electron microscope image

Fig. 1.16 Frequency responses of PIN-type germanium photodetectors



1.4 Silicon Optical Interposers for High Bandwidth Density

1.4.1 Design Consideration for Bandwidth Density and Optical Power Budget

As mentioned earlier, LSI bare chips are supposed to be mounted on the interposers using flip-chip bonding. The ITRS projections have indicated that the pitches of flip-chip pad arrays should stop shrinking at around 100 μm [7]. Therefore, we designed our silicon optical interposers so that the pad pitches of the OMs and PDs were 100 μm .

We found that the LD power consumption per channel can be improved by using a branching configuration, in which the light from a single laser is divided and distributed to many channels, because the power consumption under lasing threshold is shared by many channels [17]. Since the wall-plug efficiency of the LD is at a maximum around 14-dBm LD output, as shown in Fig. 1.8, we designed optical links of our silicon optical interposers by using the branching configuration so that the LD output was about 14 dBm for maximum energy efficiency. Since we expected that we had a margin of about 6 dB in the optical link power budget, we introduced 1×4 MMI couplers as OSs for the branching configuration.

1.4.2 Integrated Fabrication Process

The fabrication processes of our silicon optical interposers are listed in Fig. 1.17. The silicon optical interposers were fabricated from 4-inch silicon-on-insulator (SOI) wafers in the Super Clean Room at AIST Tsukuba West by CMOS process technology. The thicknesses of the buried oxide layer and the SOI layer were 3 μm and 220 nm, respectively. The silicon OW cores, as well as trident SSCs, 1×4 MMI couplers, MZIs, and side-wall gratings for the OMs were formed by VSB-EB lithography and dry etching. Lateral PIN junctions for the OMs and vertical ones for the PDs were formed by B and P ion implantations. Epitaxial germanium mesas for the PDs were selectively grown on the silicon cores by chemical vapor deposition (CVD). All the components were covered with a SiO_2 upper cladding layer by CVD. Contact holes were formed by dry etching. Electrodes and solder bumps for LDs were formed on the bottom. Finally, the arrayed LD chips were mounted on the pedestals using a passive alignment technique [20].

Microscope images of one of our fabricated silicon optical interposers are shown in Fig. 1.18 [28]. The substrate is 4.7×4.5 mm. Two 13-channel arrayed LD chips are hybridly integrated on the silicon substrate, and 26 trident SSCs, 26 1×4 OSs, 104 OMs, 104 inter-chip Ows, and 104 PDs are monolithically integrated on the substrate. Unit cells of the OMs and PDs are 400×100 μm and 200×100 μm , respectively. They are tiled so that their pad pitches are 100 μm . Two LSI bare chips are supposed to be mounted on the right and left sides of the substrate using flip-chip bonding to be optically connected to each other.

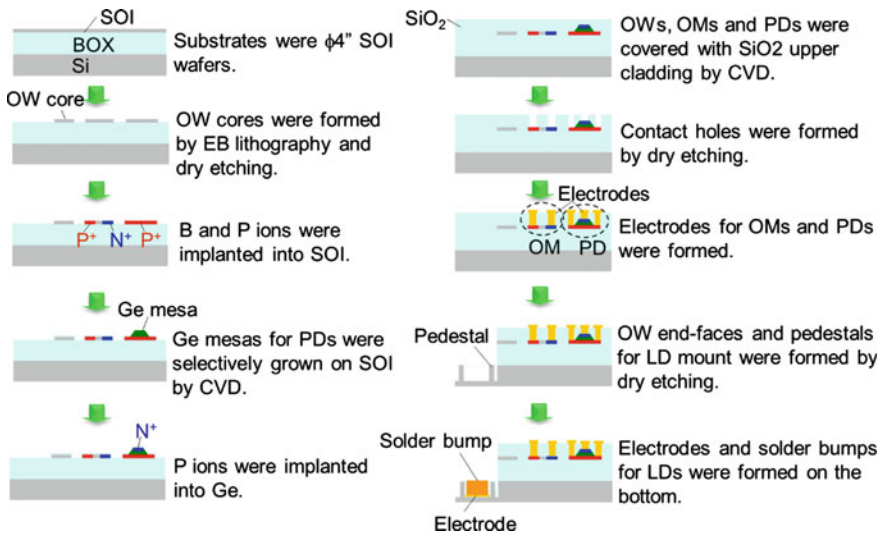


Fig. 1.17 Fabrication process of silicon optical interposers

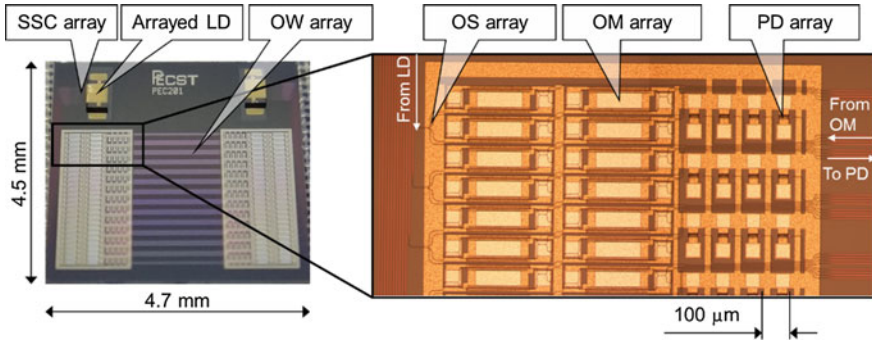


Fig. 1.18 Microscope images of fabricated silicon optical interposers

1.4.3 Data Link Experiments

We conducted data link experiments as follows. All 13 channels of an arrayed LD were simultaneously driven by a single DC current. The CW light from the LD was a wavelength of 1530 nm and a TE-like mode. It was coupled to a silicon OW by a trident SSC and then divided into four by a 1×4 OS and each of them was launched into a OM. The radio frequency (RF) input signals were pre-emphasized by a differentiator composed of passive RC circuits and drove the OM. The voltage amplitude after pre-emphasis was 3.5 V peak to peak. The modulated optical signals propagated along an inter-chip OW and were then input to a PD and converted into electrical signals.

The measured eye diagram of the PD output at 20-Gbps NRZ with a 2^7-1 pseudo-random binary sequence (PRBS) is shown in Fig. 1.19a. The clear eye opening indicates that the optical links are capable of a 20-Gbps data link. The measured bit error rates (BERs) for the 20-Gbps PRBS are plotted in Fig. 1.19b. We confirmed that the BER was less than 10^{-12} when the received power of the PD was larger than -5 dBm. An error-free data link at 20 Gbps via the 1×4 OS was achieved. These results demonstrate that the silicon optical interposers are capable of a 2.1-Tbps bandwidth for inter-chip optical interconnects.

To evaluate inter-channel crosstalk, we also demonstrated four-channel simultaneous operation. Because we did not have the equipment for 4×20 Gbps simultaneous operation, we did it with 4×12.5 Gbps. Figure 1.20a shows BERs of four individual channels when the four channels simultaneously operated. We confirmed four-channel simultaneous error-free operation. Figure 1.20b shows the BERs of a particular channel with (circles and solid line) and without (triangles and broken line) simultaneous operations of the other three channels. Because the BER difference is very small, we believe the power penalty due to the inter-channel crosstalk was negligible in these data link experiments.

The per-channel optical power budget of the data link experiments when the error-free data links were achieved is summarized in Table 1.3. The optical output

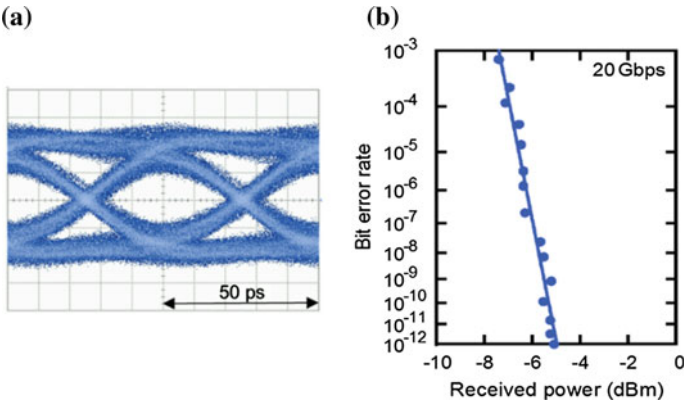


Fig. 1.19 Photodetector outputs of data link experiments at 20 Gbps. **a** Eye diagram. **b** Bit error rates

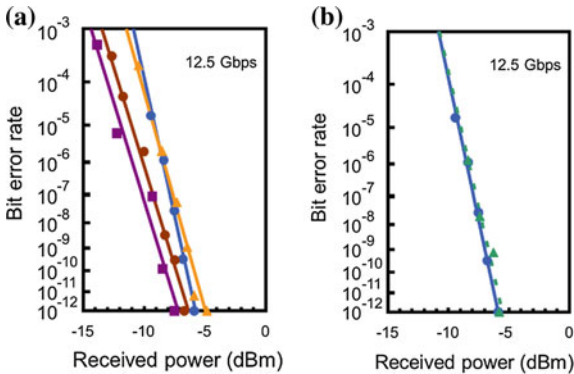


Fig. 1.20 Bit error rates (BERs) in four-channel simultaneous operation. **a** BERs of 4 individual channels when the 4 channels operated simultaneously. **b** BERs of a particular channel with (circles and solid line) and without (triangles and broken line) simultaneous operations of the other 3 channels

Table 1.3 Per-channel optical power budget of data link experiments

Item	Power (dBm)	Loss (dB)
LD output power	13.0	–
LD to OW coupling loss	–	2.3
Inherent 1 × 4 branching loss	–	6.0
1 × 4 OS excess loss	–	0.5
Inherent modulation loss	–	3.0
OM excess loss	–	2.8
OW propagation loss	–	2.2
Other losses	–	1.2
PD input power	–5.0	–

Table 1.4 Footprints of optical components per channel

Optical component	Footprint (mm ²)
Laser diode (LD)	0.0077
Optical modulator (OM)	0.0400
Photodetector (PD)	0.0200
Total	0.0677

power from the LD was 13 dBm, where the WPE of the LD was a maximum, as mentioned in the previous section, and the optical input power to the PD was -5 dBm. Therefore, the overall optical loss was 18 dB, including an inherent 6-dB branching loss and a 3-dB modulation loss.

1.4.4 Significance of Bandwidth Density

The footprints of the optical components per link channel are listed in Table 1.4. The total footprint was 0.0677 mm^2 per channel, meaning we could achieve a high bandwidth density of 30 Tbps/cm^2 with a channel line rate of 20 Gbps. Since LSI bare chips are supposed to be mounted on the silicon optical interposers by flip-chip bonding, as shown in Fig. 1.5, and the footprints of the optical components and Tx and Rx electrical circuits overlap, we believe the overall bandwidth density with the electrical circuits is similar to that of optical components. To our knowledge, this was the highest bandwidth density for an inter-chip optical interconnect. Since the maximum lithography field size (stepper shot size) in area and signal I/O pad percentage out of total pads for CPUs have currently been 8.58 cm^2 and 33 % respectively and will be so in the future [7], we can obtain an overall inter-chip bandwidth at the level of several tens of Tbps by using silicon optical interposers, which is sufficient for the required bandwidth in the late 2010s or early 2020s.

The footprints of the OMs and PDs mainly depend on their pad pitches, which were $100 \text{ }\mu\text{m}$ in this case. Therefore, we believe that it is possible to reduce their footprints with smaller pad pitches, by one-fourth with a $50\text{-}\mu\text{m}$ pitch for example.

Since this system is optically complete and closed and no temperature sensitive components are used, we did not need to align the fibers, control the polarization, or control the temperature throughout the experiments.

1.5 Silicon Optical Interposers for Wide Temperature Range Operation

In the previous section, we discussed silicon optical interposers fully integrated with the optical components on a silicon substrate, achieving a high bandwidth density of 30 Tbps/cm^2 at room temperature. For practical applications, interposers

should be usable under high temperature conditions and rapid temperature changes without complex feedback controls, namely athermal, so that they can cope with heat generated by the mounted LSIs. Since the LSI bare chips are mounted near LDs, as shown in Fig. 1.5, the LDs are expected to be affected by the heat. Because the output power of conventional LDs usually declines as temperature rises, the system requires temperature-insensitive LDs.

Quantum dot LDs (QD-LDs) are expected to be used under these thermally severe conditions because of their output power characteristics with low temperature sensitivity [21, 29–32]. Although QD-LDs monolithically integrated on silicon substrates by heteroepitaxy or wafer bonding have been reported, their characteristics and reliability have not been enough for applications due to the large lattice mismatch and thermal expansion coefficient difference with the silicon substrate [30–32]. We previously reported that QD-LDs hybridly integrated on silicon substrates were suitable for high-density and heat-tolerant optical interconnect applications [21]. Even if we use QD-LDs as on-chip light sources, lasing wavelength shifts due to temperature variation are unavoidable. Therefore, the other optical components integrated with QD-LDs should be not only temperature insensitive but also wavelength insensitive over the whole wavelength range where the lasing wavelength shifts upon changes in temperature.

In this section, we describe our athermal silicon optical interposers hybridly integrated with QD-LDs and monolithically integrated with other temperature- and wavelength-insensitive components on a silicon substrate. We discuss the error-free data link performance with the interposers over a wide temperature range without adjusting their biases or signals.

1.5.1 Hybridly Integrated Athermal Light Sources and Their Thermal Characteristics

Our 13-channel arrayed LD chips for the athermal silicon optical interposers were fabricated by QD Laser, Inc. Figure 1.21a shows a microscope image of a 13-channel arrayed QD-LD chip (bottom side) to be mounted on athermal silicon optical interposers. Each channel is a Fabry–Perot-type LD emitting around 1310-nm wavelength light [21]. The cavity length is 600 μm . The arrayed QD-LD chip has a single common pair of electrodes, the same as the arrayed QW-LD mentioned in Sect. 3.2.1. The channel pitch is also 30 μm . The chip also has a pair of alignment marks used for a passive alignment technique [20]. The measured per-channel current-light output power (I – L) characteristics of the QD-LDs on a heat sink at various temperatures are shown in Fig. 1.21b [38]. The QD-LDs can maintain their output power higher than 10 mW per channel up to 100 $^{\circ}\text{C}$. The measured temperature dependence of the threshold current is shown in Fig. 1.22a. Temperature sensitivity of the threshold current is low, and the characteristic temperature is 114 K from 25 to 120 $^{\circ}\text{C}$. The measured temperature dependence of

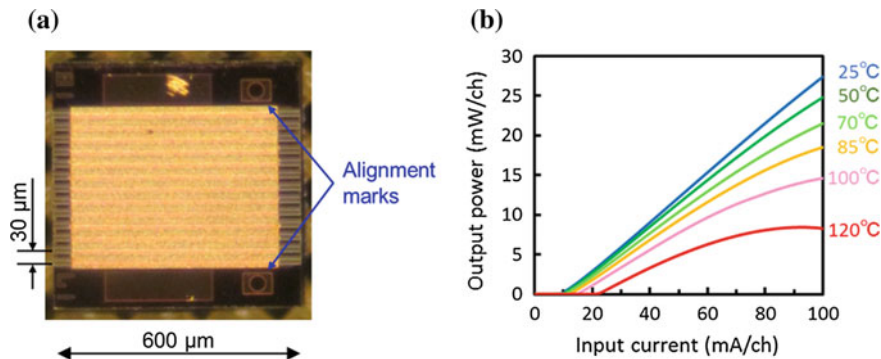


Fig. 1.21 Thirteen-channel arrayed quantum dot laser diodes (QD-LDs). **a** Microscope image of bottom side. **b** Measured per-channel current–light output power (I – L) characteristics of QD-LD on a heat sink at various temperatures

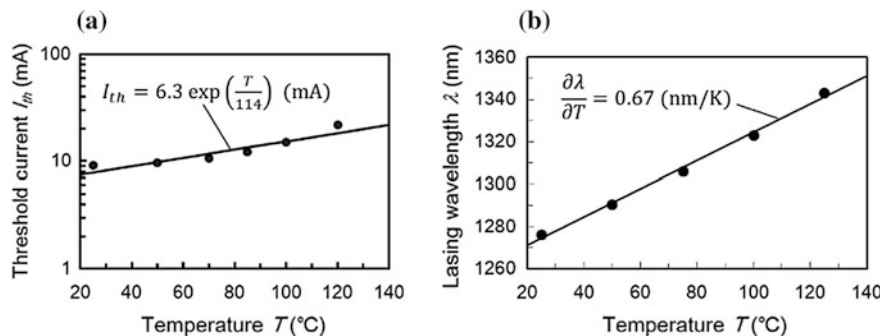


Fig. 1.22 Measured temperature dependence of quantum dot laser diode characteristics. **a** Threshold current. **b** Lasing wavelength

the lasing wavelength is shown in Fig. 1.22b. The lasing wavelengths are 1276 nm at 25 °C and 1343 nm at 125 °C, meaning the temperature coefficient of the lasing wavelength is about 0.67 nm/K. Therefore, the other optical components integrated with the QD-LDs should be not only temperature insensitive but also wavelength insensitive around the above wavelength range.

The arrayed QD-LD chips are hybridly integrated on a silicon OW platform. The silicon OWs have rectangular cross-section cores that are 200-nm thick and 348-nm wide for bent OWs and 3-μm wide for straight ones. The narrower waveguides are designed for single mode ones around a 1.3-μm wavelength. The propagation losses at a wavelength of 1310 nm are about 3 dB/cm with 348-nm wide and 0.5 dB/cm with 3-μm wide cores. The propagation losses of the OWs have little sensitivity to both temperature and wavelength over the ranges concerned (25–125 °C and 1270–1350 nm). The measured temperature dependence of the coupling loss between the mounted QD-LDs and silicon OWs from 25 to 125 °C are plotted in Fig. 1.23. The

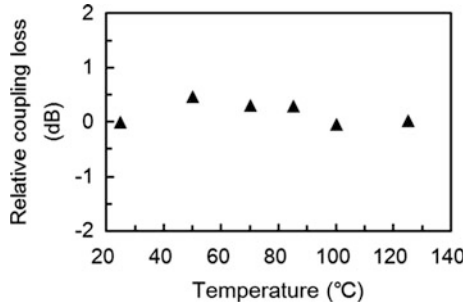


Fig. 1.23 Measured temperature dependence of the coupling loss between mounted quantum dot laser diodes and silicon optical waveguides at various temperatures

coupling loss is nearly constant across the entire temperature range. These results suggest that misalignment between the LDs and OWs due to temperature change is negligible across the entire temperature range. Since the optical system is complete and closed within the interposer substrate, it does not require external fiber alignment or polarization control. Therefore, we believe that the system is robust against both thermal and mechanical fluctuations.

1.5.2 Optical Modulators and Their Thermal Characteristics

As mentioned previously, the OMs integrated with the QD-LDs should be not only temperature insensitive but also wavelength insensitive over the whole wavelength range where the lasing wavelength shifts upon changes in temperature. Ring- or disk-resonator-based OMs are compact, but they are inherently sensitive to both temperature and wavelength [32–36]. Although some athermal or thermally stabilized resonator-based OMs have been reported, they were still sensitive to wavelength, and they usually required monitoring and feedback circuits for wavelength locking [33–36]. We believe that these additional circuits can be obstacles to developing large-scale integrated interconnect systems in terms of their footprint, power consumption, and cost. Therefore, we chose symmetric MZI-based OMs, which are inherently insensitive to both temperature and wavelength and do not require the additional circuits [37].

The structure of silicon OMs for athermal silicon optical interposers is similar to that shown in Fig. 1.13. It is a symmetric MZI. The side-wall grating is designed so that the stop-band wavelength is sufficiently shorter than the operating wavelength, and the transmission spectrum is flat around the operating wavelength. In fact, the measured wavelength dependence of passive insertion loss of the OMs without DC bias or RF signal is shown in Fig. 1.24. The wavelength dependence is less than 1 dB across the wavelength range concerned. Therefore, the OMs are wavelength

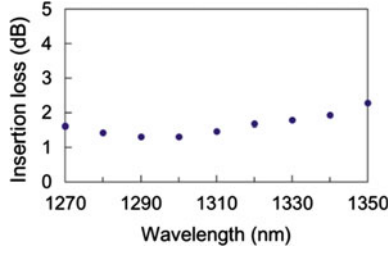


Fig. 1.24 Measured wavelength dependence of the passive insertion loss of optical modulators without DC bias or RF signal

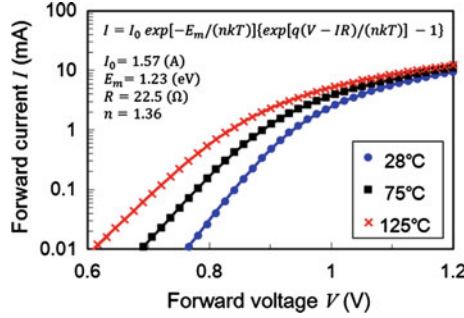


Fig. 1.25 Measured current–voltage (I – V) characteristics of optical modulators versus the forward bias voltage at operating temperature of 28, 75, and 125 °C

insensitive. One MMI coupler connected to the input port is 1×2 , and another connected to the output ports is 2×2 so that we can use differential outputs from both cross and bar ports. This configuration also allows us to apply the same bias voltages or currents to both arms of the MZI to satisfy a quadrature condition. This symmetric bias can cancel the OM output deviation due to the bias shifts in both arms due to temperature change.

The measured current–voltage (I – V) characteristics of the OMs with forward bias voltage at 28, 75, and 125 °C are plotted in Fig. 1.25 [38]. The measured I – V characteristics can be well expressed by the following equations:

$$I = I_0 \exp\left(-\frac{E_m}{nkT}\right) \left\{ \exp\left[\frac{q(V - RI)}{nkT}\right] - 1 \right\}, \quad I_0 = 1.57 \text{ A}, \quad E_m = 1.23 \text{ eV}, \quad R = 22.5 \text{ } \Omega, \quad n = 1.36, \quad (1.1)$$

where q is the electron charge, k is the Boltzmann's constant, and T is temperature. The solid lines in Fig. 1.25 were calculated using (1.1). Here n is the diode ideality factor, E_m corresponds to the band gap energy, and R corresponds to the series

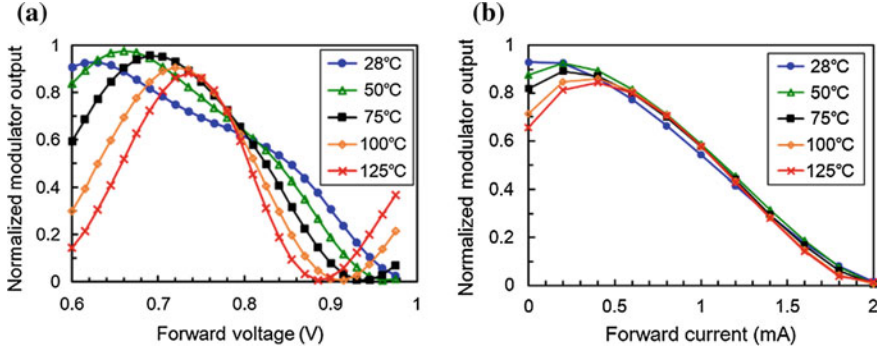


Fig. 1.26 Measured DC responses of optical modulators at various temperatures as functions of **a** forward bias voltage and **b** forward bias current

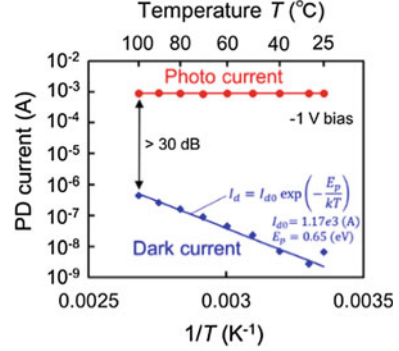
resistance. These parameters are useful for SPICE simulations. The diode current I under a constant bias voltage V around 0.8 V exponentially increased as the temperature rose.

The measured DC responses of the OM's at various temperatures as functions of forward bias voltage and forward bias current are shown in Fig. 1.26a, b, respectively [38]. On the horizontal axes in both figures, the biases were applied to both arms in an MZI on a push-pull basis so that the sum of voltages always equaled 1.575 V in (a) and the sum of currents always equaled 2.0 mA in (b). The vertical axes are normalized by the sum of the output power on both the cross and bar ports without applying bias at each temperature. In both figures, the quadrature conditions exhibit small temperature sensitivities due to the same biases being applied to both arms. However, the modulation efficiency as a function of voltage exhibits larger temperature sensitivity than that of the current. As a result, the DC responses as functions of the bias current are quite insensitive to temperature, unlike those obtained as functions of the bias voltage. Therefore, we used a constant bias-current condition for the following data link experiments.

1.5.3 Photodetectors and Their Thermal Characteristics

The structure of PD's for the athermal silicon optical interposers is similar to that shown in Fig. 1.15. The measured photo and dark currents of the PD's at various temperatures with 1-V reverse bias voltage are plotted in Fig. 1.27 [38]. The photo current is insensitive to temperature, meaning the responsivity of the PD's also exhibits little sensitivity to temperature. The dark current I_d , namely the leakage current in the PIN diode with reverse bias, can be well expressed by the following equation:

Fig. 1.27 Measured photo and dark currents of photodetectors with 1-V reverse bias voltage at various temperatures



$$I_d = I_{d0} \exp\left(-\frac{E_p}{kT}\right), \text{ with } I_{d0} = 1.17 \times 10^3 \text{ A, and } E_p = 0.65 \text{ eV.} \quad (1.2)$$

The E_p corresponding to the band gap energy is in good agreement with that of germanium (0.69 eV). Although the dark current increases exponentially with temperature rise, the photo-to-dark current ratio is higher than 30 dB up to 100 °C.

1.5.4 Data Link Experiments Over Wide Temperature Range

We carried out data link experiments with the athermal silicon optical interposers over a wide temperature range. A silicon optical interposer was put on a probe station under temperature control. The DC and RF driving conditions for LDs, OMs, and PDs were similar to those mentioned in the previous section. The measured BERs at 20 Gbps at various temperatures as functions of LD input current and PD received power are shown in Fig. 1.28a, b, respectively [38]. For these measurements, we intentionally changed the LD current to change the BER at each temperature but did not adjust the bias current of the OMs, bias voltage of the PDs, or RF input signals to the OMs throughout the entire temperature range from 25 to 125 °C. The penalty of the LD current above 100 °C was mainly caused by the decline in LD output. The penalty of the PD received power at 125 °C mainly caused by thermal noise is about 1 dB. We confirmed that the BER is less than 10^{-12} even at 125 °C when the PD received power is higher than -7.4 dBm. We achieved error-free data links at 20 Gbps without adjusting the OMs or PDs across the entire temperature range.

We also observed an eye diagram under fixed bias and signal conditions for the LDs, OMs, and PDs while the temperature was continuously changed from 25 to 125 °C. The average temperature-raising rate was about 0.8 °C/s. The eye diagram snapshots at some temperatures are summarized in Fig. 1.29. The magnification

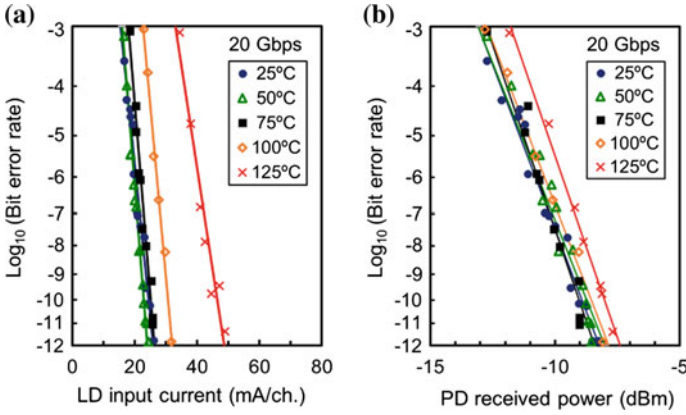
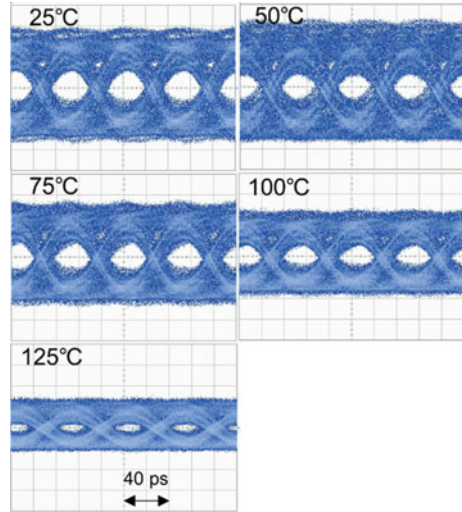


Fig. 1.28 Measured bit error rates at 20 Gbps at various temperatures as functions of **a** laser diode input current and **b** photodetector received power

Fig. 1.29 Eye diagram snapshots at 20 Gbps under fixed bias and signal conditions for laser diodes, optical modulators, and photodetectors while the temperature was continuously changed from 25 to 125 °C



ranges on the vertical axes are common among of them. Although the eye amplitude decreases due to the decline in LD output as temperature rises above 100 °C, we confirmed that the eye keeps opening across the entire temperature range without adjusting the device biases or signals. These experimental results suggest that the silicon optical interposers do not require additional monitoring or feedback circuits to stabilize temperature and/or wavelength across the wide temperature range from 25 to 125 °C or under a rapid temperature change of 0.8 °C/s.

We believe that the significance of the athermal operation up to 125 °C is as follows. Since the maximum junction temperatures in most LSIs have currently been below 125 °C and will be so in the future [7], our silicon optical interposers are

tolerant against the heat generated by the mounted LSIs. Furthermore, since an extended industrial temperature range, which is the widest one for ordinary electronic devices, is usually defined as -40 to 125 °C, the interposers are usable for a wide range of applications without complex monitoring or feedback controls.

1.6 25-Gbps Data Links Using Silicon Optical Interposers and FPGA Transceivers

To verify the feasibility of the silicon optical interposers with more practical configurations, we also demonstrated 25-Gbps optical data links on silicon optical interposers mounted on a PCB with a transimpedance amplifier (TIA) and a field-programmable gate array (FPGA) [39].

The setup for the data link experiments is shown in Fig. 1.30. A silicon optical interposer and a TIA are mounted close together on a PCB, and are linked by wire bonding. Bonding pads and coaxial connectors on the PCB are linked via differential microstrip lines. An FPGA (Altera Stratix V GT) is mounted on another PCB, and both PCBs are linked by coaxial cables. While the layout of the silicon optical interposers discussed in Sect. 1.4 is designed for flip-chip bonded LSIs, the layout in this section is designed for wire bonding. Therefore, the OM and PDs are placed near both edges of the interposers to shorten the bonding-wire length. Each channel supports differential signals to suppress common mode noises mainly radiating from the bonding wires in the OM side and received by the bonding wire in the PD side. Namely, an OM driven by a pair of electrical differential signals modulated CW light from an LD and output a pair of optical differential signals to a pair of OWs. A pair of PDs converted a pair of optical differential signals into a pair of electrical differential signals, then output them to a differential TIA. The differential system can also compensate modulation loss by the OMs up to 3 dB. The FPGA has four-channel 25-Gbps transceivers equipped with PRBS signal generators and

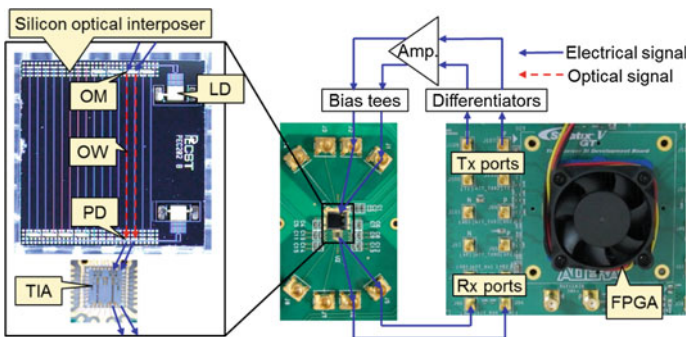


Fig. 1.30 Setup for data link experiments with silicon optical interposers, transimpedance amplifiers, and field-programmable gate arrays on printed circuit boards

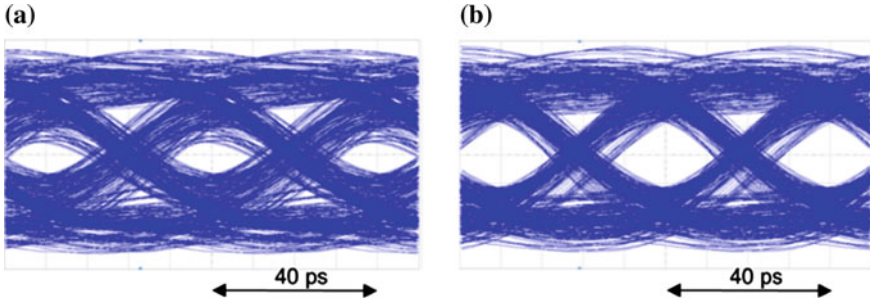
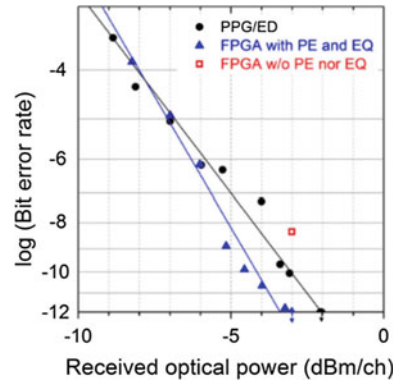


Fig. 1.31 Eye diagrams of transimpedance amplifier differential output at 25 Gbps **a** without and **b** with the pre-emphasis in field-programmable gate array transmitter

Fig. 1.32 Bit error rates at 25 Gbps without field-programmable gate array (FPGA), with FPGA without pre-emphasis (PE) or equalization (EQ), and with FPGA with PE and EQ



BER testers. The Tx has a pre-emphasis (PE) function using a three-tap finite impulse response (FIR) filter, and the Rx has an equalizer (EQ), such as a continuous time linear equalizer (CTLE).

We investigated three cases of data link experiments: (case 1) without FPGA, where the differentiators were connected to a pulse pattern generator (PPG) instead of the FPGA Tx and the TIA was connected to an error detector (ED) instead of the FPGA Rx; (case 2) with the FPGA without PE in the Tx nor EQ in the Rx; and (case 3) with the FPGA with PE and EQ. Figure 1.31 shows eye diagrams of the TIA differential output at 25 Gbps (a) without and (b) with PE in the FPGA Tx. The eye diagrams are degraded mainly due to the parasitic capacitance and inductance of the bonding wires, microstrip lines, and connectors on the PCBs. The eye diagram in Fig. 1.31b is improved by PE compared with that in Fig. 1.31a. The measured BERs in cases 1, 2, and 3 at 25 Gbps are plotted in Fig. 1.32. We confirmed error-free data links in cases 1 and 3. The receiver sensitivity is improved by about 1 dB by PE and EQ in the FPGA. The total footprint of the optical components is 0.0877 mm^2 per channel because the PD footprint is doubled for a differential receiver compared with that in Table 4.5. We achieved about 29 Tbps/cm^2 with a channel line rate of 25 Gbps.

1.7 Advanced Fabrication Process and Optical Components for Wider Bandwidth in Future

Because it generally takes a longer time and requires higher risk to design and fabricate fully integrated silicon optical interposers than to design and fabricate individual optical components, we used enough mature component designs and fabrication processes for the fully integrated silicon optical interposers mentioned in the previous sections. More advanced optical components and fabrication process, which are expected to be applied for optical interconnects that will have wider bandwidth in the future, have been also developed in the PECST project. Some are introduced in this section.

1.7.1 Hybridly Integrated 1200-Channel Light Source

We discussed a high bandwidth density of 30 Tbps/cm² with silicon optical interposers in Sect. 1.4. However, we not only need high bandwidth density but also wide bandwidth for practical optical interconnect applications. To achieve wide bandwidth, high channel-count light sources are required. Therefore, a hybridly integrated 1200-channel light sources were demonstrated [40]. Three 25-channel arrayed LD chips were mounted on a silicon OW platform by using flip-chip bonding with a passive alignment technique, as mentioned in Sect. 3.2.3, and each LD channel was split into 16 output ports by double cascade 1×4 OSs. Figure 1.33 shows the near-field pattern of outputs from the hybridly integrated 1200-channel light sources. The pitch of the output ports was 8 μm to include 1200 ports in 1 cm corresponding to a stepper shot size. The footprint of the light sources was $9700 \times 1210 \mu\text{m}^2$. The 1200-channel light source can provide 30-Tbps bandwidth with 25-Gbps OM.

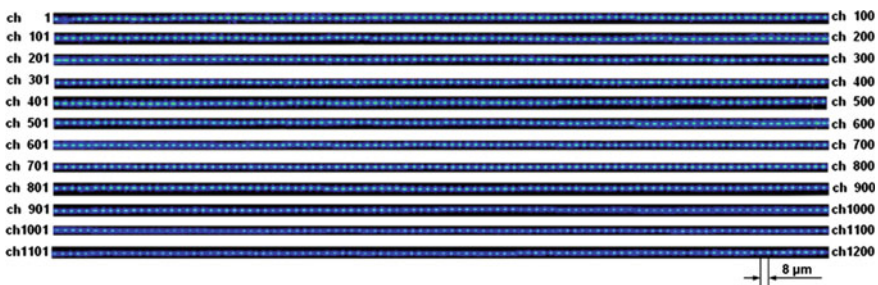


Fig. 1.33 Near-field pattern of outputs from hybridly integrated 1200-channel light sources

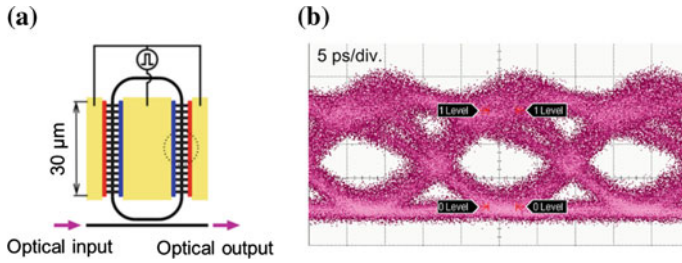


Fig. 1.34 Ring-resonator-based optical modulators (OMs) with side-wall gratings. **a** Schematic structure. **b** Eye diagram of OM output at 56 Gbps

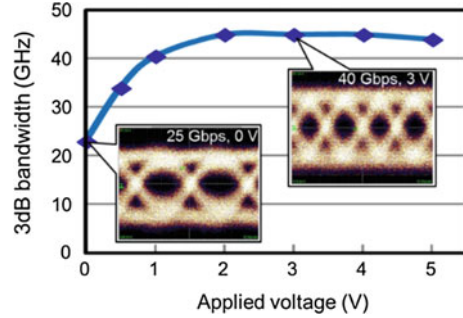
1.7.2 High-Speed Ring-Resonator-Based Optical Modulators

Although symmetric MZI-based OMs are inherently insensitive to both temperature and wavelength, as shown in Sect. 1.5, they usually require longer interaction length or higher driving voltage than ring-resonator-based OMs. The relatively long interaction length or high driving voltage often limits their modulation speed. Therefore, ring-resonator-based OMs with side-wall gratings and PIN junctions for higher speed and smaller footprint, namely higher bandwidth density, were demonstrated [41]. Figure 1.34a shows a schematic structure of the ring-resonator-based OMs. The structure of the phase shifter was similar to that mentioned in Sect. 1.3.3. The phase shifter length was 60 μm. Figure 1.34b shows a clear eye opening by the OMs at a high bit rate of 56 Gbps.

1.7.3 High-Speed Germanium Photodetectors with Low Contact Resistance

The response speeds of conventional PIN-type germanium PDs were mainly limited by their contact resistance between metal electrodes and the germanium mesa. The reduction in the contact resistance with a silicon capping layer over the germanium mesa was investigated [27]. Figure 1.35 shows the 3-dB bandwidth and eye diagrams of the improved PDs. The structure was similar to that shown in Fig. 1.15. The bandwidth was 23 GHz without bias voltage and 45 GHz with 2-V or higher bias voltages. Clear eye openings at 25 Gbps without bias voltage and at 40 Gbps with a 3-V bias were demonstrated.

Fig. 1.35 3-dB bandwidth and eye diagrams of photodetectors with reduced contact resistance



1.7.4 300-mm Wafer Processes with ArF Immersion Lithography for WDM

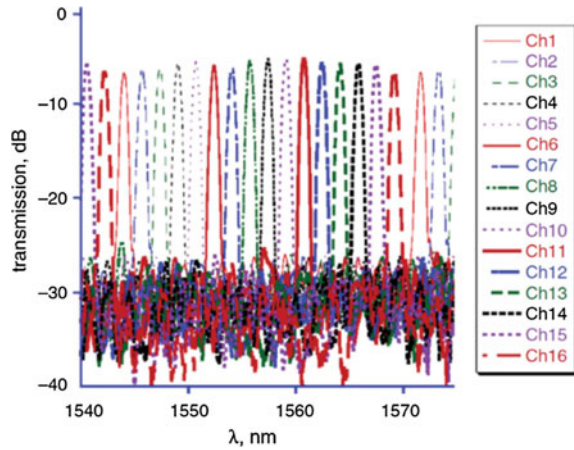
Wavelength division multiplexing (WDM) is an attractive candidate to achieve off-substrate optical interconnects with further wide bandwidth because WDM can reduce its fiber count. Interferometers or resonators composed of silicon OWs, which are expected to be used for wavelength filters or multiplexers/demultiplexers, are often affected by fluctuations in their characteristics due to fluctuations in their core dimensions. High refractive index contrast of silicon OWs requires quite small errors in patterning their cores. To mitigate the problem, a 300-mm SOI wafer process with ArF immersion lithography was introduced [42]. The measured width deviation in the silicon OW cores over a 300-mm SOI wafer was less than 2.5 nm, and the measured resonance wavelength deviation of ring resonators was less than 1.2 nm, which is sufficiently small for coarse WDM systems. Sixteen-channel arrayed waveguide gratings (AWGs) with 200-GHz channel spacing fabricated using precise SOI wafer processes combined with a carefully optimized design to reduce their crosstalk were also demonstrated [43]. Figure 1.36 shows the measured wavelength response of an AWG. A low crosstalk floor of -23 dB was achieved.

1.8 Perspectives on Inter-chip Interconnects

1.8.1 Vision for On-Board Datacenters

In Sect. 1.4, we introduced a vision of on-chip servers, with which functions and performance of present on-board servers will be integrated on a substrate in the 2020s. Then, the functions and performance of present server racks will be also integrated with the on-chip servers on a board, and the high-speed inter-substrate interconnects will be optical. We call this system an on-board data center. We believe that an optical PCB that supports both electrical and optical interconnects will be required to realize on-board data centers, and an efficient and low-cost

Fig. 1.36 Measured wavelength response of a 16-channel arrayed waveguide grating with 200-GHz channel spacing fabricated using a 300-mm silicon-on-insulator wafer process with ArF immersion lithography



coupling between optical devices on silicon optical interposers and external OWs, such as optical fibers or optical PCBs, will be a key technology.

The Integrated Photonics-Electronics Convergence System Technology Project, which is one of the projects in Future Pioneering Projects entrusted by the Minister of Economy, Trade and Industry (METI) of Japan, was started in 2012 as a 10-year project. The final target of this project in 2022 is to demonstrate the feasibility of on-board data centers. Therefore, optical PCBs are also being developed in the project [44]. In addition to the final target, we had set two milestones for practical applications. The first is an optical I/O core for application to an active optical cable (AOC) in 2015, and the second is an LSI package with optical I/Os in 2020. The AOCs are expected to be reduced in size and their power consumption and to extend their reach, as described in the following section. The LSI packages with optical I/Os are also expected to solve the bottlenecks of bandwidth density in the LSI pin and server front-panel.

1.9 Optical I/O Cores

Figure 1.37 shows photographs and schematic cross sections of four-channel parallel optical I/O cores, which are designed to be mounted either in an AOC module for the first milestone or around a host LSI in the LSI package for the second milestone [45]. They consist of a silicon photonics platform, optical coupling pins, a glass with through glass vias (TGVs) and a CMOS IC (driver or TIA). The use of the optical coupling pins and the TGVs simplifies the handling and setup for evaluating the samples because the optical and electrical I/O surface is flat enough to probe and mount easily. The SSCs, silicon OM, and grating couplers are monolithically integrated on the silicon photonics platform in a Tx, and

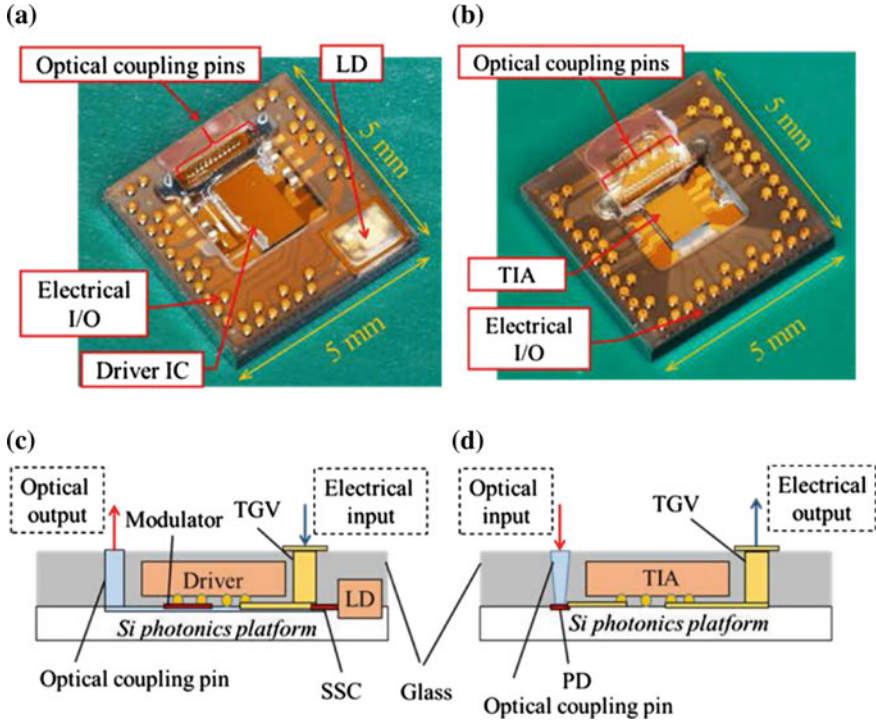


Fig. 1.37 Four-channel $\times$ 25-Gbps parallel optical I/O cores. Photographs of **a** transmitter (Tx) and **b** receiver (Rx). Schematic cross section of **c** Tx and **d** Rx

surface-illuminated germanium PDs are integrated in a Rx. An arrayed LD chip is flip-chip bonded to the substrate using a passive alignment technique, as described in Sect. 1.3.2.3. The CMOS ICs are also flip-chip bonded to the silicon photonics platform. Although the size of each optical I/O core (Tx, Rx) is only $5 \times 5 \text{ mm}^2$, it is possible to support up to 12 channels. We believe that the small size is achieved mainly due to the hybrid integration between the photonics and electronics described in Sect. 1.2.2 and also hybridly integrated butt-coupled lasers described in Sect. 1.2.3. This small size will contribute to smaller form factors for AOCs and wider I/O bandwidth for LSI packages. Error-free data links at 25 Gbps per channel over a 300-m multimode fiber (MMF) were demonstrated. The results suggest that the optical I/O cores are usable for 100-Gbps ($25 \text{ Gbps} \times 4 \text{ channel}$) transceivers, and the reach is extended by 3 times compared with conventional interconnects using VCSEL and MMF at 100 Gbps, which is up to 100 m [46]. Furthermore, the total power efficiency (or energy cost) for both Tx and Rx is 5 mW/Gbps (or pJ/bit) excluding the laser power. We estimate that the power consumption is lower than that of conventional 100-Gbps transceivers such as SR10, SR4, LR4, and PSM4 [47], even if the power consumption of LDs and clock data recoveries (CDRs) are

counted. The low power consumption was achieved mainly due to developing a lower-voltage (0.9 V) driven OM and using a 28-nm CMOS driver and TIA, which is also thanks to the hybrid integration between photonics and electronics.

1.9.1 Further Efficient Interconnects for On-Board Datacenters

Since the power consumption of a processor chip is expected to be around 100 W now and in the future, the power consumption of the optical I/O cores will exceed the processor power consumption if the power efficiency remains at 5 mW/Gbps and the inter-chip bandwidth grows beyond 20 Tbps. Therefore, our final target of power efficiency in the project is 1 mW/Gbps in 2022. To develop efficient devices, we may need stronger interactions between photons and electrons by using nano-structures such as photonic crystals [48] or plasmonics [49], and/or by using new materials such as compound semiconductors [50] or graphenes [51]. To develop efficient and flexible systems, we have to also examine network topology and routing architectures. We therefore may need efficient optical circuit switches or wavelength selective switches.

1.10 Conclusion

The problem we focused on was regarding bandwidth bottlenecks in inter-chip interconnects. To solve this problem, we first examined integration between photonics and electronics and integration between light sources and a silicon OW platform. Based on these examinations, we proposed a photonics–electronics convergence system with silicon optical interposers, which are hybridly integrated with LSIs and LDs and monolithically integrated with the other optical components on a silicon substrate. It is an optically complete and closed system. We also investigated configurations and characteristics of optical components for the silicon optical interposers, such as silicon OWs, hybridly integrated on-chip light sources, silicon OMs, and germanium PDs. The configurations are unique such as OWs with rectangular cores, light sources with high-density arrayed LDs and trident SSCs, and OMs with side-wall gratings, and the characteristics are suitable for the integrated silicon optical interposers. Then, we designed and fabricated silicon optical interposers integrated with the optical components on a silicon substrate. We achieved error-free data links with high bandwidth density of 30 Tbps/cm² by using the silicon optical interposers. The bandwidth density is sufficient for demand in the late 2010s. For practical applications, the optical interposers should be usable under high temperature conditions and rapid temperature changes so that they can cope with the heat generated by mounted LSIs. Therefore, we also designed and

fabricated athermal silicon optical interposers integrated with QD-LDs and other temperature-insensitive optical components. We demonstrated error-free data links with the athermal interposers operating up to 125 °C without any adjustments. The interposers are tolerant of the heat generated by the LSIs and usable over the extended industrial temperature range without complex monitoring or feedback controls. To verify the feasibility of the silicon optical interposers with more practical configurations, error-free data links at 25 Gbps with silicon optical interposers, TIAs, and FPGAs mounted on PCBs were also demonstrated. More advanced optical components and fabrication process, which are expected to be applied for optical interconnects that will have wider bandwidth in the future, have also been developed in the PECST project, some of which were introduced. Finally, we introduced the new IPECST project aim of demonstrating the feasibility of on-board data centers in 2022 and one of their latest achievements, optical I/O cores.

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References

1. What is big data? <http://www-01.ibm.com/software/data/bigdata/what-is-big-data.html>
2. Intel, Facebook collaborate on future data center rack technologies, http://newsroom.intel.com/community/intel_newsroom/blog/2013/01/16/intel-facebook-collaborate-on-future-data-center-rack-technologies
3. ISSCC 2014 trends, http://isscc.org/doc/2014/2014_Trends.pdf
4. JEDEC publishes Wide I/O 2 mobile DRAM standard, <http://www.jedec.org/news/pressreleases/jedec-publishes-wide-io-2-mobile-dram-standard>
5. J. Kim, Y. Kim, HBM: memory solution for bandwidth-hungry processors. Hot chips **26** (2014), http://www.hotchips.org/wp-content/uploads/hc_archives/hc26/Hc26-11-day1-epub/Hc26.11-3-Technology-epub/Hc26.11.310-HBM-Bandwidth-Kim-Hynix-Hot%20Chips%20HBM%202014%20v7.pdf
6. M. Black, Hybrid Memory Cube, in *Electronic Design Process Symposium* (2013), <http://www.eda.org/edps/edp2013/Papers/3-3%20FINAL%20for%20Mike%20Black.pdf>
7. International Technology Roadmap for Semiconductors 2012 Update, Overall Roadmap Technology Characteristics (ORTC) Tables, and Assembly and Packaging Tables, <http://www.itrs.net/ITRS%201999-2014%20Mtg,%20Presentations%20&%20Links/2012ITRS/Home2012.htm>

8. I.I.A. Young, E.M. Mohammed, J.T.S. Liao, A.M. Palermo, B.A. Block, M.R. Reshotko, P.L. D. Chang, Optical technology for energy efficient I/O in high performance computing. *IEEE Commun. Mag.* **48**, 184–191 (2010)
9. L. Chen, K. Preston, S. Manipatruni, M. Lipson, Integrated GHz silicon photonic interconnect with micrometer-scale modulators and detectors. *Opt. Express* **17**, 15248–15256 (2009)
10. K. Raj, J.E. Cunningham, R. Ho, X. Zheng, H. Schwetman, P. Koka, M. McCracken, J. Lexau, G. Li, H. Thacker, I. Shubin, Y. Luo, J. Yao, M. Asghari, T. Pinguet, J. Mitchell, A. V. Krishnamoorthy, 'Macrochip' computer systems enabled by silicon photonic interconnects. *Proc. SPIE* **7607**, 1–16 (2010)
11. G. Kim, J.W. Park, I.G. Kim, S. Kim, S. Kim, J.M. Lee, G.S. Park, J. Joo, K.S. Jang, J.H. Oh, S.A. Kim, J.H. Kim, J.Y. Lee, J.M. Park, D.W. Kim, D.K. Jeong, M.S. Hwang, J.K. Kim, K.S. Park, H.K. Chi, H.C. Kim, D.W. Kim, M.H. Cho, Low-voltage high-performance silicon photonic devices and photonic integrated circuits operating up to 30 Gb/s. *Opt. Express* **19**, 26936–26947 (2011)
12. Y. Arakawa, T. Nakamura, Y. Urino, T. Fujita, Silicon photonics for next generation system integration platform. *IEEE Commun. Mag.* **51**, 72–77 (2013)
13. R.E. Camacho-Aguilera, Y. Cai, N. Patel, J.T. Bessette, M. Romagnoli, L.C. Kimerling, J. Michel, An electrically pumped germanium laser. *Opt. Express* **20**, 11316–11320 (2012)
14. P.D. Dobbelaere, Light source approach for silicon photonics transceivers, in *Sunday workshop in ECOC, WS1* (2014), http://www.ecoc2014.org/uploads/Workshops/WS1/ECOC2014_WS1_Peter%20De%20Dobbelaere.pdf
15. M.N. Sysak, H. Park, A.W. Fang, J.E. Bowers, R. Jones, O. Cohen, O. Raday, M. Paniccia, "Experimental and theoretical thermal analysis of a hybrid silicon evanescent laser. *Opt. Express* **15**, 15041–15046 (2007)
16. T. Shimizu, N. Hatori, M. Okano, M. Ishizaka, Y. Urino, T. Yamamoto, M. Mori, T. Nakamura, Y. Arakawa, High density hybrid integrated light source with a laser diode array on a silicon optical waveguide platform for inter-chip optical interconnection, in *Proceedings of Group IV Photonics* (2011), pp. 181–183
17. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, Y. Arakawa, 2.2 pJ/bit operation of hybrid integrated light source on a silicon optical interposer for optical interconnection, in *Proceedings of IEEE Photonic Conference* (2013), pp. 254–255
18. Y. Urino, T. Shimizu, M. Okano, N. Hatori, M. Ishizaka, T. Yamamoto, T. Baba, T. Akagawa, S. Akiyama, T. Usuki, D. Okamoto, M. Miura, M. Noguchi, J. Fujikata, D. Shimura, H. Okayama, T. Tsuchizawa, T. Watanabe, K. Yamada, S. Itabashi, E. Saito, T. Nakamura, Y. Arakawa, First demonstration of high density optical interconnects integrated with lasers, optical modulators and photodetectors on single silicon substrate. *Opt. Express* **19**, B159–B165 (2011)
19. N. Hirayama, H. Takahashi, Y. Noguchi, M. Yamagishi, T. Horikawa, Low-loss Si waveguides with variable-shaped-beam EB lithography for large-scaled photonic circuits, in *Extended Abstract Solid State Devices and Materials* (2012), pp. 530–531
20. T. Shimizu, N. Hatori, M. Okano, M. Ishizaka, Y. Urino, T. Yamamoto, M. Mori, T. Nakamura, Y. Arakawa, Multichannel and high-density hybrid integrated light source with a laser diode array on a silicon optical waveguide platform for interchip optical interconnection. *Photon. Res.* **2**, A19–A24 (2014)
21. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, Y. Arakawa, A hybrid integrated light source on a silicon platform using a trident spot-size converter. *J. Lightwave Technol.* **32**, 1329–1336 (2014)
22. T. Shimizu, M. Ishizaka, N. Hatori, M. Okano, T. Yamamoto, M. Mori, Y. Urino, T. Nakamura, Y. Arakawa, Multi-channel hybrid integrated light source for ultra-high-bandwidth optical interconnections and its structural optimization for low power consumption by considering thermal interference between LD array. *Trans. Jpn. Inst. Elect. Pack.* **7**, 94–103 (2014)

23. L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, M. Paniccia, 40 Gbit/s silicon optical modulator for high speed applications. *Electron. Lett.* **43**, 1196–1197 (2007)
24. D.J. Thomson, F.Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J.-M. Fedeli, G. T. Reed, High contrast 40 Gb/s optical modulation in silicon. *Opt. Express* **19**, 11507–11516 (2011)
25. P. Dong, L. Chen, Y.-K. Chen, High-speed low-voltage single-drive push-pull silicon Mach-Zehnder modulators. *Opt. Express* **20**, 6163–6169 (2012)
26. S. Akiyama, T. Baba, M. Imai, T. Akagawa, M. Takahashi, N. Hirayama, H. Takahashi, Y. Noguchi, H. Okayama, T. Horikawa, T. Usuki, 12.5-Gb/s operation with 0.29-V·cm $V\pi L$ using silicon Mach-Zehnder modulator based-on forward-biased pin diode. *Opt. Express* **20**, 2911–2923 (2012)
27. J. Fujikata, M. Miura, M. Noguchi, D. Okamoto, T. Horikawa, Y. Arakawa, Si waveguide-integrated metal–semiconductor–metal and p–i–n-type Ge photodiodes using Si-capping layer. *Jpn. J. Appl. Phys.* **52**, 04CG10 (2013)
28. Y. Urino, T. Usuki, J. Fujikata, M. Ishizaka, K. Yamada, T. Horikawa, T. Nakamura, Y. Arakawa, High-density and wide-bandwidth optical interconnects with silicon optical interposers. *Photon. Res.* **2**, A1–A7 (2014)
29. Y. Arakawa, H. Sakaki, Multidimensional quantum well laser and temperature dependence of its threshold current. *Appl. Phys. Lett.* **40**, 939–941 (1982)
30. A. Lee, Q. Jiang, M. Tang, A. Seeds, H. Liu, Continuous-wave InAs/GaAs quantum-dot laser diodes monolithically grown on Si substrate with low threshold current densities. *Opt. Express* **20**, 22181–22187 (2012)
31. A.Y. Liu, C. Zhang, J. Norman, A. Snyder, D. Lubyshev, J.M. Fastenau, A.W.K. Liu, A.C. Gossard, J.E. Bowers, High performance continuous wave 1.3 μm quantum dot lasers on silicon. *Appl. Phys. Lett.* **104**, 041104-1–4 (2014)
32. K. Tanabe, T. Rae, K. Watanabe, Y. Arakawa, High-temperature 1.3 μm InAs/GaAs quantum dot lasers on Si substrates fabricated by wafer bonding. *Appl. Phys. Express* **6**, 082703-1-4 (2013)
33. T. Baba, S. Akiyama, M. Imai, N. Hirayama, H. Takahashi, Y. Noguchi, T. Horikawa, T. Usuki, 50-Gb/s ring-resonator-based silicon modulator. *Opt. Express* **21**, 11869–11876 (2013)
34. K. Padmaraju, D.F. Logan, T. Shiraishi, J.J. Ackert, A.P. Knights, K. Bergman, Wavelength locking and thermally stabilizing microring resonators using dithering signals. *J. Lightwave Technol.* **32**, 505–515 (2014)
35. X. Zheng, E. Chang, P. Amberg, I. Shubin, J. Lexau, F. Liu, H. Thacker, S.S. Djordjevic, S. Lin, Y. Luo, J. Yao, J.H. Lee, K. Raj, R. Ho, J.E. Cunningham, A.V. Krishnamoorthy, A high-speed, tunable silicon photonic ring modulator integrated with ultra-efficient active wavelength control. *Opt. Express* **22**, 12628–12633 (2014)
36. E. Timurdogan, C.M.S. Agaskar, J. Sun, E.S. Hosseini, A. Biberman, M.R. Watts, An ultralow power athermal silicon modulator. *Nat. Commun.* **5**(4008), 1–11 (2014)
37. S. Akiyama, T. Baba, M. Imai, M. Mori, T. Usuki, High-performance silicon modulator for integrated transceivers fabricated on 300-mm wafer, in *Proceedings of ECOC*, P.2.8 (2014)
38. Y. Urino, N. Hatori, K. Mizutani, T. Usuki, J. Fujikata, K. Yamada, T. Horikawa, T. Nakamura, Y. Arakawa, First demonstration of athermal silicon optical interposers with quantum dot lasers operating up to 125 °C. *J. Lightwave Technol.* **33**, 1223–1229 (2015)
39. D. Okamoto, Y. Urino, T. Akagawa, S. Akiyama, T. Baba, T. Usuki, M. Miura, J. Fujikata, T. Shimizu, M. Okano, N. Hatori, M. Ishizaka, T. Yamamoto, H. Takahashi, Y. Noguchi, M. Noguchi, M. Imai, M. Yamagishi, S. Saitou, N. Hirayama, M. Takahashi, E. Saito, D. Shimura, H. Okayama, Y. Onawa, H. Yaegashi, H. Nishi, H. Fukuda, K. Yamada, M. Mori, T. Horikawa, T. Nakamura, Y. Arakawa, Demonstration of 25-Gbps optical data links on silicon optical interposer using FPGA transceiver, in *Proceedings of ECOC*, P.2.11 (2014)
40. T. Shimizu, M. Okano, H. Takahashi, N. Hatori, M. Ishizaka, T. Yamamoto, M. Mori, T. Horikawa, Y. Urino, T. Nakamura, Y. Arakawa, Demonstration of over 1000-channel hybrid

- integrated light source for ultra-high bandwidth interchip optical interconnection, in *Proceedings of OFC*, Th1C.6 (2014)
41. S. Akiyama, T. Usuki, High-speed and efficient silicon modulator based on forward-biased pin diodes. *Front. Phys.* **2**(65), 1–7 (2014)
 42. H. Takahashi, M. Toyama, M. Seki, D. Shimura, K. Koshino, N. Yokoyama, M. Ohtsuka, A. Sugiyama, E. Ishitsuka, T. Sano, T. Horikawa, The impacts of ArF Excimer Immersion Lithography on Integrated Silicon Photonics Technology, in *Ext. Abst. Solid State Devices and Materials* (2012), pp. 528–529
 43. H. Okayama, D. Shimura, Y. Onawa, H. Takahashi, M. Seki, K. Koshino, N. Yokoyama, M. Ohtsuka, T. Tsuchizawa, H. Nishi, K. Yamada, H. Yaegashi, T. Horikawa, H. Sasaki, Si wire array waveguide grating with stray light reduction scheme fabricated by ArF excimer immersion lithography. *Electron. Lett.* **49**, 1401–1402 (2013)
 44. T. Amano, S. Ukita, Y. Egashira, M. Sasaki, M. Mori, K. Kurata, A 25-Gbps operation of polymer-based optical and electrical hybrid LSI package substrate with optical card edge connector, in *Proceedings of IEEE Optical interconnects conference*, WB2 (2015)
 45. K. Yashiki, Y. Suzuki, Y. Hagihara, M. Kurihara, M. Tokushima, J. Fujikata, A. Ukita, K. Takemura, T. Shimizu, D. Okamoto, J. Ushida, S. Takahashi, T. Uemura, M. Okano, J. Tsuchida, T. Nedachi, M. Fushimi, I. Ogura, J. Inasaka, K. Kurata, 5 mW/Gbps hybrid-integrated Si-photonics-based optical I/O cores and their 25-Gbps/ch error-free operation with over 300-m MMF, in *Proceedings of OFC*, Th1G.1 (2015)
 46. J. Petrilla, 100G MMF Reach Objective, in *IEEE P802.3 Next Generation 100 Gb/s Optical Ethernet Study Group Plenary Meeting* (2012), http://www.ieee802.org/3/100GNGOPTX/public/mar12/plenary/petrilla_02b_0312_NG100GOPTX.pdf
 47. J. Petrilla, 100G PSM4 Power, Size & Cost Estimates & Comparisons, in *IEEE P802.3bm 40 Gb/s and 100 Gb/s Fiber Optic Task Force Interim Meeting* (2013), http://www.ieee802.org/3/bm/public/jan13/petrilla_03a_0113_optx.pdf
 48. H.C. Nguyen, S. Hashimoto, M. Shinkawa, T. Baba, Compact and fast photonic crystal silicon optical modulators. *Opt. Express* **20**, 22465–22474 (2012)
 49. A. Melikyan, L. Alloatti, A. Muslija, D. Hillerkuss, P.C. Schindler, J. Li, R. Palmer, D. Korn, S. Muehlbrandt, D. Van Thourhout, B. Chen, R. Dinu, M. Sommer, C. Koos, M. Kohl, W. Freude, J. Leuthold, High-speed plasmonic phase modulators. *Nat. Photonics* **8**, 229–233 (2014)
 50. Y. Kim, M. Takenaka, T. Osada, M. Hata, S. Takagi, Strain-induced enhancement of plasma dispersion effect and free-carrier absorption in SiGe optical modulators. *Sci. Rep.* **4**, 4683 (2014)
 51. S.J. Koester, M. Li, High-speed waveguide-coupled graphene-on-graphene optical modulators. *Appl. Phys. Lett.* **100**, 171107 (2012)

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