

Chapter 2

Considerations for Nanoscale Manufacturing

In this part of the book the development of a versatile micro- and nanoscale structuring process is described in detail. In chapter 3, we will outline the physical principles of thin film deposition such as magnetron sputtering and electron-beam evaporation. Chapter 4 discusses the development of a unique process design that is based on a common GDSII-layout. The structure references are designed with nanometer precision and placed on different process layers.

Due to the required small length scales of uniform superconducting conduction paths down to the order of the quasiparticle cloud expansion (*Hot-Spot*) (see Fig. 1.6), a standard planar top-down approach was employed to structure the thin films with achievable critical dimensions in the sub-100 nm regime. The nanoscale pattern was generated by an electron-beam lithographic step (see chapter 5.4) followed by a dry-etching step (see chapter 5.6) in a reactive radio-frequency (RF) plasma. In order to reduce the writing time of the electron-beam lithographic machine, the microscale pattern was defined in a photolithographic (see chapter 5.3) lift-off deposition step.

Note that chapter 5.1 provides an overview about the challenges associated with easy and effective nanoscaled top-down manufacturing based on the combination of photolithography (see chapter 5.3) and electron-beam lithography (see chapter 5.4). Chapter 5.5 has been written with the intention to introduce the challenges associated with the achievement of a minimum line-edge roughness when combining the electron-beam lithography (see chapter 5.4) with reactive ion etching (see chapter 5.6) to pattern thin superconducting films.

For the fabrication of nanoscale superconducting devices one can, in principle, apply the technological approaches developed for modern information technology. However, the existing processes need a proper modification due to the different nature of the superconducting state. In order to be more flexible when interchanging process-steps and/or parameters to satisfy the specific demands of superconducting process technology, a nanoscale lift-off (see chapter 5.4.5) as well as an etching nm-patterning process (see chapters 5.4.8 & 5.4.9) were developed in order to investigate which one is more appropriate for the fabrication of high quality nanoscale superconductors. At the same time the process is flexible enough to allow for the usage of the same chromium mask (see Fig. 5.6) for the photolithographically defined structures.

The most important achievements of the process developments are the “*production of superconducting nanowire single-photon detectors*” with lithographically defined length scales of about 50 nm and with critical temperatures $T_c(0) \cong 12.5$ K that are comparable to the unstructured film $T_c(0) \cong 13.2$ K. For 14 NbN single-photon detectors, we tabulate in Tabs. 11.3 & 11.4 the arithmetic average \bar{x}_{arith} and the standard deviation $\sqrt{\sigma^2}$ for

several measured parameters. The small standard deviation reflects the high quality of the developed manufacturing procedure.

Because the University of Zürich is and will be heavily involved in research from the macro- down to the nanoscale of superconductors, the parameter frame for the used clean room machinery at the FIRST Center for Micro- and Nanoscience of ETH Zürich was explored as generally as possible with the intention that future projects can build on these results and only a few process parameters and layouts have to be optimized when investigating other (not necessarily superconducting) compounds or devices.

In this first part a detailed discussion about the physics taking place during nanofabrication is given. In Fig. 2.1, an overview is shown about the results of the developed process after a typical fabrication run. I hope to present an appealing overview about the developed process, so that every reader gains a good feeling about feasible state-of-the-art nanotechnology in our days. The reader who is not interested in the physics of the fabrication process may skip this first part of the book and continue with the second one (chapter 8 on page 129).

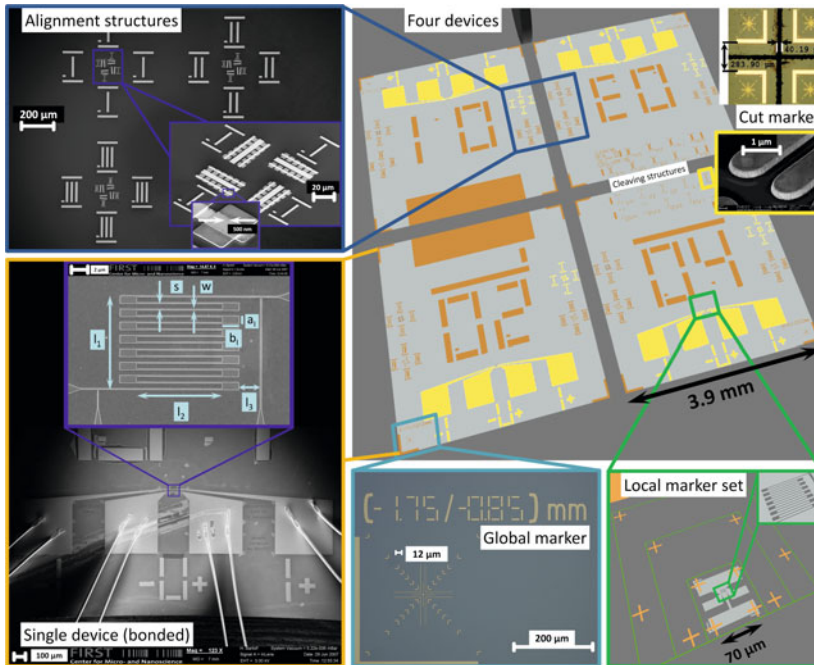


Fig. 2.1: Overview from the mm-Scale into the Nanoscale: Basic layout of a chip for the fabrication of four devices. The process enables scalability for manufacturing over 1000 devices on a 2" wafer. The nanoscale definition of the device is created by electron-beam lithography (see chapter 5.4) and reactive ion etching (see chapter 5.6). The positioning marks and the connection of the nanostructure to the outer world (bond pads via Au-leads) are fabricated by a photolithographic lift-off deposition process (see Fig. 5.5). Every electron-beam written structure can be designed individually, and the process layout allows for the definitions of differently sized write fields (see Fig. 5.15) from 100 μm up to 500 μm. The displayed four devices are fabricated in one fabrication run and are afterwards separated with a wafer saw (see also Fig. 6.3).

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