

Contents

Preface	V
Abstract	VII
Acknowledgements	IX
Contents	XI
List of Figures	XIX
List of Tables	XXIII
Abbreviations	XXVII
Nomenclature	XXX
Author's Publications	XXXI
1 Introduction	1
1.1 Motivation	1
1.2 Goal and Contributions of the Thesis	2
1.3 Organization of the Thesis	3
1.4 Applications of Multiple Constant Multiplication	5
2 Background	9
2.1 Single Constant Multiplication	9
2.1.1 Binary Multiplication	9

2.1.2	Multiplication using Signed Digit Representation . . .	10
2.1.3	Multiplication using Generic Adder Graphs	11
2.2	Multiple Constant Multiplication	12
2.3	Constant Matrix Multiplication	12
2.4	Definitions	13
2.4.1	Adder Graph Representation of Constant Multiplication	14
2.4.2	Properties of the $\mathcal{A}$ -Operation	15
2.4.3	$\mathcal{A}$ -Sets	17
2.4.4	The MCM Problem	17
2.4.5	MCM with Adder Depth Constraints	18
2.5	Field Programmable Gate Arrays	19
2.5.1	Basic Logic Elements of Xilinx FPGAs	21
2.5.2	Basic Logic Elements of Altera FPGAs	21
2.5.3	Mapping of Adder Graphs to FPGAs	22
2.5.4	Cost Models for Pipelined Adders and Registers . . .	26
2.6	Related Work	28
2.6.1	Single Constant Multiplication	28
2.6.2	Multiple Constant Multiplication	29
2.6.3	Modified Optimization Goals in SCM and MCM Op- timization	33
2.6.4	Pipelined Multiple Constant Multiplication	33

I The Pipelined Multiple Constant Multiplication Problem 37

3 Optimal Pipelining of Precomputed Adder Graphs 39

3.1	Pipelining of Adder Graphs using Cut-Set Retiming	39
3.2	Minimized Pipeline Schedule using Integer Linear Programming	41
3.2.1	Basic ILP Formulation	42

3.2.2	Extended ILP Formulation	43
3.3	Experimental Results	44
3.3.1	Register Overhead	45
3.3.2	Slice Comparison	46
3.3.3	Device Utilization	47
3.3.4	Silicon Area	49
3.4	Conclusion	51
4	The Reduced Pipelined Adder Graph Algorithm	53
4.1	Definition of the PMCM Problem	54
4.1.1	Cost Definition	55
4.1.2	Relation of PMCM to MCM	56
4.2	The RPAG Algorithm	56
4.2.1	The Basic RPAG Algorithm	57
4.2.2	Computation of Single Predecessors	58
4.2.3	Computation of Predecessor Pairs	59
4.2.4	Evaluation of Predecessors	62
4.2.5	The Overall RPAG Algorithm	63
4.2.6	Computational Complexity	68
4.3	Lower Bounds of Pipelined MCM	71
4.4	Implementation	72
4.5	Experimental Results	73
4.5.1	Registered Operations and CPU Runtime	73
4.5.2	Influence of the Search Width Limit to the Optimization Quality	74
4.5.3	Comparison of Cost Models	74
4.5.4	Comparison Between Gain Functions	77
4.5.5	Influence of the Pipeline Stages to the Optimization Quality	79

4.5.6	Comparison with the Optimal Pipelining of Precomputed Adder Graphs	81
4.5.7	Comparison Between Aksoy's Method and RPAG . . .	84
4.6	Conclusion	84
5	Optimally Solving MCM Related Problems using ILP	87
5.1	Related Work	87
5.2	ILP Formulations of the PMCM Problem	91
5.2.1	PMCM ILP Formulation 1	92
5.2.2	PMCM ILP Formulation 2	94
5.2.3	PMCM ILP Formulation 3	96
5.3	Extensions to Adder Depth Constraints and GPC Minimization	96
5.4	Further Extensions of the ILP Formulations	99
5.5	Analysis of Problem Sizes	100
5.5.1	Evaluation of Set Sizes of $\mathcal{A}^s$ and $\mathcal{T}^s$	100
5.5.2	Relation to FIR Filters	100
5.6	Experimental Results	101
5.6.1	FIR Filter Benchmark	102
5.6.2	Benchmark Filters from Image Processing	103
5.6.3	Optimization Results with High-Level Cost Model . .	104
5.6.4	Optimization Results with Low-Level Cost Model . .	105
5.6.5	Synthesis Results	105
5.6.6	Optimization Results for Minimal Adder Depth . . .	107
5.7	Conclusion	110
6	A Heuristic for the Constant Matrix Multiplication Problem	113
6.1	Related Work	115
6.2	RPAG extension to CMM	116
6.2.1	Adder Graph Extensions to CMM	116

6.2.2	Definition of the PCMM and CMM _{MAD} /CMM _{BAD} Problems	117
6.2.3	Computation of Predecessors	118
6.2.4	Evaluation of Predecessors	119
6.2.5	Overall Algorithm	119
6.3	Experimental Results	120
6.4	Conclusion	124

II FPGA Specific MCM Optimizations 125

7 Combining Adder Graphs with LUT-based Constant Multipliers 127

7.1	Related Work	127
7.2	LUT-based Constant Multiplication	128
7.3	LUT Minimization Techniques	129
7.4	ILP Formulation for the Combined PALG Optimization . . .	130
7.5	Experimental Results	133
7.6	Conclusion	135

8 Optimization of Hybrid Adder Graphs 139

8.1	Implementation Techniques for Large Multipliers	140
8.2	Hybrid PMCM Optimization with Embedded Multipliers . .	142
8.2.1	Depth of the Input PAG	146
8.2.2	Depth of the Output PAG	146
8.3	RPAG Modifications	146
8.4	Experimental Results	147
8.4.1	Trade-off Between Slices and DSP Resources	147
8.4.2	Reducing Embedded Multipliers in Large MCM Blocks	147
8.5	Conclusion	149

9	Floating Point Multiple Constant Multiplication	153
9.1	Constant Multiplication using Floating Point Arithmetic . . .	153
9.2	Floating Point MCM Architecture	154
9.2.1	Multiplier Block	154
9.2.2	Exponent Computation	155
9.2.3	Post-Processing	156
9.3	Experimental Results	156
9.3.1	Floating Point SCM	157
9.3.2	Floating Point MCM	158
9.4	Conclusion	161
10	Optimization of Adder Graphs with Ternary (3-Input) Adders	163
10.1	Ternary Adders on Modern FPGAs	163
10.1.1	Realization on Altera FPGAs	164
10.1.2	Realization on Xilinx FPGAs	165
10.1.3	Adder Comparison	166
10.2	Pipelined MCM with Ternary Adders	167
10.2.1	$\mathcal{A}$ -Operation and Adder Depth	168
10.2.2	Optimization Heuristic RPAGT	168
10.2.3	Predecessor Topologies	169
10.3	Experimental Results	172
10.4	Conclusion	174
11	Conclusion and Future Work	177
11.1	Conclusion	177
11.2	Future Work	178
11.2.1	Use of Compressor Trees	178
11.2.2	Reconfigurable MCM	179
11.2.3	Optimal Ternary SCM circuits	179

A	Benchmark Coefficients	181
A.1	Two-Dimensional Filters	181
A.2	Floating-Point Filters	183
B	Computation of the $\mathcal{A}_*$ Set	187
	Bibliography	189

Multiple Constant Multiplication Optimizations for Field
Programmable Gate Arrays

Kumm, M.

2016, XXXIII, 206 p. 47 illus., Softcover

ISBN: 978-3-658-13322-1