

# Preface

Bias Temperature Instability (BTI) is a serious reliability concern and continues to threaten the performance and lifetime of Complementary MOS (CMOS) devices and circuits. BTI affects both n- and p-channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Historically, Negative BTI (NBTI) became an important issue for p-MOSFETs as the semiconductor industry migrated from Silicon Oxide ( $\text{SiO}_2$ ) to Silicon Oxynitride (SiON) gate insulators. NBTI continues to remain a serious issue for sub-22 nm technology nodes featuring High-K Metal Gate (HKMG) gate insulator based FinFET technologies. Positive BTI (PBTI) for n-MOSFETs remained negligible for SiON devices and emerged as a serious concern with the advent of HKMG gate insulator technology. However, latest reports from sub-22 nm Replacement Metal Gate (RMG) FinFET technologies have shown that PBTI is no longer a significant reliability concern.

Due to its technological significance, various research groups have extensively studied BTI in the last 15 years. In keeping with the technological trend, published reports initially focused on NBTI in SiON p-MOSFETs and later on both NBTI and PBTI in HKMG MOSFETs. These reports can be broadly classified into five major categories as explained hereinafter. Some reports have focused on process optimization for BTI mitigation and technology qualification, and studied the impact of various gate insulator and other processes and materials on BTI degradation. Other reports have focused on the development of novel methodologies for artifact-free characterization of BTI degradation and associated gate insulator defects. A significant majority of reports have focused on the understanding of BTI physical mechanism and development of numerical and compact models to explain measured data for DC and AC BTI degradation. Recently, some reports have focused on BTI variability, which is becoming important as device dimensions are scaled down. Finally, a significant majority of reports have also been published to study the impact of BTI on circuit and product degradation.

This book covers the first three aspects of BTI degradation as mentioned above, viz., characterization methodologies, impact of gate insulator processes and materials, and physics-based models for DC and AC BTI. In the early years of research, no consensus existed among different groups on the experimental kinetics, process

and materials dependence and physical mechanism of NBTI degradation. Therefore, development of suitable processes for NBTI mitigation and control became extremely difficult. Moreover, it became almost impossible to develop predictive models for estimating DC NBTI degradation at end-of-life, and to predict AC activity aware degradation for switching logic. Furthermore, although vast majority of published reports from different groups have dealt with understanding the physical mechanism and modeling of NBTI degradation, none can provide a comprehensive framework to explain measured results in SiON and HKMG p-MOSFETs and for DC and AC stress. Finally, some controversy also surrounded the physical mechanism and modeling of PBTI in HKMG n-MOSFETs.

The results presented in this book are extensively based on research carried out by our group in the past 13 years. Published results are also reported as and when necessary, to establish a comprehensive and universal picture of BTI degradation throughout the book. Our research has demonstrated that the lack of consensus in early NBTI reports arose due to the use of different nonstandard characterization methodologies and different gate insulator processes by different groups. Subsequently, proper artifact-free stress and measurement methodologies have been developed to characterize BTI degradation and also the underlying defects responsible for BTI degradation. The gate insulator process and material dependencies of NBTI degradation have been established for SiON and HKMG p-MOSFETs. The gate insulator process and material dependencies of PBTI degradation in HKMG n-MOSFETs are also established.

A consistent physical mechanism has been proposed to explain and model the experimentally observed process and material dependencies of NBTI in SiON and HKMG p-MOSFETs and PBTI in HKMG n-MOSFETs. The proposed framework is based on different mutually uncoupled underlying defect subcomponents, which are also assessed using independent measurement methods. Finally, a comprehensive DC and AC NBTI modeling framework is proposed and verified against experimental data in SiON and HKMG p-MOSFETs. The framework can successfully explain time evolution of measured NBTI degradation during and after DC stress and during multiple DC stress and recovery cycles, and during AC stress at different frequency and duty cycle. It can also predict extrapolated degradation at end of life for DC and AC NBTI stress.

Chapter 1 reviews NBTI and PBTI results from different published reports, and also shows measured DC and AC stress data using ultra-fast methods in SiON and HKMG devices under different experimental conditions. Different ultra-fast BTI characterization methods are discussed in Chap. 2, along with different characterization techniques for directly estimating gate insulator defects responsible for BTI. A consistent NBTI and PBTI mechanism is proposed and verified against experimental data in Chap. 3. Compact NBTI and PBTI models are developed in Chap. 4 based on the mechanism developed in Chap. 3, and the models are used to explain measured NBTI data in differently processed SiON and HKMG p-MOSFETs and PBTI data in different HKMG n-MOSFETs. The fundamentals of the

Reaction-Diffusion (RD) model are discussed in Chap. 5. Finally, the comprehensive DC and AC NBTI modeling framework is established in Chap. 6, and verified against ultra-fast measured data in SiON and HKMG p-MOSFETs.

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