

Chapter 2

Line Edge Roughness (LER)

2.1 Introduction

As the physical dimensions of metal oxide semiconductor field effect transistors (MOSFETs), such as physical channel length and channel width, continue to shrink at the pace described in Moore's Law, photo-lithography technology has developed to meet the demand of printing aggressively scaled feature sizes. A brief history of the development of lithography techniques, from the 65 nm technology node to sub-10 nm technology nodes, is illustrated in Fig. 2.1. In 65 nm complementary metal oxide semiconductor (CMOS) technology, 30 nm logic gates and high density embedded memories are fabricated using ArF dry 193 nm lithography [1]. Immersion techniques for state-of-the-art photo-lithography technologies were first proposed in the 1980s [2]. While 157 nm lithography was postponed on account of strong pellicle and photoresist absorptions, 193 nm immersion lithography was rapidly adopted in the 45 nm CMOS fabrication process [3]. In sub-45 nm technology nodes, the resolution of a photoresist pattern can be further scaled down by using 193 nm immersion lithography with double exposure (DE) or double patterning (DP) [4]. Although extreme ultraviolet (EUV) lithography is expected to break through the 7 nm node with sub-15 nm resolution, technical issues, such as source power and particle contamination, prohibit its use in high-volume manufacturing.

Line edge roughness (LER) refers to the randomly varied edges of gate patterns, or the roughness of the printed pattern edge. As the minimum feature size is decreased below tens of nanometers, the effect of LER on MOSFET performance can no longer be neglected. The LER creates a few lucky channels (i.e., local short channels) in the channel length direction, resulting in device-to-device mismatch. For example, 2 % degradation in on-state drive current is experimentally observed in Intel's 65 nm devices where 3σ (where σ indicates standard deviation) of LER is greater than 10 % of the nominal gate critical dimension [5]. Because LER-induced variation is highly correlated with the short channel effect (SCE), SCE-robust

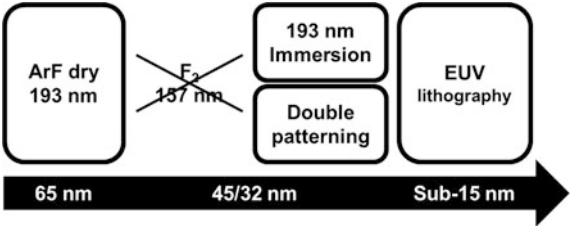


Fig. 2.1 The development history of photo-lithography techniques. For sub-30 nm CMOS technology, double patterning combined with 193 nm immersion lithography is used to fabricate extremely scaled CMOS patterns

Table 2.1 LER-induced V_{TH} variation in tri-gate MOSFETs depending on lithography technique [9]

V_{TH} variation	LER only		Total variation	
	DP (mV)	SP (mV)	DP (mV)	SP (mV)
$\sigma V_{TH, sat}$	12.2	15.3	49.1	49.6
$\sigma V_{TH, lin}$	7.0	8.6	38.5	38.7

device structures are less affected by LER-induced performance variation in a given LER profile. For example, six-transistor (6-T) SRAM cells composed of multi-gate devices, such as FinFETs and tri-gate MOSFETs [6, 7], or ultra-thin-body devices, such as FDSOI MOSFETs [8], show better immunity to LER-induced process variability because of their improved gate-to-channel capacitive coupling (in comparison with conventional planar bulk MOSFETs). Furthermore, as listed in Table 2.1, the LER-induced V_{TH} variation in 28 nm tri-gate bulk MOSFETs can be reduced by approximately 20 % by taking advantage of DP [9]. It should be noted that, despite the decrease in LER-induced V_{TH} variation, the amount of total random variation is only slightly reduced. It indicates that other random variation sources, such as random dopant fluctuation (RDF) or work function variation (WFV), are more dominant than LER in tri-gate bulk MOSFETs (note: RDF and WFV will be discussed in detail in the following sections). However, although V_{TH} variations induced by LER are reduced in FinFET devices, fin edge roughness (i.e., LER along the channel length direction) has emerged as one of the most critical random variation sources along with WFV [10]. This chapter covers (i) the root causes of LER, (ii) the method of quantitative characterization for LER profiles, and (iii) the effect of the double patterning technique on LER profiles.

2.2 Physical Origin of Line Edge Roughness

In the photo-lithography step, the pattern drawn on the mask is transferred to the resist layer because the solubility of the resist layer varies depending on whether the resist is exposed to light or not. In order to increase the sensitivity to light, chemical

amplification is quite often used. In this process, chemically amplified resists are exposed to light in order to create acids. These acids then catalyze polymer deprotection during the post-exposure bake step. The deprotected portions of the resist can be easily dissolved with developer, thereby producing the resist pattern. The final LER profile contains all of the accumulated variations of each preceding processing step. In the following sections, the physical origins of LER will be introduced, followed by a discussion of each.

2.2.1 *LER of Mask Patterns*

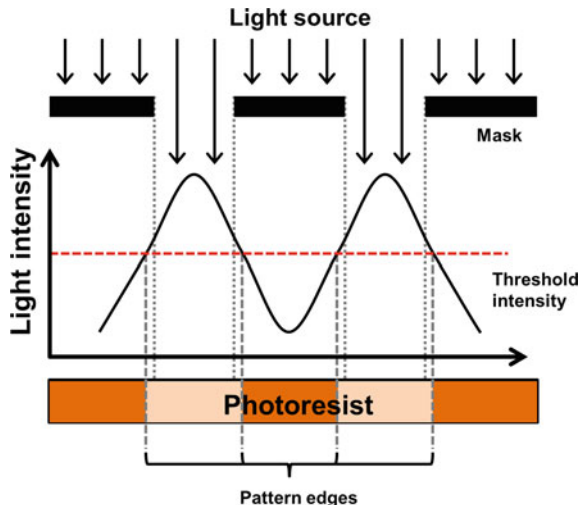
When considering LER, any roughness in mask patterns would appear to be a root-cause of LER. If mask patterns themselves have LER, and lithography techniques are able to transfer that LER without distortion, the projected patterns on the resist layer will have the identical LER profile of the mask patterns. In reality, fluctuations in the mask edge are unavoidable and the mask patterns themselves have roughness. However, the amount of roughness present is small enough to neglect when compared with the original pattern size. It is technically impossible to transfer minute patterns (i.e., roughness of the mask patterns) in current 193 nm lithography. Thus, the LER inherent in the mask patterns cannot contribute to the LER of resist patterns.

2.2.2 *Variations in the Dose of Light Exposure*

The resolution achieved in lithography techniques primarily depends on the size of projection lens used, because the aperture (or diameter) of the projection lens determines the diffraction order. Essentially, a lens with infinite size is required to collect all diffraction orders; however, an actual lens has a finite size. This reality tends to limit the resolution of lithography techniques. The consequence is that the shape of the exposure light intensity that arrives at the resist surface is not in the shape of a step function, but rather, the shape of a sinc function (i.e., the intensity of the exposure light has a certain gradient) (Fig. 2.2). We assume that, if the intensity of exposure light is equal to the threshold intensity or higher, the resist deprotection is activated by acids and can then be easily dissolved out. The edge of the resist pattern is the point where the intensity of the exposure light is identical to the threshold dose. In order to quantitatively understand the aerial image contrast at the edge of the feature, the image log-slope (ILS) is introduced:

$$\text{ILS} = \frac{1}{I_{\text{Edge}}} \left. \frac{\partial I(x)}{\partial x} \right|_{\text{Edge}},$$

Fig. 2.2 Schematic for the photo-lithography step. Note that the pattern edges are not exactly matched to the mask edges because of the gradient of light intensity



where I_{Edge} and $\left. \frac{\partial I(x)}{\partial x} \right|_{Edge}$ are the light intensity at the edge and the intensity slope at the edge, respectively [11].

As each step in the lithography process is completed during fabrication, the intensity of the exposure light in each step tends to fluctuate due to undesirable effects, such as variations in the laser's output power, vibrations in the optical system, miniscule up-and-down movements in the wafer stage, and/or fluctuations in the total dose due to light quantization. Because the edges of resist patterns are determined by the light intensity, fluctuations in exposure light intensity are one of the root-causes of LER (Fig. 2.2). If the slope of the light intensity at the edge of a pattern is steeper, the fluctuation of the edge is decreased. Thus, a large contrast between light and dark (i.e., a steep gradient of light intensity) is required in order to alleviate LER. The decrease in LER with increasing aerial image contrast has been experimentally observed [12]. It is worth noting that, even if the aerial image contrast is continuously increased, the LER becomes saturated at 5 nm. Beyond this point, any residual LER comes from the intrinsic material roughness of the resist [13].

2.2.3 LER Generation in Chemically Amplified (CA) Resists

In CMOS fabrication, chemical amplification is exploited to increase the sensitivity of the photoresist. Chemically amplified photoresist contains the photoacid generators shown in Fig. 2.3. When the photoacid generators in a chemically amplified photoresist film absorb energy from the light, they are decomposed into acid cations and other anions [14]. This decomposition process is referred to as deprotection. During the post-exposure bake step, the generated acids diffuse within the resist film and help to catalyze deprotection reactions [14, 15]. The acids are not

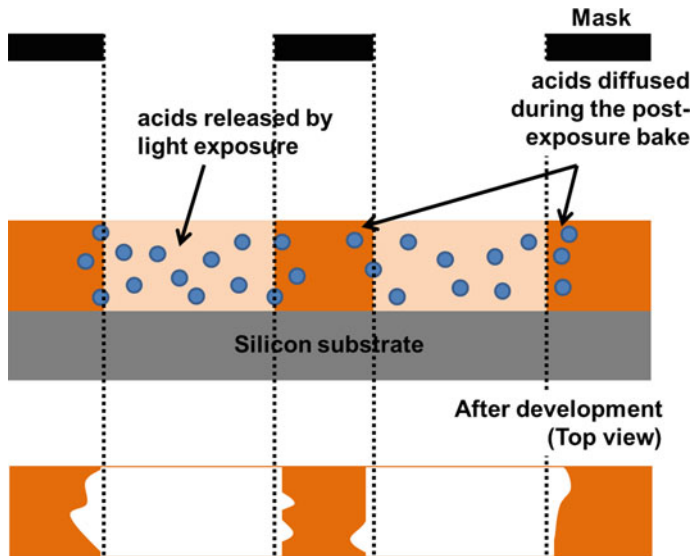


Fig. 2.3 LER, in chemically amplified resists, is formed because of acid diffusion during the post-exposure bake step

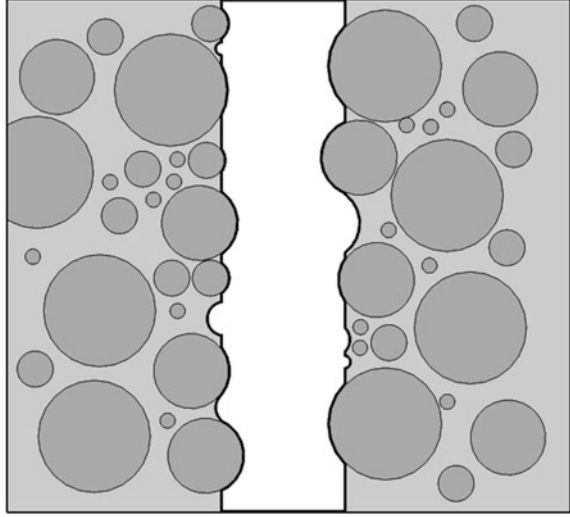
consumed but continue to exist within the deprotection reactions, and therefore are able to repeatedly catalyze the reactions. Because the acids change the solubility of polymer, the deprotected polymer regions are selectively removed with developer so that the patterns on the mask can be transferred to the resist film.

However, since the acids are randomly diffused within the resist films, this causes LER. During the post-exposure bake step, (i) bake temperature, (ii) the local extent of the deprotection reaction, and (iii) the concentration of reaction byproducts have an effect on the diffusion coefficient of the acid [16]. The diffusion distance of acid molecules is several tens of nanometers [17]. However, it is very difficult to completely control the diffusion rate because the temperature, the local extent of the reaction, and the concentration of byproducts are not constant over the baking process. Therefore, it is possible that some acids will diffuse over the target edge. If unexposed regions are sufficiently deprotected by these acids, they will be dissolved by developer, thereby causing higher frequency components in the LER (Fig. 2.3) to increase.

2.2.4 Intrinsic Roughness of the Resist

Even though other sources of LER can be excluded, intrinsic non-uniformities in photoresists cause LER along the side edges [18]. For instance, even if there is no variation in exposure light intensity, the photon absorption of photoresists varies

Fig. 2.4 Schematic of LER due to various sizes in the polymer chains of a photoresist



with physical position. Assuming uniform photon absorption, random dissolution and different sizes in the polymer chains of photoresists produces the roughness at the edge of the pattern (see Fig. 2.4). Furthermore, along the edges of the exposed patterns, some of the polymer molecules can smear into the developer while remaining anchored to the rest of the resist film. During the de-ionized water rinse, these partially dissolved polymer chains are re-deposited on the resist and redefine the edges of the patterns [19].

2.3 Characterization of Line Edge Roughness

2.3.1 Line Edge Roughness (LER)

LER can be measured by high resolution critical dimension scanning electron microscopes (CD-SEMs). In order to obtain the amount of LER, the local position of the line edge is first measured at regular intervals (i.e., Δ). Then, the average edge and the standard deviation of the line edge are defined as follows:

$$\bar{x} = \left(\sum_{i=1}^N x_i \right) / N \quad \sigma_{\text{LER}} = \sqrt{\frac{1}{N} \sum_{i=1}^N (\delta x_i)^2} = \sqrt{\frac{1}{N} \sum_{i=1}^N (x_i - \bar{x})^2},$$

where x_i is the local position measured at the i th point of the line edge. However, the average and standard deviation cannot provide us with a complete description of

the LER profile because they do not include information about the spatial aspect of the LER profile (i.e., spatial frequency of the LER profile) (Fig. 2.5).

According to the self-affine edge model [20], LER and its spatial aspect can be fully described using three parameters: (i) root-mean-square (RMS) deviation (σ), (ii) correlation length (ζ), and (iii) fractal dimension (D). These three parameters can be calculated using different methods, namely, the height–height correlation function (HHCF) [21–23], the Fourier transform, or the power spectral density (PSD) [24, 25]. The correlation length (ζ) is defined as the value of the domain in which the autocorrelation function is $1/e$ or the HHCF is 1.125σ (see Fig. 2.6a) [26].

Three parameters can be calculated from the plots, namely, RMS (σ), correlation length (ζ), and fractal dimension (D). The details of each function are as follows:

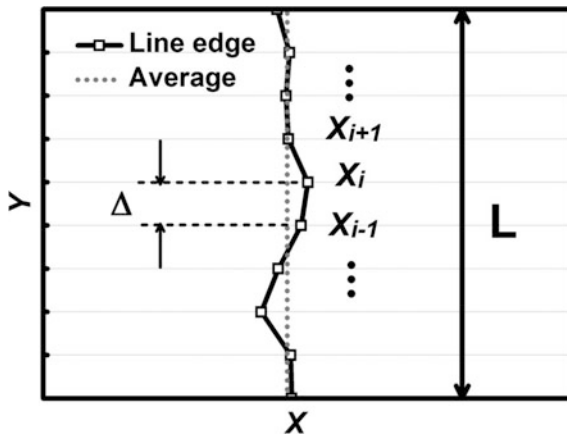


Fig. 2.5 An exemplary LER profile

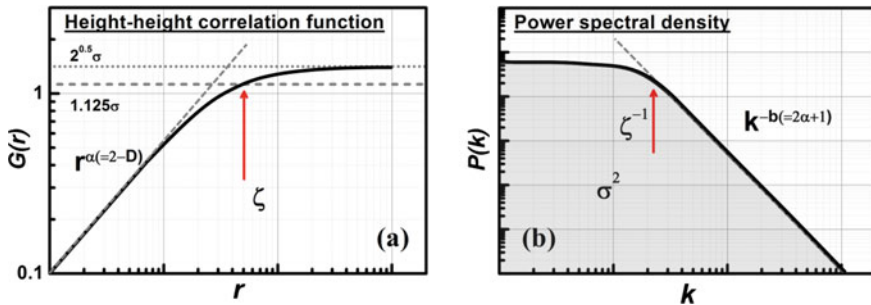


Fig. 2.6 **a** The height-height correlation function and **b** the power spectral density for an LER profile

$$G(md) = \left[\frac{1}{N-m} \sum_{i=1}^{N-m} (y_{i+m} - y_i) \right]^{1/2} \quad (\text{HHCF})$$

$$R(r = md) = \frac{1}{\sigma^2} \sum_{i=1}^{N-m} (y_{i+m} - \langle y_i \rangle)(y_i - \langle y_i \rangle), \quad (\text{autocorrelation function})$$

$$G^2(r) = 2\sigma^2[1 - R(r)],$$

(relationship between the HHCF and the autocorrelation function)

$$R(\xi) = 1/e \Rightarrow G(\xi) = \sqrt{2\left(1 - \frac{1}{e}\right)}\sigma = 1.125\sigma \quad (\text{correlation length})$$

The correlation length means how closely the edge is correlated to its adjacent (neighboring) edge. In other words, as the value of the correlation length increases, the adjacent edge is located at a position that is similar to the position of the original edge, and the LER profile has flat hills and valleys. However, there is still a high frequency component, as shown in Fig. 2.7b. From the power spectral density (PSD), we can analyze the spatial frequency of roughness [27]. The power spectral density is obtained from the Fourier transformation of the LER profile, and provides information about the power density of spatial frequencies from $1/L$ to $1/\Delta$ (where L and Δ refer to the length of the measured line and the interval distance between measurements, respectively). Therefore, we know which spatial frequency is dominant in determining the overall LER profile. Moreover, the RMS value can be obtained from the PSD using Parseval's theorem.

$$\sigma^2 = \sum_{j=1}^N P(k_j).$$

On the other hand, the PSD can be approximately defined as a power law in accordance with the self-affinity model.

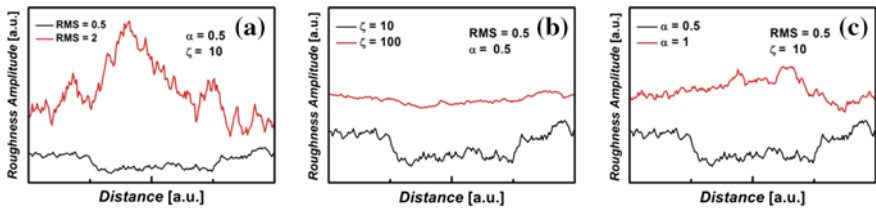


Fig. 2.7 LER profile with different **a** RMS deviation, **b** correlation length, and **c** fractal dimension (i.e., roughness exponent)

$$(P(k) \approx k^{-b}) \quad \text{for } k > \xi^{-1} \quad b = 2\alpha + 1,$$

The roughness exponent α , which is associated with fractal dimension (D) (i.e., $\alpha = 2 - D$), can be extracted from the slope of the PSD using power law behavior [28, 29] (Fig. 2.6b). The fractal dimension indicates the high frequency components in the LER profile. For instance, if the value of fractal dimension is large, the slope of the power spectral density plot becomes steeper. As a result, high frequency components of the LER profile are removed, and the line edge is smoother (see Fig. 2.7c). When analyzing high frequency components of LER, the interval distance (Δ) between each sampling point in the LER profile is very important. Because the maximum measurable high frequency is determined by the interval distance (i.e., $f_{\text{Max}} = 1/\Delta$), roughness with spatial frequencies greater than f_{Max} cannot be measured. Thus, in order to use frequency sampling, an interval distance of 2 nm is recommended beyond 22 nm semiconductor technology nodes [30].

2.3.2 Line Width Roughness (LWR)

Both LER and LWR are used to estimate the amount of random variation induced by photo-lithography fabrication. LER is defined as the roughness of a single printed pattern edge, and LWR indicates the fluctuation in the physical distance between two printed pattern edges. LWR is mathematically related to LER, and can be measured using the same method that is used for LER. Assuming the measurement window covers the LWR of the gate pattern with channel length L, the width of two lines is calculated using measured positions of the left and right line at regular intervals, as follows:

$$w_i = x_i^R - x_i^L,$$

where x_i^L and x_i^R are the position of the left and right edge, respectively, measured at the i th interval. Then, the average and standard deviation of line width can be calculated as follows:

$$\bar{w} = \left(\sum_{i=1}^N w_i \right) / N. \quad \sigma_{\text{LWR}} = \sqrt{\frac{1}{N} \sum_{i=1}^N (\delta w_i)^2} = \sqrt{\frac{1}{N} \sum_{i=1}^N (w_i - \bar{w})^2}.$$

It can be inferred from this equation that there is a correspondence between the LWR and the LER at both the left and right edges of the resist line or layer. The standard deviation of LWR can be expressed using the standard deviation of LER at both the left and right edges as follows:

$$\begin{aligned}
\sigma_{\text{LWR}}^2 &= \frac{1}{N} \sum_{i=1}^N (w_i - \bar{w})^2 = \frac{1}{N} \sum_{i=1}^N [(w_i)^2] - (\bar{w})^2 \\
&= \frac{1}{N} \sum_{i=1}^N [(x_i^{\text{R}})^2] - (\bar{x}^{\text{R}})^2 + \frac{1}{N} \sum_{i=1}^N [(x_i^{\text{L}})^2] \\
&\quad - (\bar{x}^{\text{L}})^2 + 2\bar{x}^{\text{R}} \cdot \bar{x}^{\text{L}} - \frac{2}{N} \sum_{i=1}^N (x_i^{\text{R}} \cdot x_i^{\text{L}}) \\
&= (\sigma_{\text{LER}}^{\text{R}})^2 + (\sigma_{\text{LER}}^{\text{L}})^2 + 2 \left[\bar{x}^{\text{R}} \cdot \bar{x}^{\text{L}} - \frac{1}{N} \sum_{i=1}^N (x_i^{\text{R}} \cdot x_i^{\text{L}}) \right],
\end{aligned} \tag{2.3.1}$$

where $\sigma_{\text{LER}}^{\text{L}}$ and $\sigma_{\text{LER}}^{\text{R}}$ are the standard deviation of LER at the left and right edge, respectively. Equation (2.3.1) explicitly shows the relationship between LWR and LER. By replacing the last term in (2.3.1) with a cross-correlation coefficient (ρ_{X}), (2.3.1) can be simplified, as follows:

$$\sigma_{\text{LWR}}^2 = \sigma_{\text{L}}^2 + \sigma_{\text{R}}^2 - 2\rho_{\text{X}}\sigma_{\text{L}}\sigma_{\text{R}} \tag{2.3.2}$$

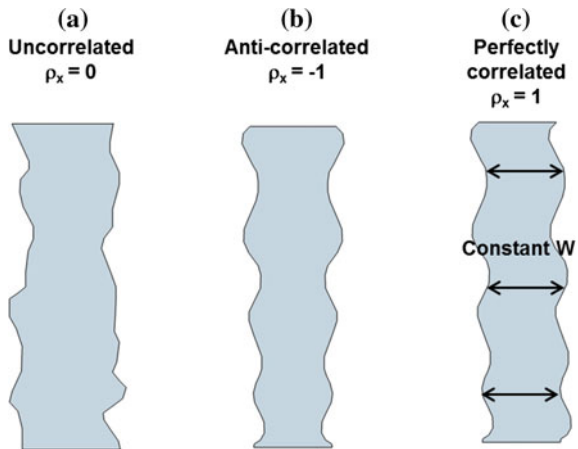
The value of the correlation factor depends on the method used when transferring the mask patterns, and its value is between -1 and 1 . Unless additional techniques, such as double, or triple, or even quadruple patterning techniques, are used for line formation, the roughness of two edges is generally uncorrelated. When the LERs of two edges are uncorrelated (i.e., $\rho_{\text{X}} = 0$), there is no resemblance between them (see Fig. 2.8a). Assuming $\sigma_{\text{LER}}^{\text{L}} = \sigma_{\text{LER}}^{\text{R}} \equiv \sigma_{\text{LER}}$, the standard deviation of LWR can be written as follows:

$$\sigma_{\text{LWR}} = \sqrt{2}\sigma_{\text{LER}}^{\text{L}} = \sqrt{2}\sigma_{\text{LER}}^{\text{R}}.$$

In the case of $\rho_{\text{X}} = -1$, we can say that the roughness of the two edges is in anti-correlation. The two anti-correlated edges simultaneously fluctuate with opposite amplitude (see Fig. 2.8b). Thus, in the worst case, the pattern is cut off in the middle of the line. However, if the value of $\rho_{\text{X}} = 1$, the two edges are completely correlated, and the LERs of each edge are exactly matched (see Fig. 2.8c). Because the distance between two edges along the line is consistent to the other distances between the other two edges along the line, the standard deviation of LWR is zero ($\sigma_{\text{LWR}} = 0$).

The standard deviation of LWR provides limited information about the roughness of two line edges [26, 31]. In order to investigate spatial spectral content, Patel et al. [32] introduced a formulation of the autocorrelation function that describes the cross-correlation of a line edge with itself at different points. With regard to a stationary LWR profile, it turns out that the autocorrelation between two points is a function of the distance between them. Similarly, in a jointly stationary LWR profile, the cross-correlation coefficient in (2.3.2) is a function of the distance between them.

Fig. 2.8 LER profile of two edges depending on the correlation between them. For the perfectly correlated case, LWR is completely removed



According to [33], an LWR profile can be conveniently described using the auto-correlation coefficient approximated by a closed-form expression, as follows:

$$\rho_A(y) = \exp\left[-(y/\xi)^{2\alpha}\right],$$

where y is the distance between two points, ξ is the correlation length, and α is the roughness exponent. Similar to LER, the correlation length indicates the distance over which the amplitudes of the two points along an edge can be almost uncorrelated. The roughness exponent is a relative measure of the high-frequency components in the roughness. Larger values mean fewer high-frequency amplitude variations. Figure 2.7 shows the impact of each parameter on roughness.

2.4 Impact of Double Patterning on Line Edge Roughness

2.4.1 Double Pattern and Double Etching

In order to enhance the resolution of the photoresist pattern without replacing the light source (e.g., from 193 nm to EUV), the double patterning technique was added to the lithography process for sub-32 nm nodes [9]. The double patterning technique has been widely adopted in industry for 22/20 nm technology and beyond. Note that the sequence of double patterning and double etching (2P2E) is an example of a double patterning technique. A comparison of the process flow between double patterning and double etching versus that of conventional patterning is shown in Fig. 2.9. In the double patterning technique, the Si-BARC and SOC are first coated onto the substrate. These layers preserve the original pattern through the 1st and 2nd lithography steps, and play a key role as a hard mask in the 2nd etching step. A photoresist layer is spin-coated onto Si-BARC

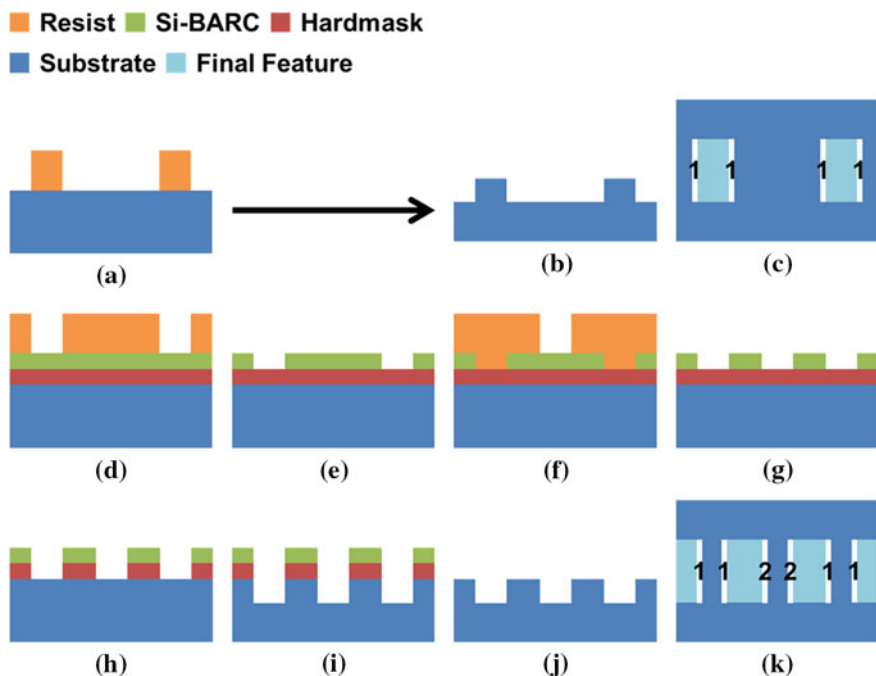


Fig. 2.9 Sequences of patterning processes for **a, b** 1P1E technique, and **d–j** 2P2E technique. Top view of the final feature for 1P1E and 2P2E is shown in **(c)** and **(k)**, respectively. Note that each line edge is denoted by “1” (“2”) to indicate that the line edge was affected by the first (second) patterning step

and the 1st pattern is projected by the 1st lithography process step (Fig. 2.9d). By the subsequent 1st etching step, the pattern on the resist is transferred to the Si-BARC, whereas the underlying substrate is etched in the conventional process (Fig. 2.9e, b). Next, another photoresist layer for the 2nd lithography step is spin-coated to fill out the 1st pattern on Si-BARC, and then the 2nd lithography step is performed (Fig. 2.9f). A thinner Si-BARC film can provide minimal impact on coating uniformity issues associated with coating the 2nd resist stack over the topography. The 2nd etching step is performed to transfer the pattern on the resist to the Si-BARC layer (Fig. 2.9g). Finally, the pattern is transferred from Si-BARC to SOC, and then from SOC to substrate (Fig. 2.9h–j). As a result, double patterning and double etching achieves finer patterns than conventional lithography while using identical light sources, photoresist, pitch size, and development method.

Because the LER profile is transferred through multiple etching processes, the LER profile on the substrate is different from the original LER profile on photoresist, Si-BARC, and SOC [34–39]. As the etching process is completed, the edges of the patterns tend to be smoothed. Using statistical and experimental data, it has been confirmed that the correlation length of the LER profile, based on the double patterning and double etching technique, is larger than that of the

conventional LER profile [9]. Thus, multiple etching processes induce smoother line edges with low spatial frequency and flat hills/valleys, and therefore can reduce LER [40, 41]. Furthermore, additional thermal treatment, such as post-applying bake and post-exposure bake between the 1st and the 2nd lithography, increases the correlation length of the LER profile [42].

2.4.2 Self-aligned Double Patterning

Although two separate lithography steps are required to double the resolution of photoresist patterns when using the double patterning and double etching technique, there is a totally different approach, namely, self-aligned double patterning, which requires only one exposure. Self-aligned double patterning is able to double the resolution of photoresist patterns using film deposition, etching, and CMP without additional lithography steps [43]. The process flow of self-aligned double patterning is reported in [44] (Fig. 2.10). A coated photoresist is patterned with a certain pitch (note that the pitch of the final pattern will be halved) through lithography and etching steps. Next, the pattern on the photoresist is transferred and printed on a sacrificial layer by plasma etching. Then, the sacrificial layer forms a dummy gate with the duty ratio of 1:3 (i.e., line/space = 1/3). Through the deposition of silicon nitride (Si_3N_4) and anisotropic etching, spacers are formed that have identical critical dimensions to the dummy gate (i.e., the duty ratio is 1:1). The dummy gate is eliminated by an isotropic etching step, leaving only the spacer pattern on the stacked film. Finally, using the Si_3N_4 spacers as a mask for etching, the spacer patterns are transferred and printed to the hard mask. As a result of using self-aligned double patterning, the original pitch of the photoresist is decreased by

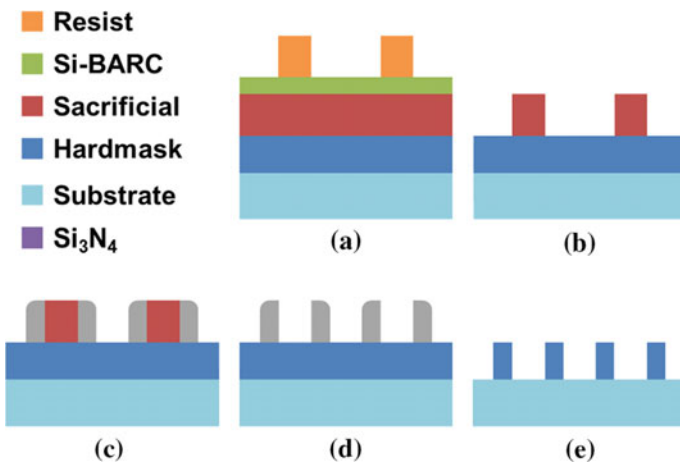


Fig. 2.10 Process flow of the self-aligned double patterning technique

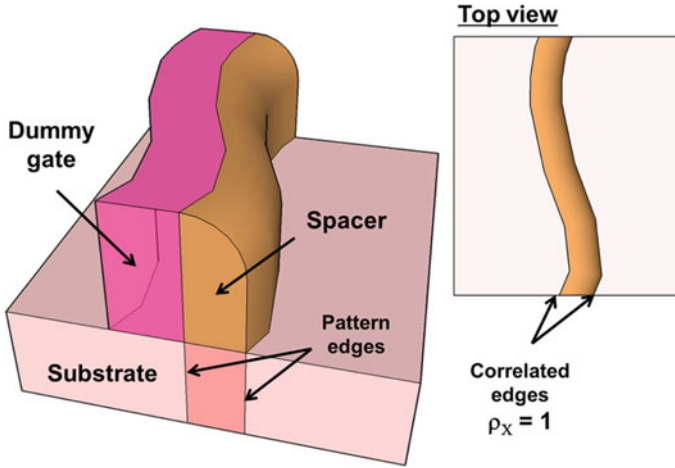


Fig. 2.11 Illustration of the self-aligned double patterning technique. This method can virtually eliminate the amount of LWR because it leads to perfectly correlated line edges

50 % in the final pattern. In other words, one resist line creates two spacers, thereby doubling the spatial frequency.

In the fabrication processes for FinFETs, the fin-shaped body can be patterned in two different ways: (1) using a resist as the mask (i.e., “resist defined”), and (2) using a spacer as the mask (i.e., “spacer-defined”). Conventional resist-defined lines create edges with uncorrelated roughness, and a ρ_x of 0 can be assumed. This is because the erosion of polymer aggregates is randomly processed for each resist edge. On the other hand, spacer-defined lines generate edges that are quite correlated. This is because of a conformal thin-film deposition process followed by a highly uniform anisotropic etch process. These preceding steps induce a spacer mask to be formed along the sidewall of a dummy resist-defined feature (Fig. 2.11). If the spacer width (corresponding to the thickness of the deposited film) is negligible (versus the inverse value of the LWR spatial frequency), the spacer-defined lines have a uniform width. Hence, a ρ_x of 1 can be assumed. In summary, if the self-aligned double patterning technique is used in the FinFET fabrication process, the performance variation induced by LWR (not LER) can be virtually eliminated.

References

1. Hashimoto K, Uesawa F, Takahata K, Kikuchi K, Kanai H, Shimizu H, Shiobara E, Takeuchi K, Endo A, Harakawa H, Miniutogi S (2003) ArF lithography technologies for 65 nm-node CMOS (CMOSS) with 30 nm logic gate and high density embedded memories. In: Symposium on VLSI Technology Digest, pp 45–46
2. Lin BJ (1987) The future of subhalf-micrometer optical lithography. *Microcircuit Eng* 6 (1):31–51

3. Narasimha S, Onishi K, Nayfeh HM, Waite A, Weybright M, Johnson J, Fonseca C, Corliss D, Robinson C, Crouse M, Yang D, Wu C-HJ, Gabor A, Adam T, Ahsan I, Belyansky M, Black L, Butt S, Cheng J, Chou A, Costrini G, Dimitrakopoulos C, Domenicucci A, Fisher P, Frye A, Gates S, Greco S, Grunow S, Hargrove M, Holt J, Jeng S-J, Kelling M, Kim B, Landers W, Larosa G, Lea D, Lee MH, Liu X, Lustig N, McKnight A, Nicholson L, Nielsen D, Nummy K, Ontalus V, Ouyang C, Ouyang X, Prindle C, Pal R, Rausch W, Restaino D, Sheraw C, Sim J, Simon A, Standaert T, Sung CY, Tabakman K, Tian C, Van Den Nieuwenhuizen R, Van Meer H, Vayshenker A, Wehella-Gamage D, Werking J, Wong RC, Yu J, Wu S, Augur R, Brown D, Chen X, Edelstein D, Grill A, Khare M, Li Y, Luning S, Norum J, Sankaran S, Schepis D, Wachnik R, Wise R, Wann C, Ivers T, Agnello P (2006) High performance 45-nm SOI technology with enhanced strain, porous low-k BEOL, and immersion lithography. In: *Proceedings of IEEE IEDM*, pp 1–4
4. Chen H-Y, Chang C-Y, Huang C-C, Chung T-X, Liu S-D, Hwang J-R, Liu Y-H, Chou Y-J, Wu H-J, Shu K-C, Huang K-K, You J-W, Shin J-J, Chen C-K, Lin C-H, Hsu J-W, Perng B-C, Tsai P-Y, Chen C-C, Shieh J-H, Tao H-J, Chen S-C, Gau T-S, Yang F-L (2005) Novel 20 nm hybrid SOI/Bulk CMOS technology with $0.183\ \mu\text{m}^2$ 6T-SRAM cell by immersion lithography. In *Symposium on VLSI Technology Digest*, pp 16–17
5. Chandhok M, Datta S, Lionberger D, Vesecky S (2007) Impact of line width roughness on Intel's 65 nm process devices. In: *Proceedings of SPIE*, p 65191A
6. Shin C, Damrongplasit N, Sun X, Liu T-JK (2011) Performance and yield benefits of quasi-planar bulk CMOS technology for 6-T SRAM at the 22-nm node. *IEEE Trans Electron Devices* 58(7):1846–1854
7. Shin C, Tsai CH, Wu MH, Chang CF, Liu YR, Kao CY, Lin GS, Chiu KL, Fu C-S, Tsai C, Liang CW, Nikolić B, Liu T-JK (2011) Quasi-planar bulk CMOS technology for improved SRAM scalability. *Solid-State Electron* 65–66:184–190
8. Shin C, Cho MH, Tsukamoto Y, Nguyen B-Y, Mazuré C, Nikolić B, Liu T-JK (2010) Performance and area scaling benefits of FD-SOI technology for 6-T SRAM cells at the 22-nm node. *IEEE Trans Electron Devices* 57(6):1301–1309
9. Shin C, Park IJ (2013) Impact of using double-patterning versus single patterning on threshold voltage (V_{TH}) variation in quasi-planar tri-gate bulk MOSFETs. *IEEE Electron Device Lett* 34(5):578–580
10. Wang X, Brown AR, Cheng B, Asenov A (2011) Statistical variability and reliability in nanoscale FinFETs. In: *Proceedings of IEEE IEDM*, pp 5.4.1–5.4.4
11. Wei Y, Brainard RL (2009) Advanced processes for 193-nm immersion lithography. *SPIE*, Bellingham
12. Pawloski AR, Acheta A, Bell S, La Fontaine B, Wallow T, Levinson HJ (2006) The transfer of photoresist LER through etch. In: *Proceedings of SPIE*, p 615318
13. Tsubaki H, Yamanaka T, Nishiyama F, Shitabatake K (2007) A study on the material design for the reduction of LWR. In: *Proceedings of SPIE*, p 651918
14. Tagawa S, Nagahara S, Iwamoto T, Wakita M, Kozawa T, Yamamoto Y, Werst D, Trifunac AD (2000) Radiation and photochemistry of onium salt acid generators in chemically amplified resists. In: *Proceedings of SPIE*, p 204
15. Wang X-B, Ferris K, Wang L-S (2000) Photodetachment of gaseous multiply charged anions, copper phthalocyanine tetrasulfonate tetraanion: tuning molecular electronic energy levels by charging and negative electron binding. *J Phys Chem A* 104(1):25–33
16. Stewart MD, Tran HV, Schmid GM, Stachowiak TB, Becker DJ, Willson CG (2002) Acid catalyst mobility in resist resins. *J Vac Sci Technol*, B 20(6):2946–2952
17. Hinsberg WD, Houle FA, Sanchez MI, Hoffnagle JA, Wallraff GM, Medeiros DR, Gallatin GM, Cobb JL (2003) Extendibility of chemically amplified resists: another brick wall? In: *Proceedings of SPIE*, p 1
18. Nam H, Lee GS, Lee H, Park IJ, Shin C (2014) Analysis of random variations and variation-robust advanced device structures. *J Semicond Technol Sci* 14(1)

19. Prabhu VM, Vogt BD, Kang S, Rao A, Lin EK, Satij SK, Turnquest K (2007) Direct measurement of the in situ developed latent image: the residual swelling fraction. In: *Proceedings of SPIE*, p 651910
20. Zhao Y (2001) *Characterization of amorphous and crystalline rough surface: principles and applications*. Academic Press, San Diego
21. Constantoudis V, Patsis GP, Tserepi A, Gogolides E (2003) Quantification of line-edge roughness of photoresists. II. Scaling and fractal analysis and the best roughness descriptors. *J Vac Sci Technol B* 21:1019–2003
22. Patsis GP, Constantoudis V, Tserepi A, Gogolides E, Grozev G, Hoffmann T (2002) Roughness analysis of lithographically produced nanostructures: off-line measurement and scaling analysis. *Microelectron Eng* 67–68:319–325
23. Constantoudis V, Patsis GP, Gogolides E (2003) Photoresist line-edge roughness analysis using scaling concepts. In: *Proceedings of SPIE*, p 901
24. Yamaguchi A, Tsuchiya R, Fukuda H, Komuro O, Kawada H, Iizumi T (2003) Characterization of line-edge roughness in resist patterns and estimations of its effect on device performance. In: *Proceedings of SPIE*, p 689
25. Bunday BD, Bishop M, Villarrubia JS, Vladar AE (2003) CD-SEM measurement line-edge roughness test patterns for 193-nm lithography. In *Proceedings of SPIE*, p 674
26. Constantoudis V, Patsis GP, Leunissen LHA, Gogolides E (2004) Line edge roughness and critical dimension variation: fractal characterization and comparison using model functions. *J Vac Sci Technol B* 22(4):1974–1981
27. Naulleau PP, Cain JP (2007) Experimental and model-based study of the robustness of line-edge roughness metric extraction in the presence of noise. *J Vac Sci Technol B* 25 (5):1647–1657
28. Barabasi A-L, Stanley HE (1995) *Fractal concepts in surface growth*. Cambridge University Press, Cambridge
29. Zhao BY, Wang G-C, Lu T-M (2001) *Characterization of amorphous and crystalline rough surface: principles and applications experimental methods in the physical sciences academic*, New York
30. Bunday BD, Bishop M, McCormack D, Villarrubia JS, Vladar AE, Dixon R, Vorburger T, Orji NG, Allgair JA (2004) Determination of optimal parameters for CD-SEM measurement of line edge roughness. In: *Proceedings of SPIE*, p 515
31. Constantoudis V, Gogolides E, Roberts J, Stowers J (2005) Characterization and modeling of line width roughness (LWR). In: *Proceedings of SPIE*, p 1227
32. Patel K, Liu T-JK, Spanos CJ (2009) Gate line edge roughness model for estimation of FinFET performance variability. *IEEE Trans Electron Devices* 56(12):3055–3063
33. Palasantzas G (1993) Roughness spectrum and surface width of self-affine fractal surfaces via the K-correlation model. *Phys Rev B Condens Matter* 48(19):14472–14478
34. Mahorowala P, Babich K, Lin Q, Medeiros DR, Petrillo K, Simons J, Angelopoulos M, Sooriyakumaran R, Hofer D, Reynolds GW, Taylor JW (2000) Transfer etching of bilayer resists in oxygen-based plasmas. *J Vac Sci Technol A* 18(4):1411–1419
35. Mahorowala AP, Goldfarb DL, Temple K, Petrillo KE, Pfeiffer D, Babich K, Angelopoulos M, Gallatin GM, Rasgon S, Sawin HH, Allen SD, Lang RN, Lawson MC, Kwong RW, Chen K-J, Li W, Varanasi PR, Sanchez MI, Ito H, Wallraff GM, Allen RD (2003) Impact of thin resist processes on post-etch LER. In: *Proceedings of SPIE*, p 213
36. Montgomery PK, Peters R, Garza C Sr, Cobb J, Darlington B, Parker C, Filipiak S, Babbitt D (2005) Reduction of line edge roughness and post resist trim pattern collapse for sub 60 nm gate patterns using gas-phase resist fluorination. In: *Proceedings of SPIE*, p 1024
37. Namatsu H, Nagase M, Yamaguchi T, Yamazaki K, Kurihara K (1998) Influence of edge roughness in resist patterns on etched patterns. *J Vac Sci Technol B* 16(6):3315–3321
38. Ren F, Pearton SJ, Lothian JR, Abernathy CR, Hobson WS (1992) Reduction of sidewall roughness during dry etching of SiO₂. *J Vac Sci Technol B* 10(6):2407–2411
39. Ren F, Pearton SJ, Shul RJ, Han J (1998) Improved sidewall morphology on dry-etched SiO₂ masked GaN features. *J Electron Mater* 27(4):175–178

40. Wallow T, Acheta A, Ma Y, Pawloski A, Bell S, Ward B, Tabery C, Fontaine BL, Kim R-H, McGowan S, Levinson HJ (2007) Line-edge roughness in 193-nm resists: lithographic aspects and etch transfer. In: Proceedings of SPIE, p 651919
41. Goldfarb DL, Mahorowala AP, Gallatin GM, Petrillo KE, Temple K, Angelopoulos M, Rasgon S, Sawin HH, Allen SD, Lawson MC, Kwong RW (2004) Effect of thin-film imaging on line edge roughness transfer to underlayers during etch processes. *J Vac Sci Technol B* 22 (2):647–653
42. Steenwinckel DV, Lammers JH, Leunisse LHA, Kwinten JAJM (2005) Lithographic importance of acid diffusion in chemically amplified resists. In: Proceedings of SPIE, p 269
43. Hand A (2007) Applied's litho scheme: patterning vs. printing. *Semiconductor International*, April 2007
44. Mukai H, Shiobara E, Takahashi S, Hashimoto K (2007) A study of CD budget in spacer patterning technology. In: Proceedings of SPIE, p 692406

<http://www.springer.com/978-94-017-7595-3>

Variation-Aware Advanced CMOS Devices and SRAM

Shin, C.

2016, VII, 140 p. 118 illus., 101 illus. in color.,

Hardcover

ISBN: 978-94-017-7595-3