

# Bulk FinFETs: Design at 14 nm Node and Key Characteristics

Jong-Ho Lee

**Abstract** In contrast to conventional 2-D MOSFETs, FinFETs are able to be scaled down to 20 nm and beyond, and have superior performance. There are two types of FinFETs: SOI FinFETs and bulk FinFETs. Bulk FinFETs are built on bulk-Si wafers, which have less defect density and are cheaper than SOI wafers, while also having better heat transfer rate to the substrate compared to SOI FinFETs. In 2011, Intel announced the world's first 3-D transistors in the mass production of a 22 nm microprocessor (code-named Ivy Bridge). The 3-D transistors adopted by Intel are actually bulk FinFETs. In this chapter, we provide the design guidelines for bulk FinFETs at the 14 nm node, and compare bulk and SOI FinFETs in terms of scalability, parasitic capacitance, and heat dissipation. Decrease of the drain current by parasitic resistance in the source (S) and drain (D) regions is also addressed. Drain current fluctuation by single charge trap is studied in terms of the trap depth, trap position, and percolation path. In the design of 14 nm bulk FinFETs, a punch-through stopper at a position just under the S/D junction depth is required to suppress unwanted cross-talk between S and D. The peak concentration of the stopper needs to be  $2\text{--}3 \times 10^{18} \text{ cm}^{-3}$ . The S/D junction depth should be equal or slightly smaller than the height of fin body, defined from the surface of the isolation oxide region to the top of the fin body. Considering the short channel effect and drain current drivability, the reasonable doping concentration of uniformly doped fin body is  $2\text{--}3 \times 10^{17} \text{ cm}^{-3}$ . To keep the drain-induced barrier below 100 mV/V when the length between the S and D junctions is the same as the gate length (14 nm), the width of the fin body should be  $\sim 9$  nm. Under the same doping concentration and geometry, both 14 nm SOI and bulk FinFETs have nearly the same  $I\text{--}V$  characteristics, which mean nearly the same scalability. Since thin fin bodies protruding from the substrate are easily depleted, the junction capacitance of the S/D to fin body can be reduced to similar or even lower values than that of SOI FinFETs. To achieve a similar heat transfer rate to the substrate as

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bulk FinFETs, the buried oxide in SOI FinFETs should be thinned down to 20 nm or beyond, which could cause unwanted increase in the parasitic capacitance. The contact area between the metal electrode and the *S/D* region should be as wide as possible to reduce the *S/D* parasitic resistance.

**Keywords** Bulk FinFET · Punch-through stopper · Body width · Body doping · Channel length · Fin height · Contact resistance · Capacitance · Temperature

## 1 Introduction

The basic concept of the field effect transistor (FET) was patented by Lilienfeld [1] in 1930, but was not implemented at that time because of the unavailability of practical means. The first oxides grown in high pressure steam were used by Kahang and Atalla [2] to fabricate the first MOSFET structures in 1960. In 1963, Grove, Deal, and Snow developed the first commercially available process for the construction of MOSFETs with stable characteristics [3]. Since around 1960, MOSFETs with planar (or two-dimensional) channel structure have been applied to integrated circuits (ICs) for the cheap and efficient performance of functions such as digital and mixed signal processing, signal amplification, computing, and information storage. Thus, silicon MOSFETs have emerged since the 1980s as the predominant technology of the microelectronics industry. MOSFETs have been scaled down consistently over many generations of technology manufacturing, resulting in steady improvements in circuit performance (speed), integration density, and cost per function (or bit). The gate lengths of MOSFETs were reduced from the  $\mu\text{m}$  range to several tens of nm. Conventional nanoscale bulk-Si MOSFETs suffer from increase of the off-current ( $I_{\text{OFF}}$ ) as one of the short channel effects (SCEs). One method to suppress such short channel effects is to reduce the thickness of the gate oxide, but use of a thin gate oxide increases the gate leakage current. Nanoscale devices require low-resistance, ultra-shallow source/drain junction depth, ultrathin equivalent gate oxide thickness using high- $\kappa$  dielectrics, and low-resistance metal (or silicide) gate electrodes to meet the specifications of the ITRS [4]. Because of these requirements, it is well known that the scaling-down of bulk MOSFETs with planar channel structure beyond 20 nm is nearly impossible. One of the technology boosters for future technology generations is device structure. Advanced device structures include ultrathin body silicon on insulator (SOI) single-gate transistors [5, 6] and double/triple-gate (or multiple gate) transistors [7–9], both of which have better device scalability than classic bulk-Si transistors [10]. Thus, better device architecture will be necessary to continue achieving the benefits obtained from device scaling in the past. Double-gate (DG) MOSFETs that have top and bottom gates or left and right gates have long been recognized for their potential to better control the SCEs. Triple-gate (TG) MOSFETs display similar behaviors to the DG devices, but have three gate electrodes on the three surfaces of the rectangular-shaped body. Several different

structures for DG and TG MOSFETs have been proposed or demonstrated experimentally [11, 12]. For decades, various kinds of three-dimensional (3-D) transistors have been reported [7–48]. Among them, FinFETs have become the predominant technology because the fabrication process of the device structure is relatively easy and compatible to that of conventional planar channel MOSFETs. Intel announced the mass production of CPUs based on 22 nm 3-D transistors in 2011 [44]. The 3-D transistor was called tri-gate or bulk FinFET. The bulk FinFET was developed at the 14 nm technology node, and is ready to be applied in mass production. Research on the development of FinFET is ongoing at 10 nm [40, 46, 47] and even 7 nm [36, 38] technology node. However, no systematic design guideline on the design of channel and source/drain contact has been presented. Therefore, in this chapter, we focus on the analysis of intrinsic device performance and source/drain contact resistance of the bulk FinFET at the 14 nm node and provide a design guideline of the device.

## 2 SOI and Bulk FinFETs

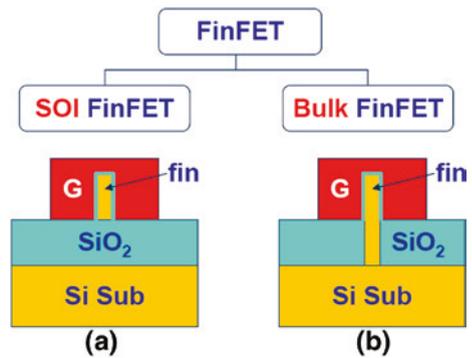
First of all, the key properties of SOI and bulk FinFETs are explained briefly in this section. FinFETs [7, 8, 15–48] seem to be very promising for the future CMOS technology including logic and memory applications. As mentioned in the introduction, FinFETs basically have a double-gate structure which yields excellent scaling-down characteristics and high performance. FinFETs have been in development for various applications, such as high speed digital integrated circuits (ICs) [17–21], analog ICs [22, 23], SRAMs [24–26], flash memories [27–31], and DRAMs [32–35].

FinFETs were known to most of us as those fabricated on SOI wafers in the late 1990s and early 2000s, which were basically SOI MOSFETs. When double-gate transistors were first reported, they were mainly demonstrated on SOI substrates to overcome the problems associated with short channel effect (SCE) [7, 9, 11, 15–20]. The FinFETs built on SOI wafers are referred to as SOI FinFETs. These devices are known to have the advantages of easy fabrication and excellent scalability, because no shallow trench isolation (STI) process is required, and they have no leakage path near the junction depth of the source/drain regions. These SOI devices are normally applied to high speed circuits due to their low parasitic capacitances. In general, floating body SOI devices, including single- and double-gate devices, may have floating body problems [49] depending on their doping, Si film thickness, and bias conditions. SOI wafers have higher wafer cost and higher defect density than bulk-Si wafers. Note that the heat generated in the channel of SOI FETs cannot be easily dissipated to the substrate due to the thick buried oxide with a very poor heat transfer rate. Switching from conventional planar MOSFETs to the SOI FinFET means not only active splitting [16] for narrow and depleted channels, but also changing from conventional four-terminal devices to three-terminal (body floating) ones. Consequently, this narrows the circuit operation

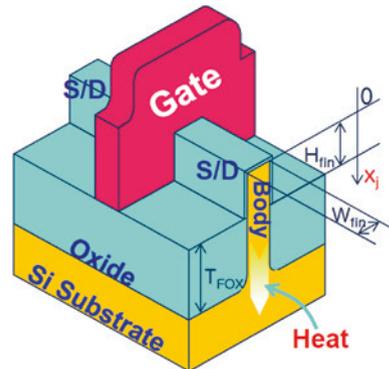
windows because of the three-terminal characteristics. Therefore, it would be more appropriate to consider four-terminal FinFETs achieved by connecting the fin body directly to the Si substrate. These four-terminal FinFETs are built on bulk-Si wafers and called body-tied FinFETs, or preferably, bulk FinFETs [26]. When body-tied FinFETs were first reported, they were referred to as Omega ( $\Omega$ ) MOSFETs because the cross-section of the body resembles the Greek letter  $\Omega$ . F.-L. Yang et al. called their MOSFET as omega FET when it was reported in 2002 IEDM, because the gate structure looks like  $\Omega$  [16]. To differentiate the body-tied FinFET from the SOI FinFET and the omega FET, we therefore called the body-tied FinFET a bulk FinFET. A brief explanation of FinFET classification is provided in Fig. 1, which shows cross-sectional views of the SOI and bulk FinFETs with the cut fin body. The fin bodies of the SOI and bulk FinFETs are floated and tied to the substrate, respectively. “G” stands for gate electrode.

Bulk FinFETs are more familiar to IC design engineers compared to three-terminal FETs, and the fabrication steps of the devices are compatible with those of the conventional planar (or 2-D) channel CMOS devices fabricated on bulk-Si wafers. A schematic 3-D view of the bulk FinFET is shown in Fig. 2. Here,  $W_{\text{fin}}$

**Fig. 1** FinFET classification, and cross-sectional views of SOI (a) and bulk (b) FinFETs



**Fig. 2** Three-dimensional schematic of bulk FinFET.  $H_{\text{fin}}$  and  $W_{\text{fin}}$  represent fin height and width, respectively.  $T_{\text{FOX}}$  and  $x_j$  stand for the field oxide thickness and the source/drain junction depth, respectively



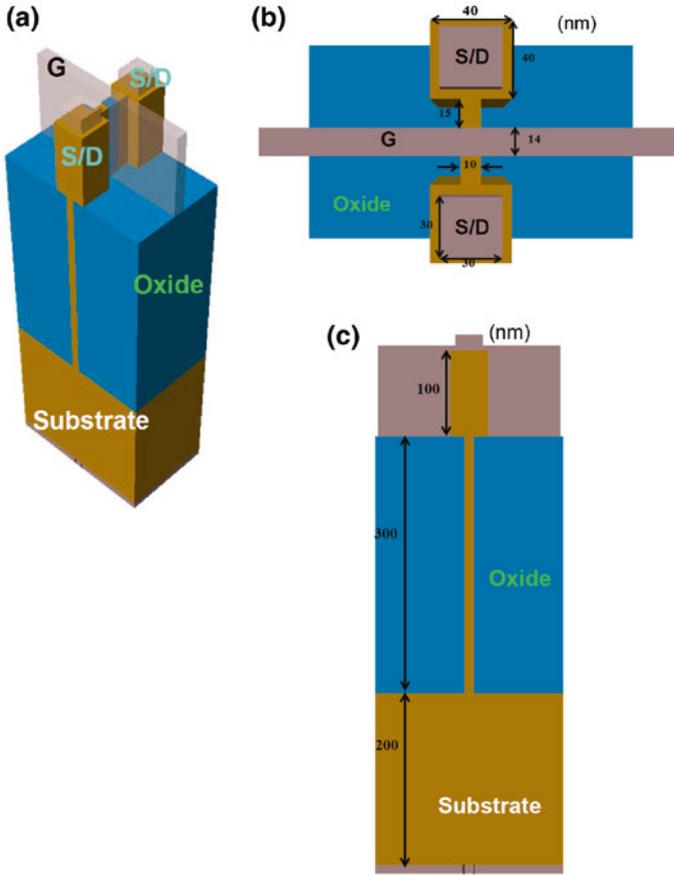
and  $H_{\text{fin}}$  represent the fin body width and fin height, respectively. The fin height is defined as the height from the surface of the oxide isolation region to the top of the fin body.  $T_{\text{FOX}}$  represents the thickness of the field oxide for device isolation. The source/drain junction depth is represented by  $x_j$ . The heat generated in the channel can be transferred to the substrate through the fin body, which is connected to the substrate.

The design of bulk FinFETs eliminates the problems associated with SOI FinFETs, such as expensive wafer cost, high defect density, floating body effect, and poor heat dissipation. In addition, they keep nearly the same scalability as SOI FinFETs while having better heat dissipation characteristics [50]. The key properties of the bulk FinFET will be explained in detail in the chapter on device design at the 14 nm node, and later compared with those of SOI FinFETs.

### 3 Design of 14 nm Bulk FinFET

In this section, the key parameters are examined, including local doping to suppress punch-through, fin body doping, junction-to-junction length, and fin body width at the technology node of 14 nm. In the 22 nm technology node, the fin body shape looks trapezoidal (or tapered) [51, 52]. Such a body profile seems to easily form isolation oxide between the fins, though a rectangular (or vertical) profile gives better electrical performance [52]. However, at 14 nm and beyond, it becomes difficult to keep the same fin body profile in terms of device scalability and control of the fin body profile. Although bulk FinFET with a tapered fin body at 14 nm has been reported [36], it is reasonable to utilize a vertical fin body profile in the channel region and then a trapezoidal body which increases in width approaching the substrate [38, 39]. In this chapter, we adopt a vertical body profile in the channel region and provide key properties and design guidelines. For simplicity, the fin body protruding from the substrate has vertical side surfaces (rectangular body shape).

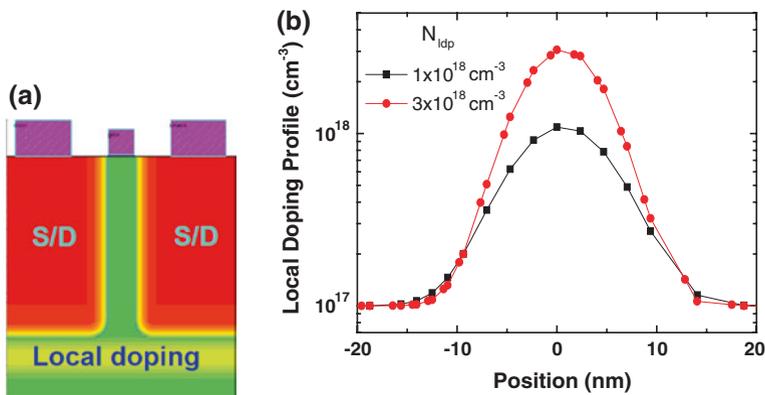
Figure 3a shows a 3-D view of a 14 nm bulk FinFET wherein the source and drain regions for the metal contact pad have an epitaxial layer. The top view of the FinFET is shown in Fig. 3b. The gate length ( $L_g$ ) and fin width ( $W_{\text{fin}}$ ) are 14 and 10 nm, respectively. The source and drain regions for metal contact pad are  $40 \times 40 \text{ nm}^2$ , and are located 15 nm away from the gate electrode. The size of the metal contact formed on the source and drain regions is  $30 \times 30 \text{ nm}^2$ , and ideal ohmic contact (interfacial contact resistivity,  $\rho_c = 0 \text{ } \Omega \text{ cm}^2$ ) is assumed. The gate oxide thickness is 1 nm. The source and drains are uniformly doped at the concentration of  $5 \times 10^{20} \text{ cm}^{-3}$ . In Fig. 3c, a cross-sectional view cut along the source or drain region across the channel length is shown. The fin height ( $H_{\text{fin}}$ ) and field oxide thickness ( $T_{\text{FOX}}$ ) are 100 and 300 nm, respectively. The metal contact for the substrate is formed on the bottom of the 200 nm thick substrate.



**Fig. 3** Three-dimensional view of a 14 nm bulk FinFET for device simulation (a). *Top view* of the FinFET (b). Gate length ( $L_g$ ) and Fin width ( $W_{fin}$ ) are 14 and 10 nm, respectively. Source and drain regions for the metal contact pad are  $40 \times 40 \text{ nm}^2$ . Cross-sectional view cut along the source or drain across the channel length (c). Fin height ( $H_{fin}$ ) and field oxide thickness ( $T_{FOX}$ ) are 100 and 300 nm, respectively. The gate oxide thickness is 1 nm. The source and drains are doped uniformly at the concentration of  $5 \times 10^{20} \text{ cm}^{-3}$ . The side surfaces of the fin body profile inside the field oxide are vertical for simplicity of simulation

### 3.1 Effect of Local Doping (LD) Profile in the Fin Body

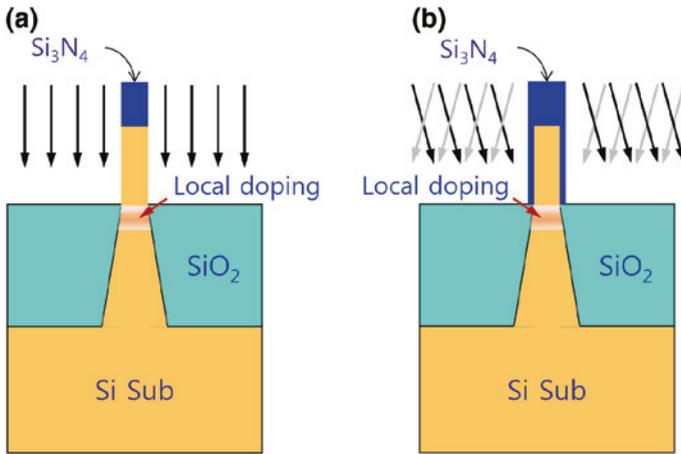
The local doping (LD) of bulk FinFETs is required to suppress unwanted bulk punch-through near the junction depth ( $x_j$ ) of the source and drain regions. In SOI FinFETs, this type of doping is not needed because the buried oxide (BOX) effectively suppresses the punch-through. Figure 4a shows a cross-sectional view cut along the channel length of the bulk FinFET. Local doping is located near the bottom of the source and drain regions, and is called a punch-through stopper (PTS)



**Fig. 4** **a** Cross-sectional view of the bulk FinFET cut along the channel length. The local doping runs laterally near the *bottom* of the source and drain regions. **b** An example of the local doping profile for the punch-through stopper. The peak position was set to 0 nm.  $N_{\text{ldp}}$  stands for peak doping concentration. Here, the fin body doping concentration was fixed at  $1 \times 10^{17} \text{ cm}^{-3}$

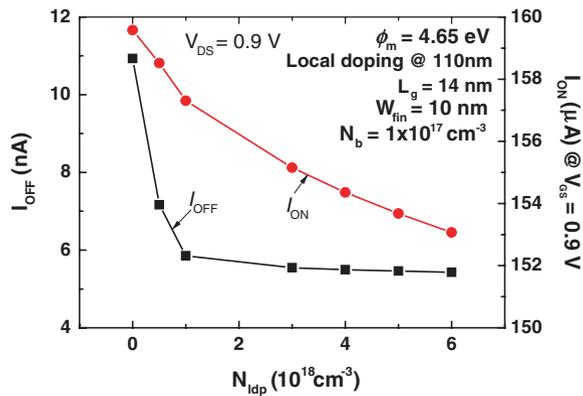
[21, 46]. The peak doping concentration and standard deviation of the local doping represent important parameters. Figure 4b shows an example of a local doping profile, wherein  $N_{\text{ldp}}$  stands for the peak doping concentration of the PTS.

In this chapter, the standard deviation of the doping profile is in the range of  $\sim 8$  nm, because there is a processing method for vertical localization of the doping profile. A new PTS formation technique utilizing lateral doping by straggling ions from the isolation region ( $\text{SiO}_2$ ) was proposed [21]. In this technology, ions for the PTS are implanted into the isolation region at a tilt angle of  $0^\circ$ . The implanted ions are scattered in the isolation region, and some of the ions scattered laterally penetrate into the fin region, resulting in localized doping. In [21], ions were implanted into the isolation region formed on both sides of the vertical fin body and the top hard mask ( $\text{Si}_3\text{N}_4$ ) formed on the fin body. Figure 5a shows a schematic cross-sectional view explaining the implantation into the isolation oxide at a tilt angle of  $0^\circ$  and the fin body profile, which consists of two parts: the vertical fin body where the channel is formed and the tapered fin body wherein the body width is increased as it gets closer to the substrate. In Fig. 5b, the implantation angle is slightly tilted and a hard mask (a layer of nitride,  $\text{Si}_3\text{N}_4$  in this case) is formed on both sides of the fin body protruding from the isolation oxide. Since the nitride layer is more resistant to the penetration of implanted ions than the  $\text{SiO}_2$  layer, the local doping region can be formed effectively using the method shown in Fig. 5b. If doping for the punch-through stopper is distributed vertically in the fin body where the channel is formed, the threshold voltage will be increased, causing clear degradation of the current drivability due to increased impurity scattering. In that case, there would be variation in the threshold voltage due to random doping fluctuation. Thus, it is important that the doping profile be localized vertically to suppress the punch-through.



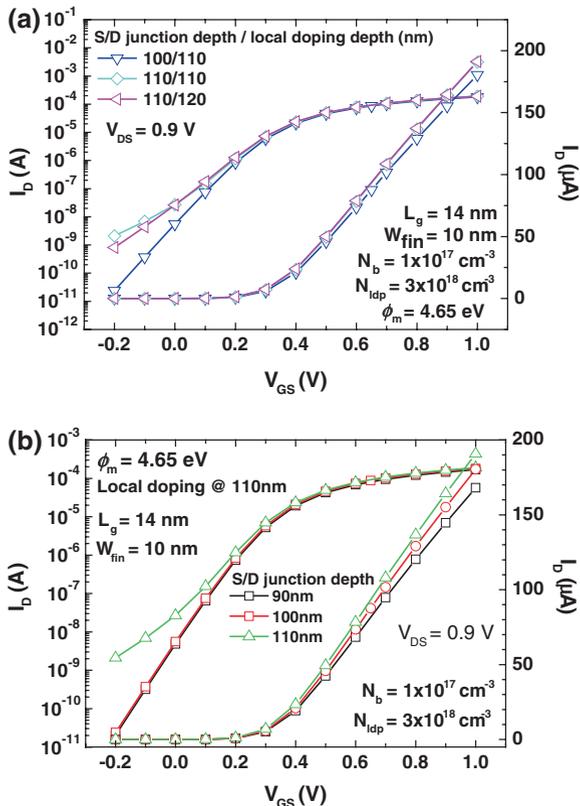
**Fig. 5** Cross-sectional views of the bulk FinFET cut across the channel length. Ion implantations in **a** and **b** were performed with a tilt angle of  $0^\circ$  and a slight tilt, respectively

**Fig. 6** On-current ( $I_{ON}$ ) and off-current ( $I_{OFF}$ ) of 14 nm bulk FinFET with the peak doping concentration of the local doping ( $N_{ldp}$ )



The peak doping concentration ( $N_{ldp}$ ) of the PTS is investigated in terms of the drain current characteristics. Figure 6 shows the  $I_{ON}$  and  $I_{OFF}$  behavior with the  $N_{ldp}$  in the 14 nm FinFET at a fixed fin height ( $H_{fin}$ ) of 100 nm. The gate oxide thickness is 1 nm in the simulated structures. The position of the peak doping concentration is 110 nm, and the source (or drain) junction depth is 100 nm. As can be seen in the figure, when the  $N_{ldp}$  increases from 0 to  $6 \times 10^{18} \text{ cm}^{-3}$ , the  $I_{ON}$  decreases slowly by 4 %. However, the  $I_{OFF}$  demonstrates a significant decrease from 11 to 6 nA with increase of the  $N_{ldp}$  from 0 to  $6 \times 10^{18} \text{ cm}^{-3}$ , after which only slight decrease occurs on further increase of the  $N_{ldp}$ . From the figure,  $N_{ldp}$  values above  $1 \times 10^{18} \text{ cm}^{-3}$  could be considered acceptable. However, if a process margin and the junction capacitance between the source (or drain) to the substrate are considered, the  $N_{ldp}$  of  $2\text{--}3 \times 10^{18} \text{ cm}^{-3}$  is reasonable.

**Fig. 7**  $I_D$ - $V_{GS}$  curves of 14 nm bulk FinFETs at a fixed  $V_{DS}$  of 0.9 V. **a** Examination of position of the peak local doping and  $x_j$  as parameters. **b** Change of the  $x_j$  at a fixed position of peak local doping of 110 nm



The position effect of the peak doping concentration by changing the source and drain junction depth ( $x_j$ ) is now discussed. Figure 7a shows the  $I_D$ - $V_{GS}$  characteristics of 14 nm FinFETs according to the source (or drain) junction depth and the position of the peak local doping concentration (equivalent local doping depth). The drain bias is set to 0.9 V. The  $H_{fin}$ ,  $W_{fin}$ , and  $N_{ldp}$  are 100 nm, 10 nm, and  $3 \times 10^{18}$  cm $^{-3}$ , respectively. In this figure, uniform body doping ( $N_b$ ), which will be examined in the next section, is assumed to be  $1 \times 10^{17}$  cm $^{-3}$ . The work-function of the gate electrode ( $\phi_m$ ) is 4.65 eV. Three different cases show nearly the same  $I_{ON}$ , but with differences of about 4 times in the  $I_{OFF}$  values. Inverse triangle symbols represent a reasonable  $I_D$ - $V_{GS}$  curve of 14 nm FinFETs when the  $x_j$  and position of the peak concentration are 100 and 110 nm, respectively, at a fixed  $H_{fin}$  of 100 nm. If the  $x_j$  is increased to 110 nm at a fixed  $H_{fin}$  of 100 nm, a significant increase in the  $I_{OFF}$  occurs, regardless of the position of the peak local doping concentration, as depicted by the diamond and triangle symbols. The results give the important message that the  $x_j$  should be less than the  $H_{fin}$ , since unwanted cross-talk between the source and drain can be suppressed effectively by the electric field from the gate electrode under such conditions.

**Fig. 8** Subthreshold swing (SS) and drain-induced barrier lowering (DIBL) of 14 nm FinFETs as a parameter of fin body doping concentration. Here,  $V_{DS}$  was 0.9 V. The fin body doping was assumed to be uniform

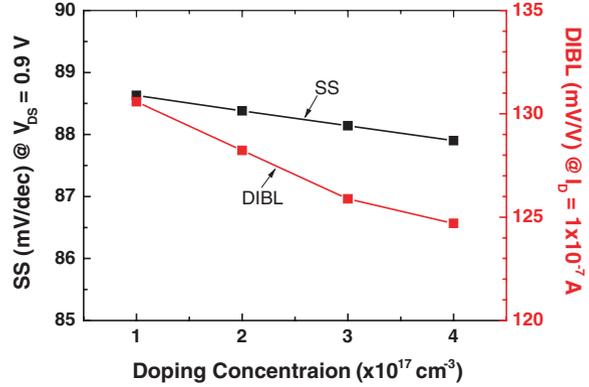


Figure 7b shows similar results to those obtained in Fig. 7a as a function of  $x_j$  at a fixed  $H_{fin}$  of 100 nm. The  $I_D$ - $V_{GS}$  curves of the 14 nm FinFETs with  $x_j$  of less than 100 nm are reasonable since the punch-through is suppressed by the electric field from the gate bias. However, if the  $x_j$  is increased to 110 nm, a significant increase in the  $I_{OFF}$  occurs, as depicted by the triangle symbols. Note that decreasing  $x_j$  causes a slight decrease in the  $I_{ON}$  because the effective channel width is decreased.

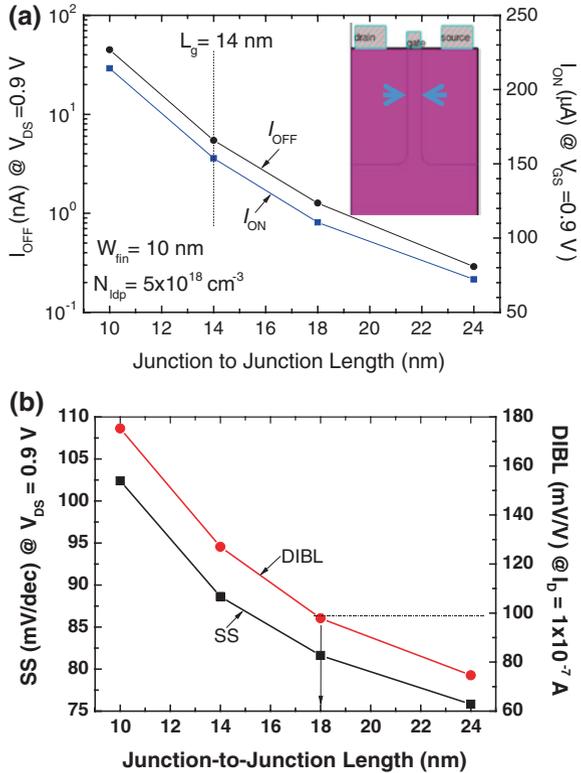
### 3.2 Effect of Fin Body Doping

The doping concentration in the fin body is a key design parameter affecting the subthreshold slope (SS), drain-induced barrier lowering (DIBL), and carrier mobility. In terms of carrier mobility, the body doping should be kept as low as possible. However, decrease in the body doping causes increase in the DIBL and SS, as shown in Fig. 8. In the figure, the body doping is assumed to be uniform. As the body doping is increased from  $1 \times 10^{17}$  to  $4 \times 10^{17} \text{ cm}^{-3}$ , the  $I_{ON}$  decreases by about 5 %, while the  $I_{OFF}$  decreases more significantly (~40 %). Note that the  $V_{th}$  keeps nearly the same values for different concentrations of body doping because it is mainly determined by the work-function of the gate electrode (4.65 eV). When the body doping is increased from  $1 \times 10^{17}$  to  $2 \times 10^{17} \text{ cm}^{-3}$ , a significant decrease of the  $I_{OFF}$  occurs. In Fig. 8, as the body doping increases from  $1 \times 10^{17}$  to  $4 \times 10^{17} \text{ cm}^{-3}$ , the DIBL at an  $I_D$  of  $10^{-7} \text{ A}$  changes within 2.5 %, while the SS at a  $V_{DS}$  of 0.9 V changes by about 2 %. Considering all factors mentioned above, the body doping of  $2\text{--}3 \times 10^{17} \text{ cm}^{-3}$  is reasonable.

### 3.3 Effect of Junction-to-Junction Length

Now, the effect of the length between the source and drain junctions (junction-to-junction length) at a fixed channel length of 14 nm is examined.

**Fig. 9**  $I_{ON}$  and  $I_{OFF}$  behaviors according to the length between the source and drain (a). *SS* and *DIBL* behaviors according to the length (b). The inset in figure (a) represents a cross-sectional view, cut along the channel length. The arrows depicts the length (14 nm)

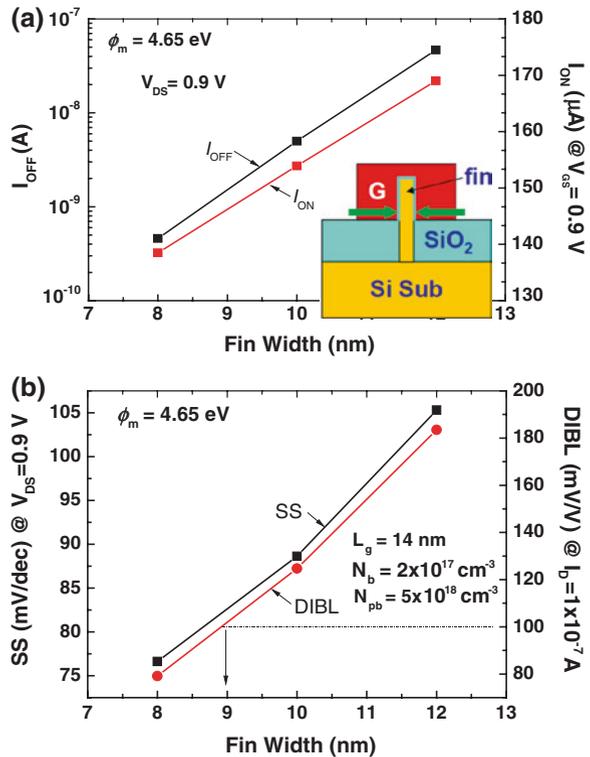


The inset of Fig. 9a illustrates the cross-sectional view cut along the channel length of a bulk FinFET. The arrows were prepared to show the length between the source and drain junctions (junction-to-junction length), which is 14 nm of the example provided. In this figure, the body doping ( $N_b$ ) is  $1 \times 10^{17}$  cm $^{-3}$ . Looking at Fig. 9a, it can be seen that the  $I_{ON}$  and  $I_{OFF}$  decrease significantly with increase in length. Especially high changes in the  $I_{OFF}$  can be observed, by  $\sim 100$  times with change in the length from 10 to 24 nm. If the length is larger than 14 nm, it can be said that the source and drain are underlapped. When the length is 14 nm, the  $I_{ON}$  at the  $V_{GS}$  and  $V_{DS}$  of 0.9 V is  $\sim 728$   $\mu$ A/ $\mu$ m, while the  $I_{OFF}$  at the  $V_{GS}$  of 0 V and  $V_{DS}$  of 0.9 V is 26 nA/ $\mu$ m. Note that only a drift and diffusion model was applied in this simulation. Figure 9b shows the *SS* and *DIBL* characteristics according to the length. As the junction-to-junction length increases, the *SS* and *DIBL* are greatly improved. However, appreciable degradation of the  $I_{ON}$  and  $I_{OFF}$  occurs with increasing length. If the *DIBL* is kept under 100 mV/V, the length needs to be larger than 18 nm when the body doping is  $1 \times 10^{17}$  cm $^{-3}$ . If the reasonable body doping of  $2\text{--}3 \times 10^{17}$  cm $^{-3}$  is considered, the length can be reduced to  $\sim 14$  nm. If there is no mention to the junction-to-junction length in the following sections, the length is 14 nm.

### 3.4 Effect of Fin Body Width

The control of the fin body width ( $W_{\text{fin}}$ ) is very important at a given technology node because the width greatly affects the short channel effect. The fin body width is defined by two arrows in the inset of Fig. 10a. By decreasing the fin body width from 12 to 8 nm, the  $I_{\text{ON}}$  decreases by 18 %, while the  $I_{\text{OFF}}$  decreases by  $\sim 100$  times, as shown in Fig. 10a. Thus, the  $I_{\text{OFF}}$  is very sensitive to the fin body width, which should be controlled accurately to maintain a narrow  $I_{\text{OFF}}$  distribution. Note the total effective channel width ( $2 \times H_{\text{fin}} + W_{\text{fin}}$ ) decreases from 212 to 208 nm as the  $W_{\text{fin}}$  decreases from 12 to 8 nm. The decrease of the total width is just less than 2 % of the  $W_{\text{fin}}$ . The reason for the decrease of  $I_{\text{ON}}$  can mainly be attributed to the decrease of  $V_{\text{th}}$  with decreasing  $W_{\text{fin}}$ . Conversely, the decrease of  $I_{\text{OFF}}$  with decreasing  $W_{\text{fin}}$  can be explained by two reasons: the decrease in  $V_{\text{th}}$  and increase in  $SS$  with decreasing  $W_{\text{fin}}$ . The  $V_{\text{th}}$  defined at an  $I_{\text{D}}$  of  $1 \mu\text{A}/\mu\text{m}$  is decreased by 0.14 V by decreasing the  $W_{\text{fin}}$  from 12 to 8 nm. Figure 10b shows change of the  $SS$  and  $DIBL$  with the  $W_{\text{fin}}$ . As the  $W_{\text{fin}}$  decreases from 12 to 8 nm, the  $SS$  decreases from 106 to 77 mV/dec, while the  $DIBL$  decreases from 183 to 80 mV/V. Therefore,  $W_{\text{fin}}$  also has a significant effect on the  $SS$  and

**Fig. 10**  $I_{\text{ON}}$  and  $I_{\text{OFF}}$  behaviors according to the fin body width (a).  $SS$  and  $DIBL$  behaviors according to the width (b). The inset in figure (a) represents the cross-sectional view cut across the channel length. The arrows indicate the fin body width. The junction-to-junction length in this figure is 14 nm. The fin height and the source/drain junction depth are 100 nm, respectively. The  $I_{\text{ON}}$  was obtained at the  $V_{\text{GS}}$  and  $V_{\text{DS}}$  of 0.9 V, while the  $I_{\text{OFF}}$  was obtained at the  $V_{\text{GS}}$  of 0 V and  $V_{\text{DS}}$  of 0.9 V



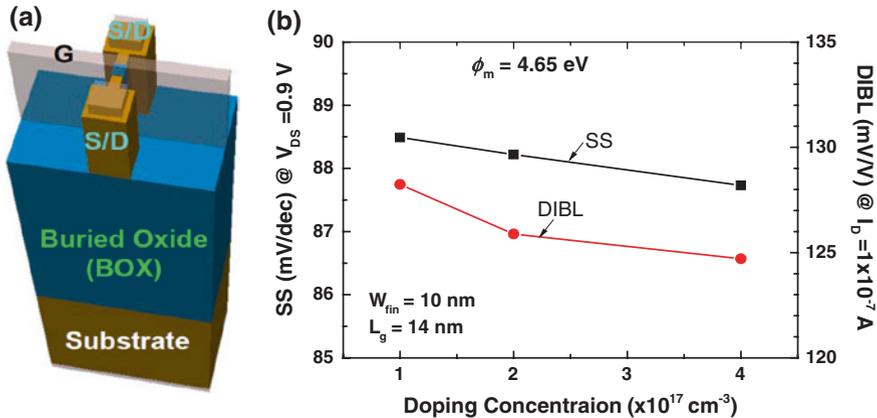
*DIBL*. The  $W_{fin}$  of about 9 nm gives a *DIBL* of 100 mV/V at the given body concentration of  $2 \times 10^{17} \text{ cm}^{-3}$ . If we increase the body doping concentration to  $2.5\text{--}3 \times 10^{17} \text{ cm}^{-3}$ , the *DIBL* decreases, and the  $W_{fin}$  required to give a *DIBL* of 100 mV/V will be about 10 nm.

## 4 Design of 14 nm SOI FinFET

In Sect. 3, we investigated the key design factors of 14 nm bulk FinFETs. Now, we examine the device performance of 14 nm SOI FinFETs and compare the key properties of SOI FinFETs with those of bulk FinFETs.

### 4.1 Effect of Fin Body Doping

In SOI FinFETs, there is no need for the local doping required in bulk FinFETs to suppress punch-through between the source and drain, because it contains buried oxide (*BOX*) located under the fin body where the channel and source/drain are formed. The 3-D schematic view of the 14 nm SOI FinFET is shown in Fig. 11a. The geometry of the device is exactly the same as that of the bulk FinFET shown in Fig. 3, except for the buried oxide. The *BOX* is 300 nm thick. Figure 11b shows the *SS* and *DIBL* of 14 nm SOI FinFETs as a function of fin body doping



**Fig. 11** Three-dimensional schematic view of the 14 nm SOI FinFET (a). Device geometry is exactly the same as that of the 14 nm bulk FinFET shown in Fig. 3. The only difference is the buried oxide (*BOX*) present in the SOI FinFET. The thickness of the *BOX* is 300 nm. *SS* and *DIBL* versus the doping concentration of the fin body (b). The junction-to-junction length in this figure is 14 nm. The fin height and the source/drain junction depth are 100 nm, respectively. The *SS* was obtained at the  $V_{DS}$  of 0.9 V

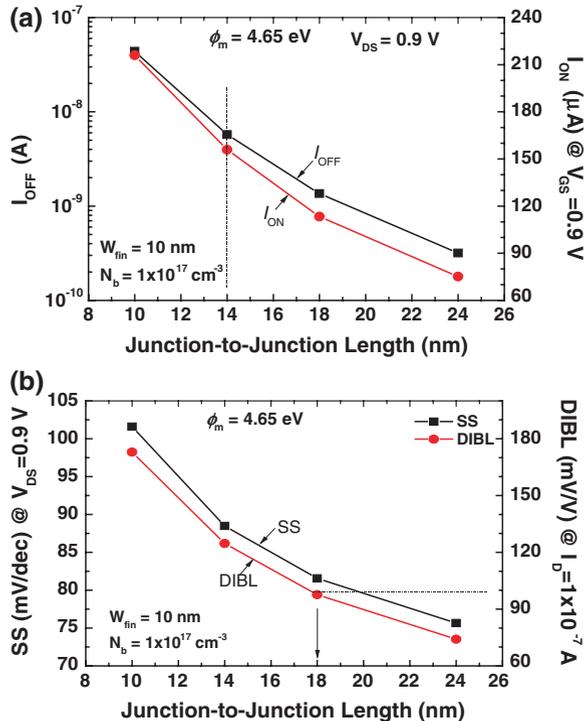
concentration ( $N_b$ ). As the  $N_b$  increases from  $1 \times 10^{17}$  to  $4 \times 10^{17} \text{ cm}^{-3}$ , the  $SS$  decreases from 88.5 to 87.7 mV/dec, while the  $DIBL$  decreases from 128.2 to 124.7 mV/V. These parameters change only slightly with the  $N_b$ , and quite similar to those of the 14 nm bulk FinFET in Fig. 8.

## 4.2 Effect of Junction-to-Junction Length

The effect of junction-to-junction length on the device performance of 14 nm SOI FinFETs is investigated in Fig. 12.

In Fig. 12, the body doping ( $N_b$ ) is  $1 \times 10^{17} \text{ cm}^{-3}$ . With examination of Fig. 12a, it can be seen that  $I_{ON}$  and  $I_{OFF}$  decrease significantly with increase in the length. Especially high changes in the  $I_{OFF}$  can be observed, by  $\sim 100$  times with change in the length from 10 to 24 nm. At length of 14 nm, the  $I_{ON}$  at the  $V_{GS}$  and  $V_{DS}$  of 0.9 V is  $\sim 730 \mu\text{A}/\mu\text{m}$ , while the  $I_{OFF}$  at the  $V_{GS}$  of 0 V and  $V_{DS}$  of 0.9 V is 26 nA/ $\mu\text{m}$ . Note that only a drift and diffusion model was applied in this simulation. The  $I_{ON}$  and  $I_{OFF}$  of the SOI FinFET are quite similar to those of the bulk FinFET shown in Fig. 9a. Figure 12b shows the  $SS$  and  $DIBL$  characteristics of the 14 nm SOI FinFET according to the length. As the junction-to-junction

**Fig. 12**  $I_{ON}$  and  $I_{OFF}$  behaviors according to the length between the source and drain (a).  $SS$  and  $DIBL$  behaviors according to the length (b). The  $I_{ON}$  was obtained at the  $V_{GS}$  and  $V_{DS}$  of 0.9 V, while the  $I_{OFF}$  was obtained at the  $V_{GS}$  of 0 V and  $V_{DS}$  of 0.9 V. The fin height and the source/drain junction depth are 100 nm, respectively. The  $SS$  was obtained at the  $V_{DS}$  of 0.9 V

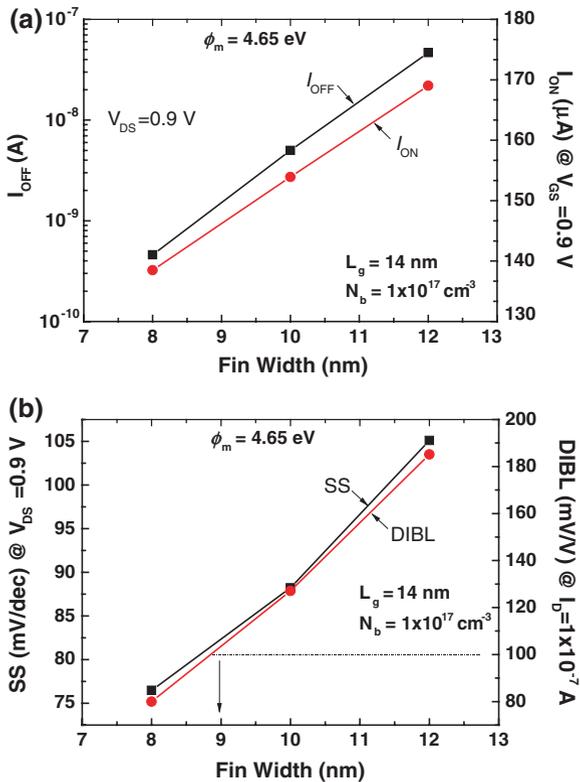


length increases, the *SS* and *DIBL* are greatly improved. However, appreciable degradation of the  $I_{ON}$  and  $I_{OFF}$  occurs with increase in the length. If a *DIBL* of below 100 mV/V is maintained, the length needs to be larger than 18 nm when the body doping is  $1 \times 10^{17} \text{ cm}^{-3}$ . If the reasonable body doping of  $2\text{--}3 \times 10^{17} \text{ cm}^{-3}$  is considered, the length can be reduced to  $\sim 14 \text{ nm}$ . Thus, the 14 nm SOI FinFET shows nearly the same performance as that of the 14 nm bulk FinFET.

### 4.3 Effect of Fin Body Width

As in the case of the bulk FinFET, the effect of fine body width is studied in the 14 nm SOI FinFET in this section. By decreasing the fin body width from 12 to 8 nm, the  $I_{ON}$  decreases by 18 % while the  $I_{OFF}$  decreases by  $\sim 100$  times, as shown in Fig. 13a. Since the  $I_{OFF}$  is highly sensitive to the fin body width, the width should be controlled accurately to maintain a narrow  $I_{OFF}$  distribution. As mentioned in Sect. 3.4, the decrease of the total effective channel width is less than 2 % of the  $W_{fin}$ . The decrease in the  $I_{ON}$  can mainly be attributed to the decrease in  $V_{th}$  with decreasing  $W_{fin}$ . Conversely, the decrease in  $I_{OFF}$  with

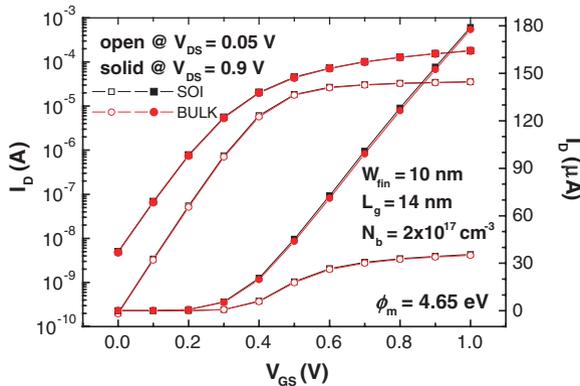
**Fig. 13**  $I_{ON}$  and  $I_{OFF}$  behaviors according to the fin body width (a). *SS* and *DIBL* behaviors according to the width (b). The inset in figure a represents the cross sectional view cut across the channel length. The arrows indicate the fin width. The junction-to-junction length in this figure is 14 nm. The fin height and the source/drain junction depth are 100 nm, respectively. The  $I_{ON}$  was obtained at the  $V_{GS}$  and  $V_{DS}$  of 0.9 V, while the  $I_{OFF}$  was obtained at the  $V_{GS}$  of 0 V and  $V_{DS}$  of 0.9 V



decreasing  $W_{\text{fin}}$  can be explained by the accompanying decrease in  $V_{\text{th}}$  and increase in  $SS$ . The  $V_{\text{th}}$  defined at an  $I_{\text{D}}$  of  $1 \mu\text{A}/\mu\text{m}$  is decreased by  $0.14 \text{ V}$  with a decrease in  $W_{\text{fin}}$  from  $12$  to  $8 \text{ nm}$ . Figure 13b shows the  $SS$  and  $DIBL$  according to the  $W_{\text{fin}}$ . As the  $W_{\text{fin}}$  lowers from  $12 \text{ nm}$  to  $8 \text{ nm}$ , the  $SS$  decreases from  $106$  to  $77 \text{ mV/dec}$ , while the  $DIBL$  decreases from  $183$  to  $80 \text{ mV/V}$ . Therefore,  $W_{\text{fin}}$  also has a significant effect on the  $SS$  and  $DIBL$ . The  $W_{\text{fin}}$  which gives a  $DIBL$  of  $100 \text{ mV/V}$  is about  $9 \text{ nm}$  at a given body concentration of  $1 \times 10^{17} \text{ cm}^{-3}$ . If we increase the body doping concentration to  $2.5\text{--}3 \times 10^{17} \text{ cm}^{-3}$ , the  $DIBL$  decreases, and the  $W_{\text{fin}}$  of about  $10 \text{ nm}$  is required to provide a  $DIBL$  of  $100 \text{ mV/V}$ . All analyses done for the bulk FinFET are exactly the same as those for the SOI FinFET.

#### 4.4 Comparison of $I_{\text{D}}\text{--}V_{\text{GS}}$ of Bulk and SOI FinFETs

In this section, we compare the  $I_{\text{D}}\text{--}V_{\text{GS}}$  curves of  $14 \text{ nm}$  bulk and SOI FinFETs. As mentioned above, they have exactly the same geometry, except that the bulk FinFET has local doping located under the source/drain junction depth, whereas the SOI FinFET contains buried oxide at that location instead of local doping. The fin height and width are  $100$  and  $10 \text{ nm}$ , respectively. The fin body concentration is uniformly doped with a concentration of  $2 \times 10^{17} \text{ cm}^{-3}$ . As shown in Fig. 14, bulk and SOI FETs have exactly the same  $I\text{--}V$  characteristics, as depicted by circle and square symbols, respectively.



**Fig. 14**  $I_{\text{D}}\text{--}V_{\text{GS}}$  curves of  $14 \text{ nm}$  bulk (circle) and SOI (square) FinFETs. The junction-to-junction length in this figure is  $14 \text{ nm}$ . The fin height and source/drain junction depth are  $100 \text{ nm}$ , respectively. Solid and open symbols represent the curves for the  $V_{\text{DS}}$  values of  $0.9$  and  $0.05 \text{ V}$ , respectively. The fin body is uniformly doped with a concentration of  $2 \times 10^{17} \text{ cm}^{-3}$ . Gate oxide thickness is  $1 \text{ nm}$

## 5 Parasitic Resistance and Capacitance in Bulk FinFETs

In this section, the parasitic resistance and capacitance of bulk FinFETs are discussed. The resistance is related to the contact resistivity between the source/drain region and the metal, as well as the contact area between them. The resistance in the source/drain regions has significant effects on the  $I_{ON}$  and speed characteristic. The capacitance is studied in terms of the junction and gate capacitance. The junction capacitance is formed between the source/drain regions to the substrate in the fin body. Since the speed of the device depends on the capacitance, examination of the capacitance is needed.

### 5.1 Effect of S/D Contact Resistance

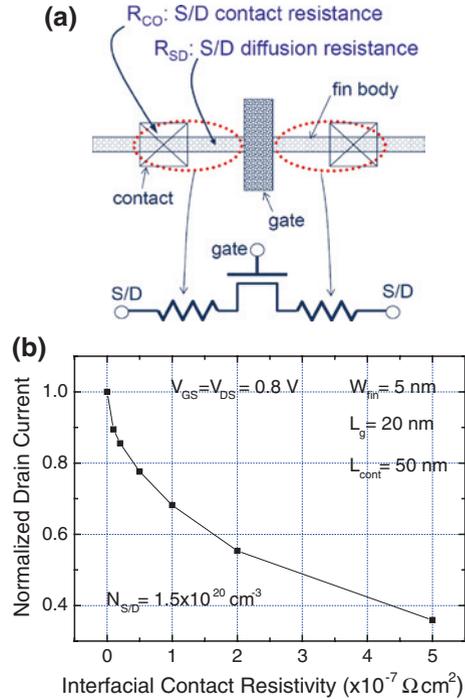
As mentioned in Sect. 4, the width of the fin body in 14 nm FinFETs is about 10 nm. The source/drain and channel are formed in the fin body. The source/drain regions formed in the thin fin body are particularly likely to have high resistance due to diffusion resistance ( $R_{SD}$ ) and contact resistance ( $R_{CO}$ ).

Before starting the discussion on contact area and structure, the effects of the interfacial contact resistivity ( $\rho_c$ ) on the drain current of the FinFET will be examined. Figure 15a shows a schematic top view of a FinFET, wherein the contact resistance and diffusion resistance of the source/drain are depicted. Such parasitic resistance is reflected in the equivalent circuit of a MOSFET, and causes degradation of the drain current and transconductance ( $g_m$ ). Figure 15b shows the normalized drain current of a 20 nm FinFET at the given  $V_{GS}$  and  $V_{DS}$  of 0.8 V. Since the FinFET has a fin body width of 5 nm and contact length ( $l_c$ ) of 50 nm, the contact area between the source/drain region and the metal electrode becomes  $5 \times 20 \text{ nm}^2$ . If the sheet resistivity of the diffusion resistance ( $\rho_{sd}$ ) is too small to meet  $l_c \ll \sqrt{(\rho_c/\rho_{sd})}$ , the contact resistance ( $R_{CO}$ ) is given by  $\rho_c/(W_{fin} \cdot l_c)$ . The drain current is normalized to the drain current occurring when the  $\rho_c$  is  $0 \text{ } \Omega \text{ cm}^2$ . As  $\rho_c$  increases from  $0 \text{ } \Omega \text{ cm}^2$  to  $1 \times 10^{-7} \text{ } \Omega \text{ cm}^2$ , the drain current decreases by ~30 %, which means that  $\rho_c$  must be kept as low as possible in highly scaled MOSFETs.

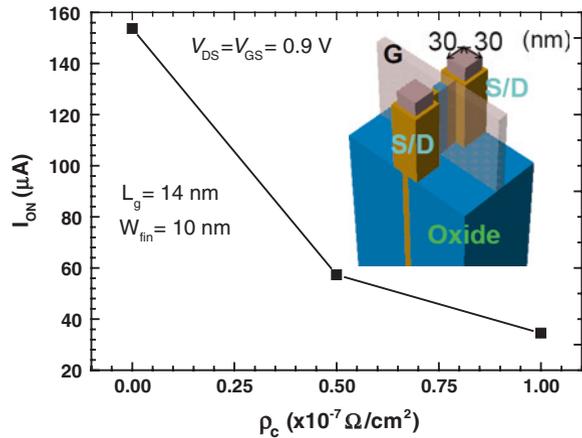
Next, the drain current of a 14 nm bulk FinFET is investigated, according to  $\rho_c$ . The inset of Fig. 16 represents the 3-D structure of the 14 nm FinFET for 3-D device simulation. The fin body width ( $W_{fin}$ ) is 10 nm, and the fin height ( $H_{fin}$ ) is 100 nm. The source and drain regions on both ends of the fin body have a wide width (40 nm), which can be used to effectively reduce the source and drain parasitic resistance. The length of the wide source/drain regions is 40 nm, making the area of the top region  $40 \times 40 \text{ nm}^2$ . In this inset, the area of the metal electrodes formed on the top surface of the source/drain regions is  $30 \times 30 \text{ nm}^2$ .

Figure 16 shows the  $I_{ON}$  behavior of a 14 nm FinFET at the  $V_{GS}$  and  $V_{DS}$  of 0.9 V with variation of  $\rho_c$  from 0 to  $1 \times 10^{-7} \text{ } \Omega \text{ cm}^2$ . Decrease of the  $I_{ON}$  from

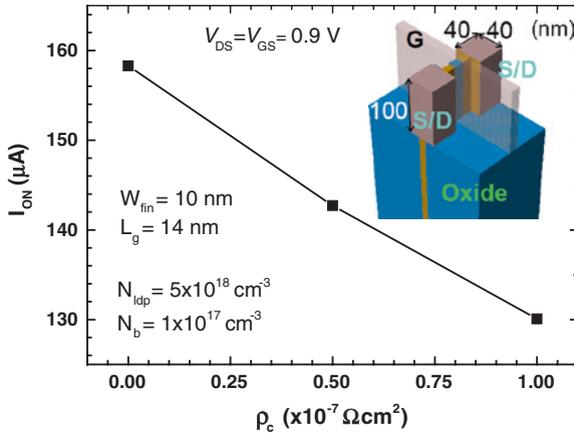
**Fig. 15** Schematic *top view* of a FinFET and equivalent circuit including parasitic source and drain resistances (a). Normalized drain current of a 20 nm bulk FinFET versus the interfacial contact resistivity between the source/drain region and the metal electrode (b). Here, the fin body width ( $W_{fin}$ ) is 5 nm and the contact length ( $l_c$ ) is 50 nm. The source and drain regions are doped uniformly with a concentration of  $1.5 \times 10^{20} \text{ cm}^{-3}$



**Fig. 16**  $I_{ON}$  behavior of 14 nm bulk FinFETs versus interfacial contact resistivity. The *inset* shows the 3-D view of a FinFET. The source and drain regions to provide the contact pad have a height of 100 nm and an area of  $40 \times 40 \text{ nm}^2$ . Here, the fin body width ( $W_{fin}$ ) is 10 nm, and the metal contact area on the pad is  $30 \times 30 \text{ nm}^2$



153.7 to 34.5  $\mu\text{A}$  occurs as  $\rho_c$  increases from 0 to  $1 \times 10^{-7} \Omega \text{ cm}^2$ . The reduction of the current with the increase of  $\rho_c$  is remarkable (77.6 % decrease). It should be noted that  $\rho_c$  of  $1 \times 10^{-7} \Omega \text{ cm}^2$  is popular in the industry. Thus, it is imperative to develop new materials and/or process methods to decrease the interfacial contact resistivity. Are there any methods to reduce the contact resistivity other than

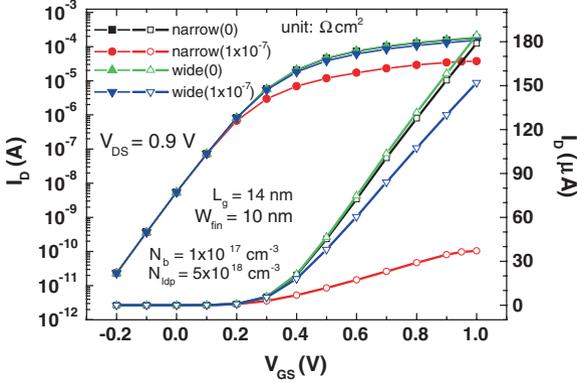


**Fig. 17**  $I_{ON}$  behavior of 14 nm bulk FinFETs versus interfacial contact resistivity ( $\rho_c$ ). The inset shows the 3-D view of a FinFET. The source and drain regions for provision of the contact pad have a height of 100 nm and an area of  $40 \times 40 \text{ nm}^2$ . Here, the fin body width ( $W_{fin}$ ) is 10 nm and the metal contact area on the source or drain is  $13,600 \text{ nm}^2$  ( $3 \times 40 \times 100 \text{ nm}^2 + 40 \times 40 \text{ nm}^2$ )

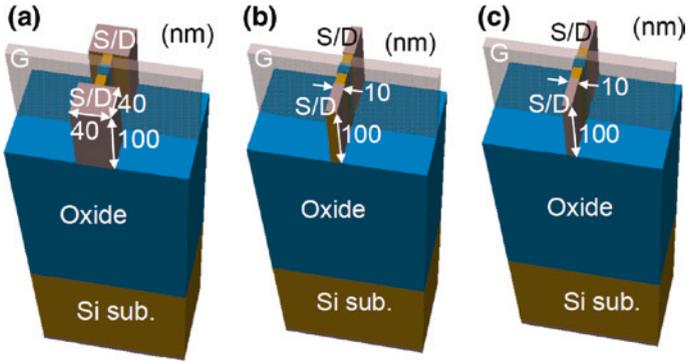
developing new materials and/or process methods? Increasing the contact area between the metal electrode and the source/drain may provide the answer to this question.

Figure 17 shows the  $I_{ON}$  behavior according to the  $\rho_c$  for a 14 nm bulk FinFET with a wide contact area ( $3 \times 40 \times 100 \text{ nm}^2 + 40 \times 40 \text{ nm}^2 = 13,600 \text{ nm}^2$ ) between the metal electrode and the source (or drain). The FinFETs in Figs. 16 and 17 have the same doping and geometry, but the contact area in Fig. 17 is about 15 times wider than that examined in Fig. 16. The inset in Fig. 17 clearly illustrates the metal electrode, which covers the surfaces of three sides and the top of the wide source (or drain) region. As  $\rho_c$  increases from 0 to  $1 \times 10^{-7} \Omega \text{ cm}^2$ , the  $I_{ON}$  decreases from 158 to 130  $\mu\text{A}$  (about an 18 % decrease). In an effort to increase the contact area, deposit of *Ni* on epitaxially grown source and drain regions via atomic layer deposition (ALD) was reported, after which nickel silicide (*NiSi*) was formed to provide a wide contact area [53]. In Fig. 18, the  $I_D$ - $V_{GS}$  curves of 14 nm bulk FinFETs are compared in terms of the contact area between the metal electrode and the source/drain regions. The FinFETs with narrow ( $90 \text{ nm}^2$ ) and wide ( $13,600 \text{ nm}^2$ ) contact areas examined are exactly the same as those in Figs. 16 and 17, respectively. When the contact resistivity is  $0 \Omega \text{ cm}^2$ , the  $I_{ON}$  is nearly the same, regardless of the contact area. However, a significant reduction in the  $I_{ON}$  occurs when the contact resistivity is  $1 \times 10^{-7} \Omega \text{ cm}^2$ . From these results, the importance of keeping the contact area between the metal electrode and the source (or drain) region as wide as possible can be understood, in addition to lowering the interfacial contact resistivity.

Now, let us systematically examine the effect of the contact area and structure. Figure 19 shows 3-D structures of 14 nm SOI FinFETs with exactly the same



**Fig. 18**  $I_D$ - $V_{GS}$  curves of 14 nm bulk FinFETs with different contact areas between the metal electrode and the source (or drain) as a parameter of the interfacial contact resistivity ( $\rho_c$ ). The wide and narrow contact areas are 90 and 13,600  $\text{nm}^2$ , respectively



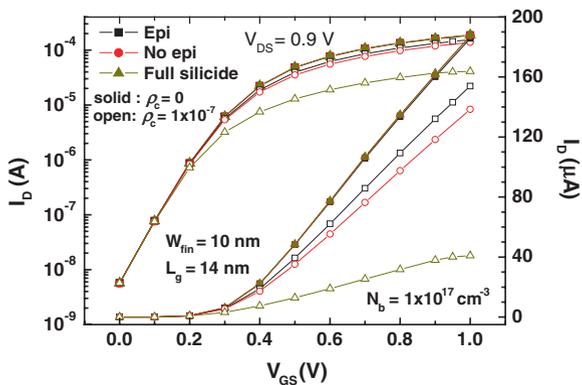
**Fig. 19** 3-D structures of 14 nm bulk FinFETs with different contact areas and structures. Figure **a** shows the wide metal contact formed on epitaxially grown source and drain regions. The contact area in figure **a** is 13,600  $\text{nm}^2$  ( $= 3 \times 40 \times 100 \text{ nm}^2 + 40 \times 40 \text{ nm}^2$ ). The wide metal contact of 9,400  $\text{nm}^2$  ( $= 10 \times 40 \text{ nm}^2 + 10 \times 100 \text{ nm}^2 + 2 \times 40 \times 100 \text{ nm}^2$ ) is formed on the source and drain regions without an epitaxial layer (**b**). In figure **c**, the source/drain regions have no epitaxial layer, and fully-silicided source and drain regions are formed 15 nm away from the gate electrode. Therefore, the contact area between the metal and the source (or drain) is 400  $\text{nm}^2$  ( $10 \times 40 \text{ nm}^2$ )

doping and device geometry, except for the source and drain regions. As mentioned in Fig. 14, both SOI and bulk FinFETs have nearly the same characteristics. Consequently, it is acceptable to consider the SOI FinFETs as bulk FinFETs when investigating the  $I_{ON}$  with the metal contact area and the source/drain

structure. Figure 19a has the same metal contact area and source/drain structure as that presented in the inset of Fig. 17. The epitaxial layer is formed on the fin source/drain regions at a width of 10 nm. The source/drain regions have a width of 10 nm from the edge of the gate electrode until 15 nm away from the gate, and a width of 40 nm from 15 nm away from the gate to 55 nm away, along the fins. The metal electrode for the contact of the source/drain region is assumed to cover the top and side surfaces of the wide source/drain region. Therefore, the contact area is  $13,600 \text{ nm}^2 (= 40 \times 40 \text{ nm}^2 + 3 \times 100 \times 40 \text{ nm}^2)$ . In Fig. 19b, the source/drain structure has no epitaxial layer, and the metal contact area is  $9,400 \text{ nm}^2 (= 10 \times 40 \text{ nm}^2 + 10 \times 100 \text{ nm}^2 + 2 \times 100 \times 40 \text{ nm}^2)$ . The source and drain regions in Fig. 19c have no epitaxial layer, and the source and drain regions 15 nm away from the gate are fully silicided. As a result, the contact area between the silicided region and the remaining source (or drain) region becomes  $1,000 \text{ nm}^2 (= 10 \times 100 \text{ nm}^2)$ .

Figure 20 shows the  $I_D-V_{GS}$  curves of the 14 nm FinFETs illustrated in Fig. 19 as a parameter of the interfacial contact resistivity. The curves represented by squares, circles, and triangles correspond to the data of the source/drain structures of Fig. 19a–c, respectively. The  $I_D-V_{GS}$  curves among the three different arrangements of FinFETs are quite similar when the interfacial contact resistivity is  $0 \text{ } \Omega \text{ cm}^2$ . However, appreciable difference according to the contact structures can be seen at the contact resistivity of  $1 \times 10^{-7} \text{ } \Omega \text{ cm}^2$ . The FinFET with the epitaxial layer and wide contact area shows the largest  $I_{ON}$  among the three devices, depicted by square symbols. The device with no epitaxial layer and a wide contact area displays 10 % degradation of the  $I_{ON}$  compared to that with an epitaxial layer and a wide contact area. In contrast, 71 % degradation of the  $I_{ON}$  can be observed for the FinFET with the fully silicided source/drain region. These data emphasize the importance of having a wide contact area between the metal and source/drain regions.

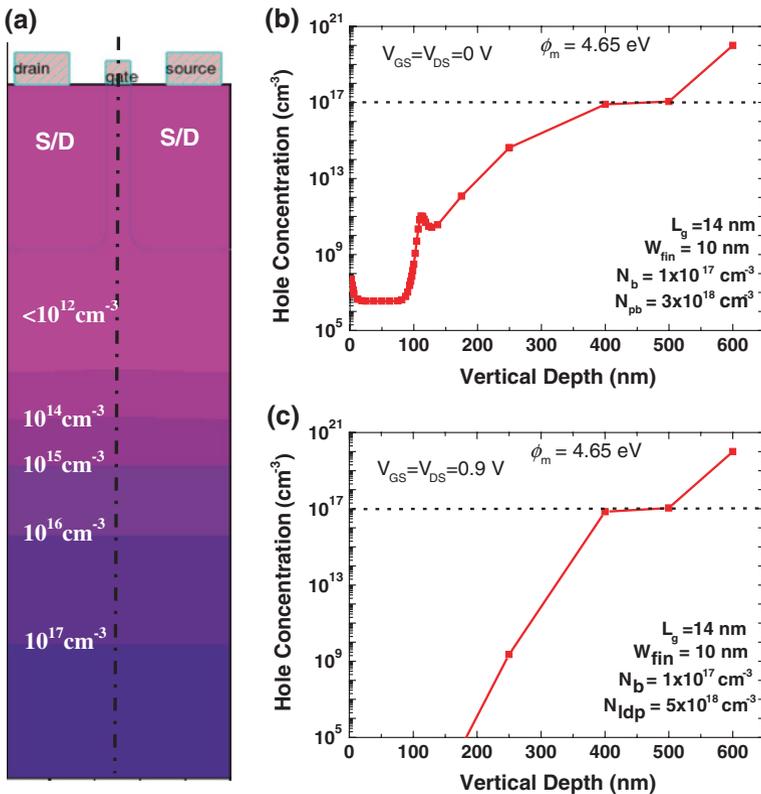
**Fig. 20**  $I_D-V_{GS}$  curves of 14 nm bulk FinFETs with different contact areas and structures as a parameter of the interfacial contact resistivity ( $\rho_c$ ). The curves corresponding to *square*, *circle*, and *triangle* symbols represent the data for the structures shown in Fig. 19a–c, respectively



### 5.2 Junction and Gate Capacitances of Bulk FinFETs

In addition to parasitic resistance, the parasitic capacitance is also important in determining the speed characteristic and power consumption. In this section, investigation of the source/drain to substrate and gate oxide capacitances is carried out.

Figure 21a shows a cross-sectional view cut along the channel length, wherein the contour of the hole concentration in the fin body at the  $V_{GS}$  and  $V_{DS}$  of 0 V is depicted. In this simulation, the source and drain regions are doped uniformly with a doping concentration of  $5 \times 10^{20} \text{ cm}^{-3}$ , and the fin body has the uniform doping of  $1 \times 10^{17} \text{ cm}^{-3}$ . It should be noted that the punch-through stopper (PTS) is

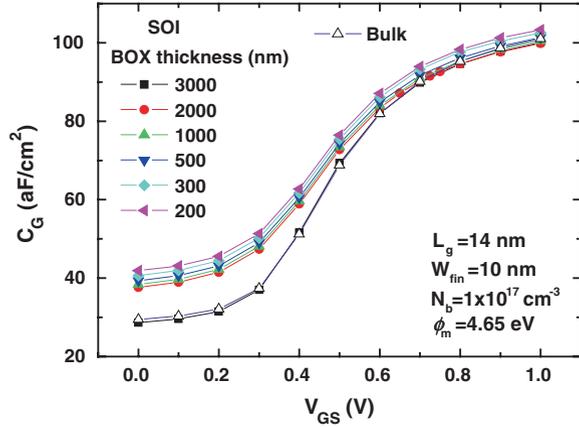


**Fig. 21** Cross-sectional view of a fin body, cut along the channel length (a). The source/drain junction depth is 100 nm from the top of the fin body. Hole concentration profile, cut along the dashed-dotted line in figure (a), when both the  $V_{GS}$  and  $V_{DS}$  are 0 V (b) and 0.9 V (c), respectively. The fin body is uniformly doped with a concentration of  $1 \times 10^{17} \text{ cm}^{-3}$ . The peak concentration of the local doping is  $5 \times 10^{18} \text{ cm}^{-3}$

located at 110 nm, with a peak p-type doping concentration of  $5 \times 10^{18} \text{ cm}^{-3}$  and a standard deviation of 8 nm, for suppression of the punch-through between the drain and source. In this n-type FinFET, the fin body and PTS are doped with the same p-type impurity, resulting in increase of the impurity concentration of the fin body. In this situation, the junction capacitance between the source (or drain) and the substrate formed within the fin body is now discussed. One method to determine the depletion width at the junction is to check the hole concentration profile of the fin body. An example hole contour at equilibrium is shown in Fig. 21a. For quantitative evaluation of the hole profile, the hole concentration along the dash-dot line in Fig. 21a was extracted and prepared in Fig. 21b, c, where the profiles were obtained at equilibrium ( $V_{GS} = V_{DS} = 0 \text{ V}$ ) and given  $V_{GS} = V_{DS} = 0.9 \text{ V}$ , respectively. In both figures (b) and (c), the region from 0 to 100 nm is the channel wherein the fin body is fully depleted. In Fig. 21b, the channel region has a hole concentration of less than  $\sim 10^8 \text{ cm}^{-3}$  because of the work-function difference between the gate and body at equilibrium. The peak hole concentration is found near 110 nm due to the locally enhanced p-type doping for the PTS. Near 400 nm, the hole concentration becomes the doping level of the body ( $1 \times 10^{17} \text{ cm}^{-3}$ ). In Fig. 21c, the fin body at a position less than 400 nm is fully depleted, and much lower hole concentration compared to that in Fig. 21b is observed, due to the given  $V_{GS}$  and  $V_{DS}$ . Note that the height of the total fin body protruding from the substrate is 400 nm in this simulation. Then, the depletion width under the source/drain regions becomes about 300 nm, which is equivalent to oxide with a thickness of 100 nm, considering the dielectric constant of Si and  $\text{SiO}_2$ . The junction capacitance of the bulk FinFET in Fig. 21 is similar to that of the SOI FinFET when 100-nm thick buried oxide is used. As mentioned in Sect. 6.2, the thickness of the buried oxide needs to be thinned down to  $\sim 20 \text{ nm}$  to allow effective transfer of the heat generated in the channel to the substrate. From this point of view, the bulk FinFET can have smaller junction capacitance than the SOI FinFET, although SOI devices traditionally have the merit of low junction capacitance due to the thick buried oxide.

Figure 22 shows the simulated  $C_G$ - $V_{GS}$  curves of 14 nm SOI FinFETs as a parameter of the buried oxide (BOX) thickness. As a reference, the  $C_G$ - $V_{GS}$  curve of the 14 nm bulk FinFET is also depicted in open triangle symbols. Here, the source, drain, and substrate are grounded. The area of the gate electrode butted to the isolation oxide is  $2,660 \text{ nm}^2$  ( $14 \times 190 \text{ nm}^2$ ). The channel area covered by the gate is  $2,940 \text{ nm}^2$  ( $2 \times 14 \times 100 \text{ nm}^2 + 14 \times 10 \text{ nm}^2$ ). As can be seen in the figure, decreasing BOX thickness increases the capacitance between the gate and the substrate. The gate oxide thickness is fixed at 1 nm. The SOI FinFET with a BOX thickness of 300 nm displays a quite similar  $C_G$ - $V_{GS}$  curve to that of the bulk FinFET. As the BOX thickness decreases, the  $C_G$  increases at all gate biases. The  $C_G$  difference in the inversion region is quite small, but it becomes more appreciable in the depletion region due to a significant reduction in the gate oxide capacitance.

**Fig. 22** Simulated gate capacitance ( $C_G$ ) versus gate bias in 14 nm SOI FinFETs as a parameter of buried oxide (BOX) thickness. As a reference, the  $C_G$ - $V_{GS}$  of the 14 nm bulk FinFET is also depicted by *open triangle* symbols

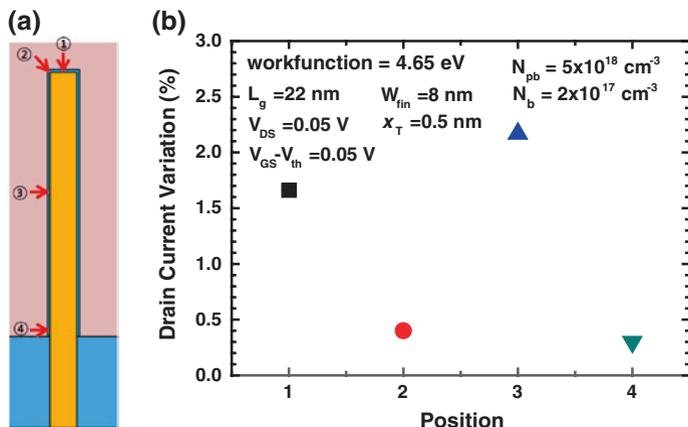


## 6 Current Fluctuation with Charge Trap and Temperature

In analog integrated circuit (IC) applications, drain current fluctuation with the trapping/detrapping of channel charges significantly affects the signal-to-noise ratio. The temperature in channels under operation can increase significantly. This results in changes in the key device parameters, including threshold voltage, mobility, and leakage, which causes problems in the ICs. In this section, we will study the fluctuation of drain current and temperature in the channel.

### 6.1 Drain Current Fluctuation with Single Charge Trap

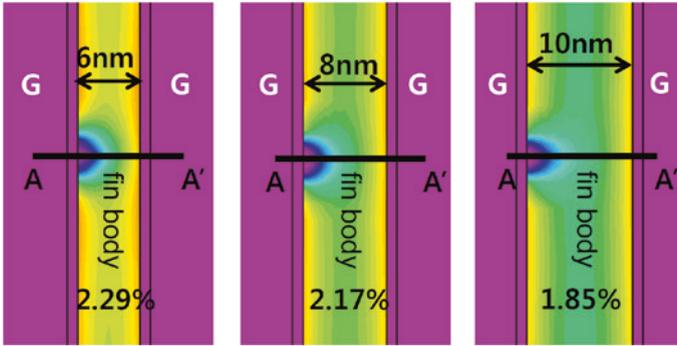
The carriers in the channel can become trapped inside the gate oxide and detrapped into the channel randomly, leading to random fluctuation of the drain current. This kind of fluctuation adversely affects the amplification of very small signals. In this section, we examine how much drain current fluctuation occurs due to random trapping and detrapping of a carrier. Since the trap position along the channel width can cause different fluctuations in the drain current of bulk FinFETs, the effect of trap position should be determined. The position effect has partially been reported in SOI FinFETs [54]. Figure 23a shows a cross-sectional view across the fin body, wherein numbers 1, 2, 3, and 4 identify the trap position along the channel width. In this study, the channel length of the bulk FinFET is set to 22 nm because the current fluctuation in the bulk FinFETs is compared to that of the 22 nm planar MSOFET. Here, the fin body width is 8 nm and the gate oxide thickness is 1 nm. Positions 1, 2, 3, and 4 represent the trap position of the top center, top corner, and the center and bottom of the side, respectively. These traps are assumed to be located in the middle of the channel length. The trap depth ( $x_T$ ), which is the distance from the interface between the gate oxide and the fin body to a position inside the gate oxide, is fixed at 0.5 nm.



**Fig. 23** Cross-sectional view of the fin body, cut across the channel length. The numbers in circles along the channel width of the FinFET represent the trap positions examined. The positions are assumed to be located in the *middle* of the channel between the source and the drain. Numbers 1 and 2 represent the positions of the *top center* and *top corner* traps, respectively. Numbers 3 and 4 represent the positions of the trap on the *center* and *bottom* of the side, respectively. The trap depth ( $x_T$ ), which is defined as the distance from the interface between the gate oxide and the fin body for the channel, is fixed at 0.5 nm. Drain current variation according to trap position in the 22 nm bulk FinFET (b). The drain current fluctuation was obtained at the  $V_{GS} - V_{th}$  of 0.05 V

In Fig. 23b, the drain current variation according to trap position is shown at the  $V_{GS} - V_{th}$  of 0.05 V and the  $V_{DS}$  of 0.05 V. Trap position 3 gives the largest current fluctuation, because trapping of an electron in position 3 appreciably decreases the channel electron density near the trap, while partly decreasing the electron density on the opposite side (right side) of the channel. Accordingly, it seems that a trap located inside the gate oxide on one of the facing channels will result in larger effects to the other channel when the fin width is thinner. This phenomenon cannot be observed in planar channel MOSFETs. It should be noted that the threshold voltage of the bulk FinFET is mainly determined by the workfunction difference between the gate and the fin body, not by the channel doping ( $1 - 3 \times 10^{17} \text{ cm}^{-3}$ ). Therefore, the current density along the channel width is uniform; no current crowding region is present in the channel.

Next, the dependence of drain current fluctuation on the fin body width is examined. Figure 24 shows the contours of the channel electron density on part of the cross-sectional views for three fin widths. Here, ‘G’ indicates the gate electrode. The fin widths, from left to right, are 6, 8, and 10 nm, respectively. It is assumed that a trap is located at the depth of 0.5 nm from the interface between the gate oxide and the fin body on the left side. Through this examination, it can be seen that the electron density in the channel on the right side can be affected more appreciably for thinner fin body width. For the given fin height of 100 nm and the channel length of 22 nm, the drain current variations for the fin body widths of 6, 8, and 10 nm are 2.29, 2.17, and 1.85 %, respectively. This

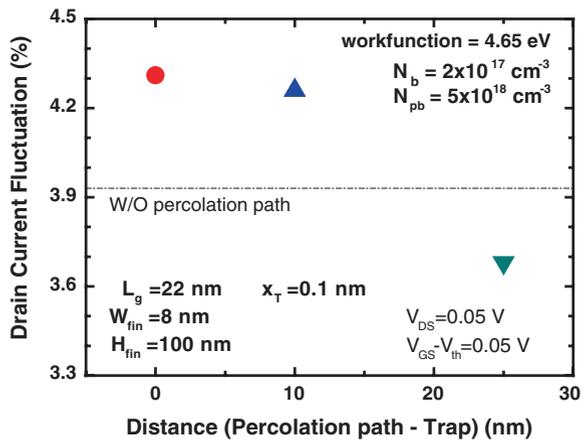


**Fig. 24** Contours of electron density on the cross-sectional views cut across the fin body at the  $V_{GS}-V_{th}$  of 0.05 V and  $V_{DS}$  of 0.05 V. The fin body widths, from *left to right*, are 6, 8, and 10 nm, respectively. The trap depth ( $x_T$ ) is 0.5 nm

demonstrates that thinner fin body gives rise to higher variation of the drain current. If the fin height is reduced, the variation will be increased.

In fabricated FinFETs, there may be a sort of percolation path which comes from random dopant fluctuation (RDF) [55] and/or work-function variation of the gate electrode [56]. Since the threshold voltage ( $V_{th}$ ) of bulk FinFETs is mainly determined by the work-function difference between the gate electrode and the fin body, a percolation path cannot be generated by random dopant fluctuation. Planar channel MOSFETs can have percolation paths generated by the RDF and work-function difference. If the trap position mentioned above is aligned to the percolation path, an increase in the drain current variation can be expected. Figure 25 shows the percentage of drain current variation as a function of the distance between the percolation path and trap. Here, the trap depth ( $x_T$ ) is 0.1 nm. When the distance between the percolation path and the trap is 0 nm (perfectly aligned), the variation is the largest, as expected. Note that the effective size of the

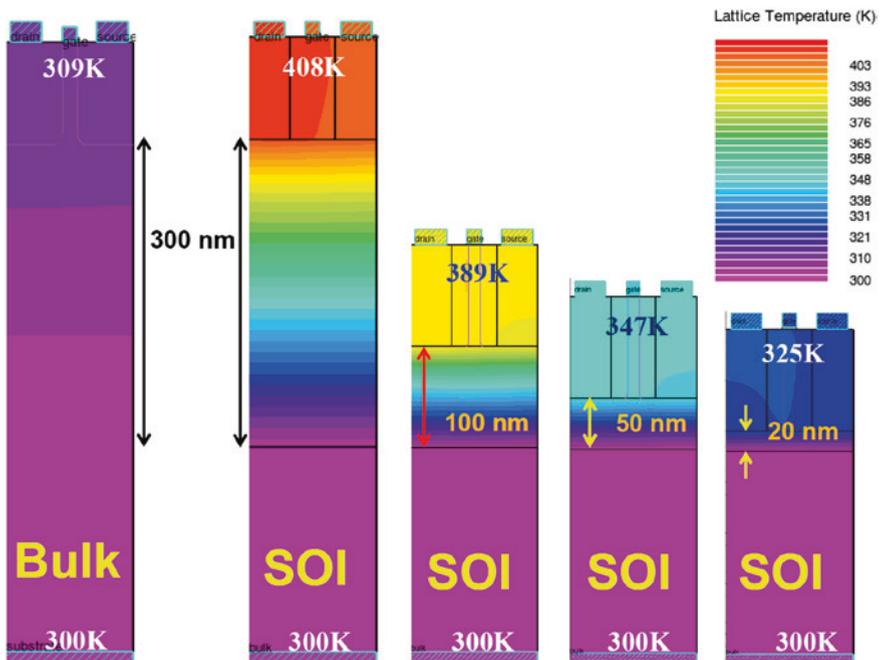
**Fig. 25** Drain current fluctuation at the  $V_{GS}-V_{th}$  of 0.05 V and  $V_{DS}$  of 0.05 V as a function of the distance between the percolation path and trap. A distance of 0 nm means that the trap position corresponds to the percolation path



percolation path is  $2 \times 2 \text{ nm}^2$  in the cross-section cut across the fin body, located near the surface of the fin body while contacting the gate oxide. When the distance becomes 10 nm, the variation is slightly decreased, through still similar to that at the distance of 0 nm. The dashed–dotted line represents the current variation without a percolation path. The variations were larger with a percolation path. As the distance increases to 25 nm, the variation decreases appreciably, even dropping below that without percolation due to the higher drain current with the percolation path than without. In a planar (2-D) MOSFET with the same channel length and width,  $V_{th}$ , and bias conditions, the drain current variation is 5.7 % when the distance is 0 nm.

### 6.2 Device Temperature

When MOSFETs are turned on, a temperature increase in the channel should occur due to Joule heating. Conventional SOI MOSFETs have experienced heat



**Fig. 26** Temperature contours in cross-sectional views of the fin body, cut along the channel length, when the 14 nm FinFETs are turned on. The temperature contours in SOI FinFETs are shown with BOX thickness from 300 to 20 nm, and are compared to the contour of the bulk FinFET (*leftmost*). The *arrows* in the cross-sections of SOI FinFETs indicate the thickness of the BOX

dissipation problems because of poor thermal conductivity of the buried oxide ( $\text{SiO}_2$  0.8–1.4 W/m K) [57] compared to that of crystalline Si (~150 W/m K) [58] at room temperature. Thus, crystalline Si has over 100-fold higher thermal conductivity than amorphous  $\text{SiO}_2$ . If the temperature in the channel is not reduced, the carrier mobility will be decreased, leading to low drain current, and finally, low-speed operation. Here, we investigate the temperature generated in the channel of 14 nm bulk and SOI FinFETs. Figure 26 shows the temperature contour in cross-sectional views cut along the channel length of the fin body when the devices are turned on. In this simulation, the electrode for substrate contact is grounded and acts as a thermal contact, fixed at 300 K. Examination of the maximum temperatures displayed on top of the cross-sectional views reveals the maximum device temperature of 309 K in the 14 nm bulk FinFET (the left). In contrast, the 14 nm SOI FinFET with a BOX thickness of 300 nm (the second) displays a maximum temperature of 408 K. If the BOX thickness is reduced to 20 nm, the maximum temperature in the 14 nm SOI FinFET can be reduced to 325 K.

Thus, it is required that the BOX thickness be reduced to 20 nm and beyond to allow effective transfer of the heat generated in the channel to the substrate. In this case, increase of the parasitic capacitances between the gate, the source, and the drain to the substrate should be addressed.

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