Chapter 2
Development of High-Endurance and Long-Retention FeFETs of Pt/$Ca_ySr_{1-y}Bi_2Ta_2O_9$/$(HfO_2)_x(Al_2O_3)_{1-x}$/Si Gate Stacks

Mitsue Takahashi and Shigeki Sakai

Abstract Studies of our Pt/$Ca_ySr_{1-y}Bi_2Ta_2O_9$(CSBT(y))/$(HfO_2)_x(Al_2O_3)_{1-x}$(HAO(x))/Si MFIS FeFETs were reviewed which were originated from the Pt/$SrBi_2Ta_2O_9$(SBT)/HAO(x = 0.75)/Si FeFET invented in 2002. Electrical properties of the fist FeFET were introduced which were 10^6 s-long retention, 10^{12} cycles-high endurance and 4×10^{-8} s-demonstrated writing speed. Stable I_d–V_g curves and I_d-retentions were measured up to 85 °C using p-channel FeFETs. Individual requirements to the M, F, I and IL layers as the components of MFIS were discussed using a band profile of the Pt/SBT/HAO(x = 0.75)/Si. Experimental studies for improving the HAO(x) and IL layer qualities were introduced. The composition ratio x in HAO(x) was optimized using single HAO(x) films and the MIS characters which all underwent a standard 800 °C annealing for SBT poly-crystallization. The ratio $x \geqq 0.75$ was found to be suitable for the I layer in the MFIS. As an ambient gas in depositing HAO(x = 0.75) by PLD, O_2 and N_2 were compared. In the Pt/SBT/HAO(x = 0.75)/Si FeFET, the HAO worked as a material-diffusion barrier only when it was deposited in N_2. Effect of increasing the ambient N_2 pressure was studied using the FeFETs. The pressure should be less than 40 Pa for keeping a clear interface between the SBT and HAO. Direct nitriding Si was studied for enlarging the memory window of Pt/SBT/HAO(x = 0.75)/Si FeFET. Oxinitriding Si was also demonstrated as a modified way to decrease the subthreshold-voltage swing of the FeFET. Experimental works to use CSBT(y) instead of the SBT was also introduced. The Pt/CSBT(y = 0.1, 0.2)/HAO(x = 0.75)/Si FeFETs showed wider pulse-memory window V_{plsW} than the reference Pt/SBT/HAO(x = 0.75)/Si FeFET at the common measurement conditions. When (V_E, V_P) = (−5, 7 V) and t_{pls} = 1 μs, the Pt/CSBT(y = 0.1, 0.2)/HAO(x = 0.75)/Si

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FeFETs showed V_{plsW} = 0.35 V which was 13 % larger V_{plsW} than the reference FeFET.

2.1 Introduction

In developing semiconductor memories, downsizing has been a general trend common to all memories for long time. The most successful semiconductor memory today is a flash memory which has advantages of not only data non-volatility with low-power consumption but also high scalability. Recently the flash memory has the feature size under 20 nm and is coming close to the limit of downsizing worth developing and manufacturing at a huge cost [1]. Alternative or supplemental nonvolatile memories, so-called emerging memories, have been intensively developed which have some additional values of faster access speed, higher endurance and lower power consumption than the conventional flash memory. The emerging memories are using functional materials such as resistive switching, phase change, magnetic and ferroelectric [2].

Ferroelectric-gate field effect transistor (FeFET) is a nonvolatile memory transistor using a ferroelectric material in the gate insulator [3]. The FeFET is a voltage-driven one-transistor (1T) memory as well as a flash memory cell. The 1T memories have advantages of non-destructive-read operation and potential high scalability in integrating memory cells by $4F^2$. The F is a feature size which is the minimum size manufacturable in every semiconductor-process generation. An FeFET is using ferroelectric-polarization switching for programming and erasing the data. Hence it has the intrinsic low-power consumption and high endurance against program-and-erase cycles. Actually we reported that FeFETs of metal/ferroelectric/insulator/semiconductor (MFIS) gate stacks had about 1/3 as small program voltage and 10^4 times as high endurance as a flash-memory cell [4, 5]. As far, we have investigated the MFIS FeFET with two directions. One is finding a good fabrication process for downsizing the single FeFETs which leads to the future manufacturing process. The other is demonstrating operations of multiple-FeFET integrated circuits introduced later in Chap. 13. This chapter is a part of the former research directions in which we discuss materials and the fabrication process of MFIS FeFETs to increase the memory windows in preparation for the prospective reduction of the F layer thicknesses. The thinning of the Flayer is important for downsizing an FeFET because the F layer is occupying the most volume of the gate stack. Since we reported the first self-aligned-gate FeFET with at least 33.5 days-long retention in 2005 [6], gate length of FeFET was decreased from the early 2 μm to the recent 100 nm with our technological progress in lithography, etching and ion implantation. On the basis of the studies reviews in this chapter, the 100 nm-gate size FeFETs with 4×10^5 s long retentions and 10^8 cycles endurances were achieved [7, 8].

The first long-retention FeFETs were invented in 2002 by Sakai. The structures and production method were patent-applied [9] and the electrical properties were

press-released [10]. Later the characterization of the 1×10^6 s-long retention, the 10^{12} cycles-high endurance and writing speed was reported by Sakai and Ilangovan in an academic paper [11]. The FeFETs had MFIS gate stacks of $Pt/SrBi_2Ta_2O_9(SBT)/(HfO_2)_x(Al_2O_3)_{1-x}(HAO)/Si$ [9–11] or $Pt/SBT/HfO_2/Si$ [9]. The SBT is a kind of bismuth-layered perovskite ferroelectric materials. Weak fatigues and small leakage currents of metal/ferroelectric/metal (MFM) capacitors using the SBT were reported [12]. The ferroelectric SBT is often made from a precursor oxide Sr-Bi–Ta-O by a poly-crystallization annealing. The annealing temperature at least 650 °C is necessary and that around 800 °C is sufficient for exhibiting the ferroelectric performance effectively [13]. Otherwise, if the annealing temperature is 550 °C for example, the raw material will grow into cubic crystals with paraelectric natures [14]. Since 2002, we have developed the MFIS FeFET according to the device fabrication policy as follows. The top priority was using bismuth-layered perovskite ferroelectrics like the SBT and CSBT for the F layer in the expectation of producing high-endurance FeFETs derived from the fatigue-free natures of the ferroelectric materials [12]. The second was annealing the MFIS in high temperature at about 800 °C for maximizing the ferroelectric quality. Materials for the M and I were selected from heat resistant materials. We tested their compatibility with Si and the bismuth-layered perovskite by stacking them in MFIS and annealing at about 800 °C altogether. The MFIS of Pt/SBT/HAO/Si was the first successful solution to realize an excellent FeFET with long retention and high endurance [9–11]. Since then, single FeFETs have been developed on a basis of advancing the Pt/SBT/HAO/Si as follows.

2.2 Basic Fabrication Process and Characterization of Pt/SBT/HAO/Si FeFETs

2.2.1 Fabrication Process

We introduce our basic fabrication process of *n*-channel non-self-aligned-gate FeFETs consisting of Pt/SBT/HAO/Si stack. Schematic cross-section of an *n*-channel non-self-aligned-gate MFIS FeFET is shown in Fig. 2.1. First, *p*-type Si wafers were prepared on which n^+ source-and-drain and p^+ substrate regions for probing were formed in advance. After removing a sacrificial SiO_2 on the Si by

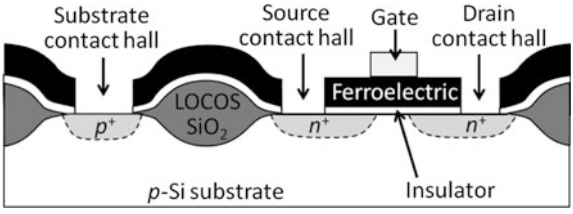

Fig. 2.1 Schematic cross-section of non-selfaligned gate FeFET

buffered hydrofluoric acid (BHF), HAO(x = 0.75) was deposited on the Si by KrF-excimer pulsed-laser-deposition (PLD) in 13 Pa N_2 ambient at 200 °C substrate temperature. A ceramic target of Hf–Al-O with the molar ratio corresponding to HfO_2:Al_2O_3 = 3:1 was used for depositing the HAO. Then $SrBi_2Ta_2O_9$ (SBT) was deposited on the HAO/Si by the PLD in 13 Pa O_2 ambient at 400 °C substrate temperature. A ceramic target of Sr–Bi–Ta–O with the element ratio Sr:Bi:Ta = 1:3:2 was used for depositing the SBT. On the SBT/HAO/Si, Pt was deposited in vacuum by 50 kV electron-beam (EB) evaporator. The thicknesses of the Pt, SBT and HAO layers were controlled by the individual deposition-time lengths. For example, the thicknesses we often used were about 200 nm for the Pt, 400 nm for the SBT and 13 nm for the HAO. The Pt thickness was verified by a stylus profiler. The SBT and HAO thicknesses were verified by an ellipsometer. After preparing the Pt/SBT/HAO/Si, the stack was once annealed in 1 atm O_2 at 400 °C for 30 min in a furnace. Photo-resist masks of the FeFET gates were patterned on the Pt/SBT/HAO/Si by photolithography using a g-line stepper. The next process was an etching by Ar^+ ion milling with the beam voltage 500 V and current 20 mA in 1.3×10^{-4} torr Ar ambient. The Pt gate electrodes were formed by the Ar^+ milling. The typical gate length (L) of a non-self-aligned gate FeFET was L = 10 μm. The gate widths (W) were W = 10, 20, 40, 50, 80, 100, 150 and 200 μm which were the typical pattern sizes in a photo-mask set of ours. The Pt/SBT/HAO/Si was annealed in O_2 at 800 °C for the SBT poly-crystallization. Then the photolithography was used again for making photo-resist patterns to open source-and-drain and substrate contact holes on the Si by Ar^+ ion milling. Consequently, we completed fabrication of an FeFET. The FeFET was a kind of metal-oxide-semiconductor (MOS) FETs having four terminals of gate, drain, source and substrate. The FeFETs were characterized by measurements of drain current versus gate voltage (I_d–V_g) curves, data retention, endurance, and writing speed as follows.

2.2.2 Static Memory Window

Static memory window is basic information of an FeFET quality as a memory device. It is characterized by I_d–V_g curves measured using a semiconductor parameter analyzer. The I_d–V_g curve is drawn by measuring I_d values of an FeFET with static scanning V_g from $V_{base} - V_{SA}$ to $V_{base} + V_{SA}$ and back to $V_{base} - V_{SA}$ or in a simplified description $V_g = V_{base} \pm V_{SA}$. The V_{base} is a base V_g and the V_{SA} is V_g scan amplitude.

Figure 2.2a showed an I_d–V_g of a Pt/SBT/HAO(x = 0.75)/Si FeFET measured at $V_g = \pm 6$ V which meant V_{base} = 0 V and V_{SA} = 6 V [11]. The drain voltage (V_d), source voltage (V_s), substrate voltage (V_{sub}) were kept at V_d = 0.1 V and $V_s = V_{sub}$ = 0 V. The n-channel FeFET shows the counterclockwise I_d–V_g loop with the right upward- and left downward-paths as indicated in Fig. 2.2a. A p-channel FeFET shows the opposite clockwise I_d–V_g loop as later shown in

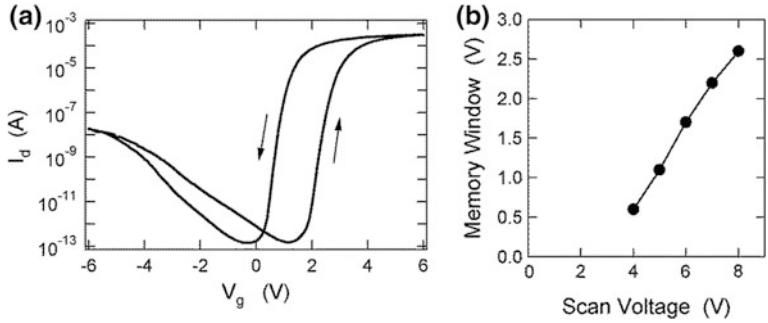

Fig. 2.2 **a** I_d–V_g curve of an *n*-channel Pt/SBT/HAO(x = 0.75)/Si FeFET with L = 10 μm and W = 200 μm. Thicknesses in the gate stack were 200 nm Pt, 400 nm SBT and 13 nm HAO. **b** $V_w - V_{SA}$ extracted from the I_d–V_g curves for various V_{SA}. Modified from [11]

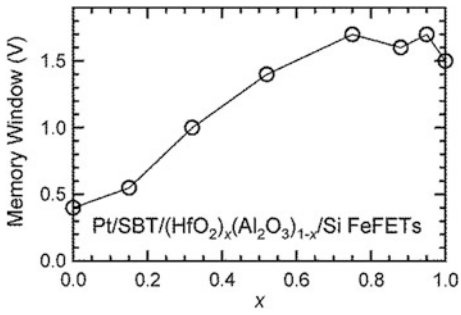

Fig. 2.3 x dependence of static memory window at V_g = ±6 V of *n*-channel Pt/SBT/HAO(x)/Si FeFETs. Thicknesses in the gate stack were 200 nm Pt, 400 nm SBT and 14 nm HAO(x). The gate area sizes were L = 10 μm and W = 200 μm. Modified from [15]

Fig. 2.8. Static memory window (V_w) of an FeFET was defined as a difference between two threshold voltage (V_{th}) values in the I_d–V_g loop which were regarded as the V_g values at $I_d = 10^{-6}$ A for simplification in this work. The reason of using x = 0.75 in HAO was the largest static memory window of the Pt/SBT/HAO (x = 0.75)/Si FeFET among the Pt/SBT/HAO(x)/Si FeFET with the x ranged from 0 to 1.0 [9, 15] as indicated in Fig. 2.3. The memory windows at V_g = 2 ± 6 V were extracted from the I_d–V_g curves of the FeFETs which were annealed at 800 °C in O_2 for 1 h. Thicknesses were 200 nm for the Pt, 14 nm for the HAO and 400 nm for the SBT.

I_d–V_g curves of the Pt/SBT/HAO(x = 0.75)/Si FeFET were precisely measured at various V_g ranged from V_g = ±4 V to ±8 V. The V_w extracted from the I_d–V_g curves exhibited a monotonic increase as the V_{SA} was raised from 4 to 8 V as shown in Fig. 2.2b [11]. The increasing V_W in Fig. 2.2b indicated that ferroelectric polarization of the SBT in the FeFET was not saturated even at the large V_{SA} of 8 V. The reason of the unsaturated SBT polarization was a growth of an interfacial layer (IL) between the HAO and Si during the SBT crystallization annealing at 800 °C [15–17]. As shown in Fig. 2.4, cross-sectional transmission electron microscopy (TEM) and the point analyses by energy dispersive X-ray spectroscopy

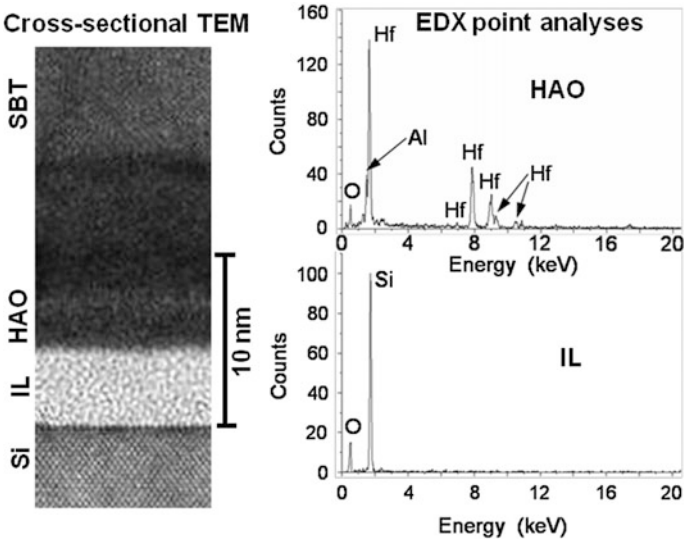

Fig. 2.4 Cross-sectional TEM picture of an SBT/HAO(x = 0.75)/Si sample and the EDX point analyses at the HAO and the IL. The sample underwent an O_2 annealing at 800 °C for 1 h. The deposited initial thicknesses were 400 nm SBT and 14 nm HAO. Modified from [15]

(EDX) suggested that the IL was SiO_2 with a low dielectric constant of ε_{IL} = 3.9. The total V_g across the MFIS was divided and shared among the layers of F, I and S, in proportion to the inverse of the individual capacitances connected in series. Under a given V_g, the voltage across the IL-SiO_2 was fairly large because of the low ε_{IL}. As a result, the voltage across the SBT became so small that the FeFET shows the unsaturated polarization as indicated in Fig. 2.2b. From the different points of view, however, the growth of the IL also gives a benefit of protecting the Si interface by the flat SiO_2 film with the uniform quality as later discussed in Sect. 2.3. The good Si interface was suggested by the steep I_d–V_g curves with a small subthreshold-voltage swing (S). The S in our FeFET works was basically about S = 100 mV/decade as we later described in Sect. 2.3.2.

2.2.3 Retention

Retention of an FeFET is hold-time dependence of either I_d or V_{th} binary state. It is the evidence of data nonvolatility of the FeFET. In this study, we measured I_d retentions which were the time-dependences of two I_d values for on- and off-states, respectively. The on-state I_d versus time (I_d–t) was measured after a programming gate voltage $V_g = V_P$ was applied. The off-state I_d–t was measured after an erasing gate voltage $V_g = V_E$ was applied. Each I_d–t curve was measured with keeping a common hold gate voltage $V_g = V_{hold}$. As shown in Fig. 2.5, a Pt/SBT/HAO/Si

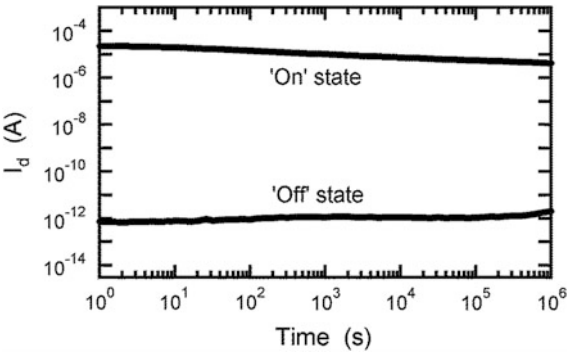

Fig. 2.5 I_d-retention of an *n*-channel FeFET measured at V_{hold} = 1.7 V after the poling by V_g = ±6 V. The FeFET had Pt/SBT/HAO(x = 0.75)/Si. Thicknesses in the gate stack were 200 nm Pt, 400 nm SBT and 13 nm HAO. The gate area size was L = 10 μm and W = 200 μm. Modified from [11]

FeFET exhibited the I_d retentions with no significant degradation for at least 1×10^6 s or 11.6 days [11]. They were measured at room temperature. For the on-state I_d measurement, $V_g = V_P = 6$ V was applied for poling then reduced to $V_g = V_{hold} = 1.7$ V. The V_g was applied by a dc voltage source connected to the gate and substrate of the FeFET. During the V_g swing, we kept V_d, V_s and V_{sub} at $V_d = V_s = V_{sub} = 0$ V. The on-state I_d measurement was immediately started and was continued for 1×10^6 s with keeping $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. The I_d–t was measured by a time-sampling mode of a semiconductor parameter analyzer connected to the drain and source of the FeFET. For the off-state I_d measurement, $V_g = V_E = -6$ V was applied for poling then raised to $V_g = V_{hold} = 1.7$ V by a dc voltage source with keeping $V_d = V_s = V_{sub} = 0$ V. The off-state I_d measurement was immediately started and was continued for 1×10^6 s with keeping $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V by the semiconductor parameter analyzer in the time-sampling mode. In this study, we empirically determined the V_{hold} to maximize the ratio of the on-state log(I_d) to the off-state log(I_d). There was a strong positive correlation between the V_{hold} and the flat-band voltage of the MFIS, therefore, we could adjust the V_{hold} to $V_{hold} = 0$ V by optimizing the ion-implantation condition of the Si [18]. The other option for reducing the V_{hold} to 0 V may be using another heat-resistive metal for the M layer which has a smaller work function than Pt [19].

2.2.4 Endurance

Endurance of an FeFET shows how many times of program and erase operations are accepted before incorrect writing begins due to the FeFET degradation. The endurance of a Pt/SBT/HAO/Si FeFET was investigated by measuring static I_d–V_g curves after many cycles of endurance pulses were imposed. In this study, the endurance pulses were V_g pulses of alternate $V_P = 8$ V and $V_E = -8$ V with 1 μs period as shown in the inset of Fig. 2.6 [11]. The endurance V_g pulses applied on the gate were outputted from a pulse generator and transmitted through a 50 Ω coaxial cable terminated with a 50 Ω resistance. Accuracy of the pulse-wave forms

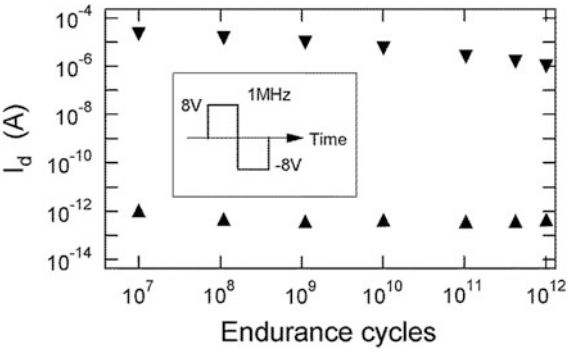

Fig. 2.6 Endurance of an *n*-channel Pt/SBT/HAO (x = 0.75)/Si FeFET. The inset shows a V_g endurance-pulse cycle. Thicknesses in the gate stack were 200 nm Pt, 400 nm SBT and 13 nm HAO. The gate area size was L = 10 μm and W = 200 μm. Modified from [11]

were checked by an oscilloscope in advance. We fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub} = 0$ V during the endurance pulses were imposed. Every time after counting the accumulated numbers of endurance cycles to 10^7, 10^8, 10^9, 10^{10}, 10^{11}, 5×10^{11} and 10^{12}, the pulse application was interrupted and the V_g connection was changed to a semiconductor parameter analyzer. Then a static I_d–V_g curve was drawn by scanning V_g from −6 to 6 V and back to −6 V, or $V_g = \pm 6$ V in a simplified description, with keeping $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. On- and off-state I_d values were extracted from the I_d–V_g loop at a common $V_g = 2$ V and plotted in Fig. 2.6. After drawing the static I_d–V_g curve by $V_g = \pm 6$ V, the V_g connection was changed back to the pulse generator and the endurance-pulse application was resumed toward the next accumulated number of endurance cycles. As shown in Fig. 2.6, the FeFET maintained more than 6 order difference between the on- and off-state I_d values even after 10^{12} endurance cycles. Note that V_{th} endurance was recently investigated as discussed in Sects. 2.5 and 2.6 instead of the I_d endurance introduced in this study.

2.2.5 *Writing Speed*

Pulse writing is a substantial writing technique rather than the static writing for the practical FeFET use. Writing speed of an FeFET is estimated by measuring V_g-pulse-width (t_{pls}) dependence of either I_d or V_{th} binary state. To be exact, the writing is programming and erasing. As mentioned in Sect. 2.2.2, ferroelectric polarization in FeFETs is usually unsaturated. According to a study of ferroelectric switching kinetics [20], unsaturated polarizations tend to have slower switching speeds than saturated polarizations. The study suggests that FeFETs have significant t_{pls} dependence of the memory windows due to the unsaturated ferroelectric polarizations. As t_{pls} increases, memory windows measured by the pulsed V_g applications become close to those measured by static V_g applications.

In this work, we introduced the t_{pls} dependence of I_d in programming and erasing a Pt/SBT/HAO(x = 0.75)/Si FeFET as shown in Fig. 2.7 [11]. The gate and

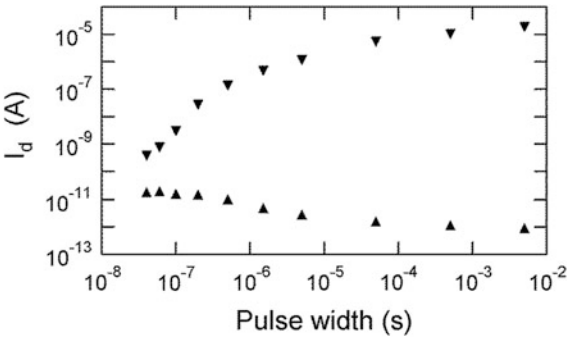

Fig. 2.7 Pulse width t_{pls} dependence of on- and off-state I_d value of an n-channel Pt/SBT/HAO (x = 0.75)/Si FeFET. Thicknesses in the gate stack were 200 nm Pt, 400 nm SBT and 13 nm HAO. The gate area size was L = 10 μm and W = 200 μm. Modified from [11]. Unpublished data were added

substrate of the FeFET were connected to a pulse generator. The drain and source of the FeFET were connected to a semiconductor parameter analyzer. The single V_g pulses were outputted from the pulse generator and transmitted through a 50 Ω coaxial cable terminated with a 50 Ω resistance. Accuracy of the pulse shape was confirmed using ($2 \times t_{pls}$)-period ±8 V V_g wave by an oscilloscope in advance. The pair of $I_d - t_{pls}$ characteristics for 8 and −8 V V_g-pulse applications was measured with stepping up the t_{pls} from 4×10^{-8} to 5×10^{-3} s. For measuring an on-state-I_d at a t_{pls}, a single programming V_g pulse of a fixed height V_P and the time width t_{pls} was applied by the pulse generator. During the programming V_g pulse application, we fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub} = 0$ V. In the programming V_g pulse, V_g started from $V_{base} = 2$ V, increased to $V_P = 8$ V, kept at the V_P for t_{pls} and back to the V_{base}. With holding the V_{base} on the gate, the on-state-I_d measurement immediately began using the semiconductor parameter analyzer in a time-sampling mode at $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. Next, for measuring an off-state-I_d at the t_{pls}, a single erasing V_g pulse of a fixed height V_E and the time width t_{pls} was applied by the pulse generator. During the erasing V_g pulse application, we fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub} = 0$ V. In the erasing V_g pulse, V_g started from $V_{base} = 2$ V, decreased to $V_E = -8$ V, kept at the V_E for t_{pls} and back to the V_{base}. With holding the V_{base} on the gate, the off-state-I_d measurement immediately began using the semiconductor parameter analyzer in the time-sampling mode at $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V. As shown in Fig. 2.7, the FeFET still remained the on/off-I_d ratio of more than one order, exactly 26, at a fastest writing speed of $t_{pls} = 4 \times 10^{-8}$ s.

2.2.6 I_d–V_g and Retention at Elevated Temperatures

Finally, we introduce electrical properties of p-channel Pt/SBT/HAO/Si FeFETs [21]. The difference from the n-channel one was using n-type Si wafers with p^+ source-and-drain and n^+ substrate regions for probing. Thicknesses of the Pt, SBT and HAO layers were about 200, 600 and 7 nm, respectively. Figure 2.8 shows

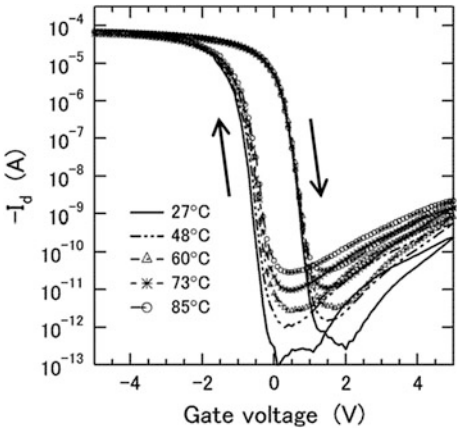

Fig. 2.8 static I_d–V_g curves of a *p*-channel Pt/SBT/HAO (x = 0.75)/Si FeFET measured at elevated temperatures from 27 to 85 °C. Thicknesses in the gate stack were 200 nm Pt, 600 nm SBT and 7 nm HAO. The gate area size was L = 10 μm and W = 200 μm. Modified from [21]

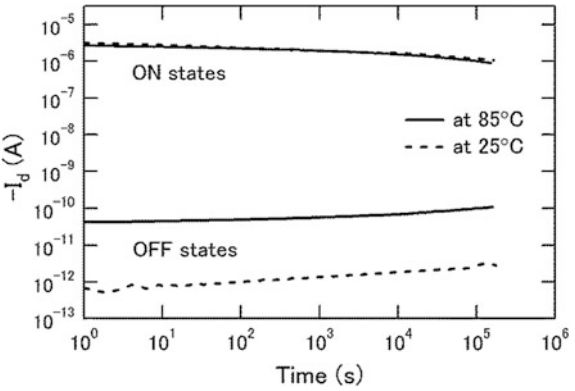

Fig. 2.9 I_d-retentions of a *p*-channel Pt/SBT/HAO (x = 0.75)/Si FeFET measured at 27 and 85 °C. Thicknesses in the gate stack were 200 nm Pt, 600 nm SBT and 7 nm HAO. The gate area size was L = 10 μm and W = 200 μm. Modified from [21]

static I_d–V_g curves of the FeFET measured at elevated temperatures from 27 to 85 °C [21]. The temperature was the sample-stage temperature of a manual prober. The I_d–V_g loops of the *p*-channel FeFET were drawn in clockwise directions by scanning V_g from −5 to 5 V and back to −5 V with keeping V_d = −0.1 V and $V_s = V_{sub}$ = 0 V. As shown in Fig. 2.9, the I_d-retentions measured at 27 and 85 °C showed stable curves for more than 10^5 s [21]. The on-state I_d was measured at $V_g = V_{hold}$ = 0 V, V_d = −0.1 V and $V_s = V_{sub}$ = 0 V, after the poling by $V_g = V_P$ = −5 V and $V_d = V_s = V_{sub}$ = 0 V. The off-state I_d was measured also at $V_g = V_{hold}$ = 0 V, V_d = −0.1 V and $V_s = V_{sub}$ = 0 V, after the poling by $V_g = V_E$ = 5 V and $V_d = V_s = V_{sub}$ = 0 V. The V_{hold} of 0 V during the retention measurements indicated that the *p*-channel FeFET had the appropriate impurity concentration in the Si channel as mentioned in Sect. 2.2.3.

2.3 Requirements to the Layers in MFIS

2.3.1 Requirements to the Layers M, F, I

We will review the requirements to the M, F, and I layers. All the material of the M, F and I layers must be heatproof enough to show material stabilities even through an annealing process of the MFIS stack all at once. The material stability means that they do not have either significant reactions or element diffusions at the interfaces among the layers of the M, F, I and S. The annealing temperature is determined by crystallization temperature of the F-layer material for securing the ferroelectric performance. The temperature is about 800 °C in using SBT for the F material as we mentioned in Sect. 2.2.1. In this chapter, we introduced the experimental works only using Pt as the M layer and Si as the S substrate. With regard to the M layer, there may be an option of choosing another material with smaller work function [19] than the Pt in expectation of adjusting the V_{th} of the FeFET for V_{hold} = 0 V.

Requirements to the F and the I layers are very much related with each other on the points of equivalent oxide thickness (EOT) and band alignment. Figure 2.10a shows the band profile of the Pt/SBT/HAO(x = 0.75)/Si FeFET at V_g = 5.95 V for programming [22]. The assumed thicknesses were 200 nm Pt, 200 nm SBT, 7 nm HAO and 3.5 nm IL. The IL was a thermally grown SiO_2 as indicated in Fig. 2.4. The band profile was drawn on the assumption that the F layer shows the unsaturated ferroelectric polarization along the minor loop of polarization *versus* electric field (P–E) as indicated in Fig. 2.10b [23]. As we discussed in Sect. 2.2.2, the total V_g across the MFIS was divided and shared among the layers of F, I and S, in proportion to the inverse of the individual capacitances connected in series. The F

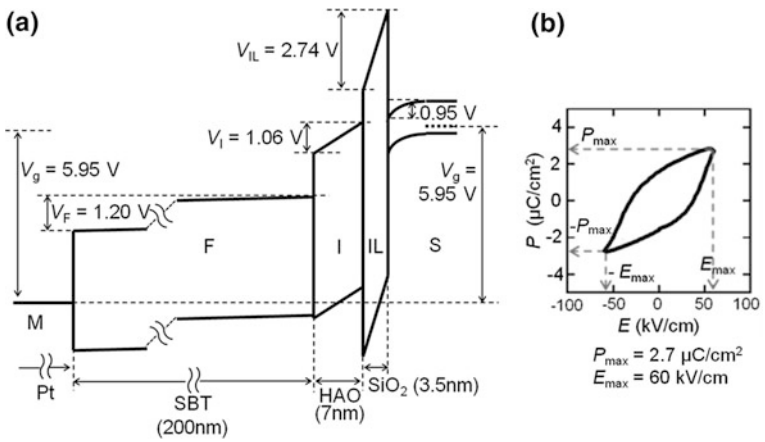

Fig. 2.10 **a** Band profile of the Pt/SBT/HAO(x = 0.75)/Si FeFET at V_g = 5.95 V for programming. **b** Assumed P–E curve of the SBT in the FeFET. The curve was measured using an MFM capacitor of SBT. Modified from [22]

layer had a small V_g share of V_F = 1.2 V because the IL took much voltage of V_{IL} = 2.74 V as indicated in Fig. 2.10a. The ways to increase the memory window V_w of the FeFET from the view point of EOT, the F layer should have a relatively large EOT(F), and the I-and-IL total layers should have a relatively small EOT (I, IL) in comparison with their present states. Increasing the EOT(F) is difficult because the F material usually have a high dielectric constant ε_F and the F layer thickness d_F is to be reduced for the physical downsizing of the FeFET as we discussed layer in Sect. 2.6. Therefore the EOT(I, IL) must be decreased either by reducing the physical thicknesses d_I and d_{IL}, or by increasing the dielectric constants ε_I and ε_{IL} of the I-and-IL layers.

2.3.2 *Requirements Especially to the I-and-IL Layers*

Thinning the d_{IL} and increasing the ε_{IL} are required as discussed in Sect. 2.3.1. The d_{IL} can be decreased by much reducing the FeFET annealing temperature. It will be possible by drastic changing of the F material which is out of the scope in this chapter. Our work of increasing the ε_{IL} in later introduced in Sect. 2.5. The existence of the IL has some benefits to the FeFET. As indicated in Fig. 2.10a, the IL has a large band gap which aligned in the MFIS band profile as a good electrical barrier against charge injection from the S toward the F. Moreover the IL has a role of preserving good Si interface with little state densities. The good Si interfaces were indicated by many steep I_d–V_g curves with small subthreshold-voltage swings (S) about S = 100 mV/decade as we demonstrated in many works reviewed in this chapter. The S value was defined as $S = \ln 10 \cdot dV_g/d(\ln I_d)$ [24].

With regard to the I layer, thinning the d_I and increasing the ε_L is required in addition to the material stability at high temperature about as discussed in Sect. 2.3.1. A thin-deposited high-k material will satisfy the requirements. From the viewpoint of band alignment in the MFIS, there is another requirement of the I layer. It is a higher barrier of the I layer than that of the F layer both against electrons and holes. Otherwise, the I layer forms a potential well between the SBT and a high-barrier IL which causes charge trapping. The uncontrollably trapped charges degrade the FeFET V_{th} stability. To summarize the requirements to the I layer, high-temperature-proof, thin-deposited high-k material with higher barriers than the F layer against electrons and holes is wanted.

A good candidate material of the I layer is $(HfO_2)_x(Al_2O_3)_{1-x}$ (HAO). It is 800 °C-resistive as we demonstrated in Fig. 2.4 and high-k of ε_I ranged from 9 for x = 0 to 25 for x = 1.0 [25]. The HAO also has a larger energy gap than the SBT without forming a potential well between the SBT the SiO_2 [26]. Thus we investigated the HAO as the I layer of the Pt/SBT/HAO/Si FeFETs.

2.4 Preparation of HAO for Pt/SBT/HAO/Si Gate Stack

2.4.1 *Single HAO(x) and the MIS Characters at Various Composition Ratios*

We investigated the composition ratio x of $(HfO_2)_x(Al_2O_3)_{1-x}$ (HAO(x)) to be amorphous in Pt/SBT/HAO(x)/Si MFIS FeFETs even after an annealing for the SBT polycrystallization [15]. X-ray diffraction (XRD) of 50 nm-thick HAO (x) films deposited on Si substrates were studied. The x was varied from 0 to 1.0. All the samples for the XRD underwent an annealing at 800 °C in O_2 for 1 h. As shown in Fig. 2.11, only the HAO(x) with x = 1.0 and 0.95 exhibited a peak corresponding to HfO_2 crystallization. Cross-sectional TEM images of Pt/HAO(x)/Si MIS FETs suggested the HfO_2 crystallization in the HAO(x) with x = 1.0 and 0.95 [15]. In the TEM pictures, there were some spots of stripe patterns derived from the HfO_2 crystal lattice which were not found in Al_2O_3-rich HAO cross sections. The MIS FETs were fabricated by the same as described in Sect. 2.2.1, except for varying the x and no depositing the SBT. The gate-area sizes were L = 10 μm and W = 200 μm formed by photolithography and Ar^+ milling. Thicknesses were 200 nm for the Pt and 14 nm for the HAO(x). All of the MIS FETs were annealed at 800 °C in O_2 for 1 h in the same way as our basic Pt/SBT/HAO(x)/Si MFIS FETs underwent.

We measured static I_d–V_g and I_g–V_g curves of the MIS FETs for all the x [15]. There seemed negligibly small hystereses indicating no significant trapped charges in the I_d–V_g. As shown in Fig. 2.12, the MIS FETs had small gate-leakage current in the all x range. Precisely speaking, the I_g of the MIS FETs tended to be small as x was reduced. The cross-sectional TEM pictures indicated that the IL between the HAO(x) and Si in the MIS FETs became thick as the x was reduced toward

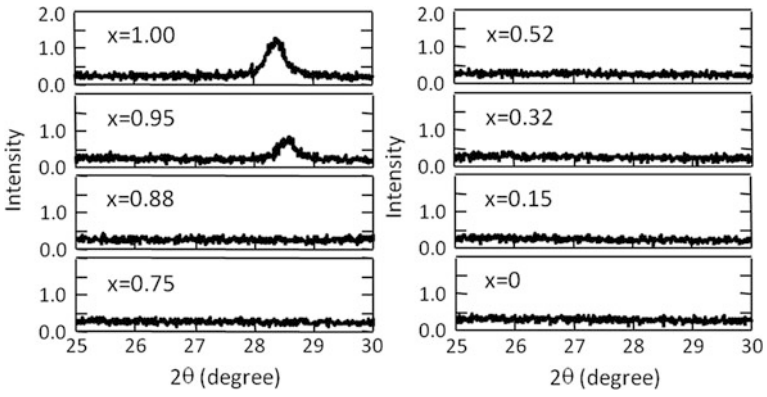

Fig. 2.11 XRD analyses of 50 nm-thick HAO(x) films deposited on Si substrates which all underwent annealing at 800 °C in O_2 for 1 h. The x was varied from 0 to 1.0. Modified from [15]

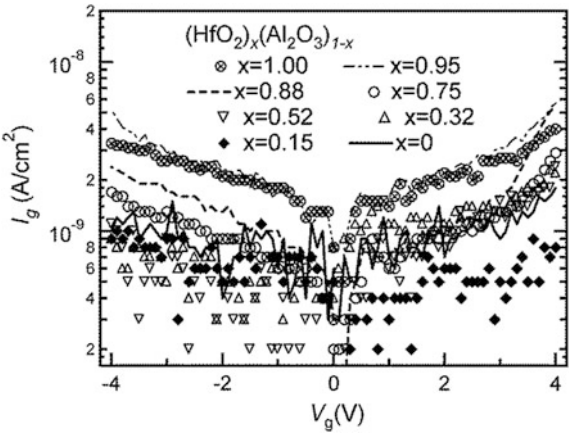

Fig. 2.12 Gate leakage currents of Pt/HAO(x)/Si MIS FETs with various x from 0 to 1.0. The all MIS FETs underwent annealing at 800 °C in O_2 for 1 h. They had the gate lengths of L = 10 μm and the gate widths of W = 80 and 20 μm. Deposited thicknesses were 200 nm for the Pt and 14 nm for the HAO common to the all MIS FETs. Modified from [15]

Al_2O_3-rich side [15]. The thick grown IL might be the reason of the I_g decrease as the x was reduced as indicated in Fig. 2.12.

In the MIS stack, EOT of the gate oxide was investigated by measuring capacitance vs V_g (C–V) curves [15]. The gate oxide was the double layer of HAO (x) and IL. Pt/HAO(x)/p-Si MIS diodes for various x from x = 0 to 1.0 were prepared. The gate area size was 200 μm × 200 μm formed by photolithography and Ar^+ milling. All of the MIS diodes were annealed at 800 °C in O_2 for 1 h. Hence they had IL grown on the Si. The MIS diode had two terminals: gate and substrate. The C–V curves were measured at 10 kHz by an LCR meter. The V_g was scanned and the V_{sub} was fixed to 0 V. There were no significant hystereses observed in the all C–V as shown in Fig. 2.13a. The capacitances at V_g = −2 V in the accumulation region were extracted from the C–V curves and plotted in Fig. 2.13b. The maximum C with the minimum EOT was observed at around x = 0.95. As a result of the works in this section, x = 0.75 was often used when we wanted amorphous and small-leakage HAO(x). We also used x = 1.0 for the largest ε_I = 25 [25] when suppressing the total EOT of HAO(x) and IL was prioritized.

2.4.2 *Comparison of O_2 and N_2 Ambient in Depositing HAO*

We verified which gas was better, O_2 or N_2, for the ambient during the HAO deposition by PLD [27]. Two types of Pt/SBT/HAO/p-Si diodes were prepared. One had the HAO named HAO(O) which was deposited to the physical thickness 15 nm in 13 Pa O_2 at 200 °C substrate temperature. The other had the HAO named HAO(N) which was deposited to the physical thickness 15 nm in 13 Pa N_2 at 200 °C substrate temperature. Fabrication process except for using O_2 ambient in deposition the HAO(O) was the same as described in Sect. 2.2.1. Thicknesses were 130–150 nm for the Pt, 400 nm for the SBT and 15 nm for both the HAO(N) and

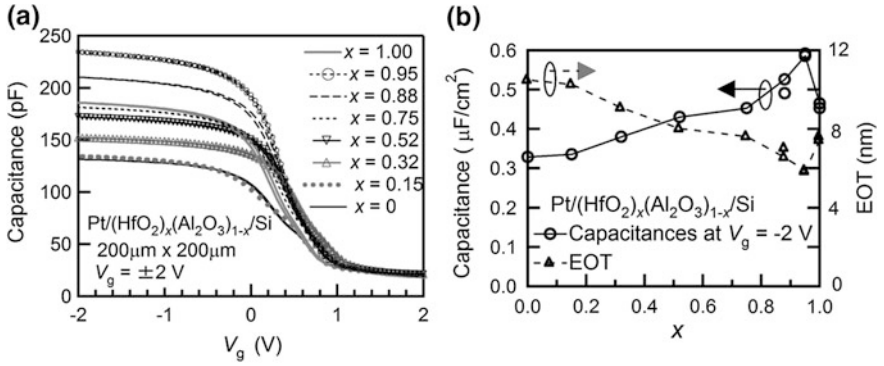

Fig. 2.13 **a** C–V curves of Pt/HAO(x)/p-Si MIS diodes for various x from $x = 0$ to 1.0. **b** x dependence of capacitors and the estimated EOT values of Pt/HAO(x)/p-Si MIS diodes. Deposited thicknesses were 200 nm for the Pt and 14 nm for the HAO common to the all diodes. The gate-electrode areas were 200 μm × 200 μm. Modified from [15]

HAO(O). An ellipsometer was used for understanding the precise deposition speeds of the HAO(N) and HAO(O) which significantly depended on the ambient gas kinds. Shapes of the Pt electrodes were 1.5 mm-diameter dots deposited using a metal hard mask. All the capacitors of Pt/SBT/HAO(N)/Si and Pt/SBT/HAO(O)/Si underwent an annealing process in 1 atm O_2 at 800 °C for 1 h. Backsides of the Si substrates were mechanically ground and covered with Al deposited by the EB evaporator. C–V characteristics of the Pt/SBT/HAO(N)/Si and Pt/SBT/HAO(O)/Si were measured at 10 kHz by an LCR meter. As shown in Fig. 2.14a, b, the C–V hysteresis curves were drawn in clock-wise directions which indicated ferroelectric-polarization switching on the p-type semiconductor. At every scan range of V_g, the Pt/SBT/HAO(N)/Si in Fig. 2.14a showed a larger V_w than the Pt/SBT/HAO(O)/Si in Fig. 2.14b. For example at $V_g = \pm 6$ V, the Pt/SBT/HAO (N)/Si showed $V_w = 0.9$ V while the Pt/SBT/HAO(O)/Si showed $V_w = 0.3$ V as indicated in Fig. 2.15. The reason of the small V_w of the Pt/SBT/HAO(O)/Si was a thick IL grown between the HAO(O) and Si. The IL thicknesses were confirmed by a cross-sectional scanning transmission electron microscope (STEM) [27]. The IL thickness in the Pt/SBT/HAO(O)/Si was 7.4 nm which was much larger than that in the Pt/SBT/HAO(N)/Si 3.4 nm. The IL has a dielectric constant $\varepsilon_{IL} = 3.9$ [15] which is the lowest among those of the SBT, HAO(O) and HAO(N). Hence much decrease of the V_w was caused by the 4 nm increase in the IL thickness.

We found that the IL growth on the Si was promoted by the HAO(O) because the HAO(O) did not work sufficiently as a material-diffusion barrier. Backside secondary-ion-mass-spectrometry (SIMS) gave us useful information about the quality as the material-diffusion barrier of the HAO(O) and HAO(N) as shown in Fig. 2.16. The elements Sr, Bi and Ta of the SBT in Fig. 2.16c–e had the intensity peaks at the depth of the HAO(O) while the same elements did not show penetrations into the HAO(N) location. As a conclusion of this work, O_2 was not a

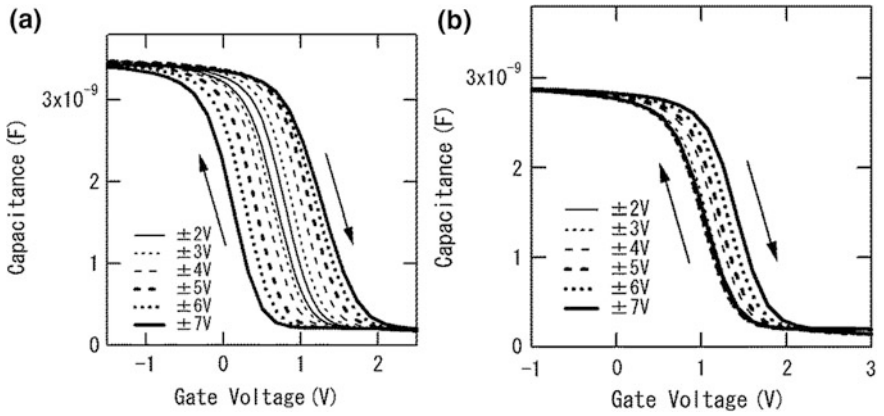

Fig. 2.14 *C–V* hysteresis curves of **a** Pt/SBT/HAO(N)/*p*-Si and **b** Pt/SBT/HAO(O)/*p*-Si MFIS diodes. Thicknesses were 130–150 nm Pt, 400 nm SBT and 15 nm for the HAO(N) and HAO(O). The gate-electrode areas were 1.5 mm-diameter dots. Modified from [27]

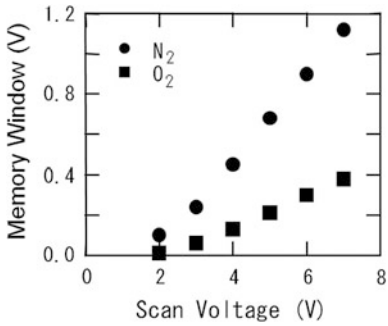

Fig. 2.15 Memory windows of Pt/SBT/HAO(N)/*p*-Si and Pt/SBT/HAO(O)/*p*-Si MFIS diodes extracted from *C–V* curves for various scan ranges of V_g in Fig. 2.14a, b. Modified from [27]

suitable ambient gas in depositing the HAO by PLD for preparing the Pt/SBT/HAO/Si stack. Therefore we selected N_2 ambient in depositing the HAO by the PLD.

2.4.3 *Effect of N_2 Ambient Pressure Increase in Depositing HAO*

We investigated effects of increasing ambient N_2 pressure during HAO deposition (P_{HAO}) in Pt/SBT/HAO/*p*-Si [28]. Fabrication process except for varying the P_{HAO} was the same as described in Sect. 2.2.1. The P_{HAO} was varied from 7 to 158 Pa. The all FeFETs had the gate area of $L = 10$ μm and $W = 200$ μm formed by photolithography and Ar^+ milling. Thicknesses were 250 nm for the Pt, 450 nm for the SBT and 10 nm for the HAO. I_d–V_g hysteresis curves of the FeFETs of

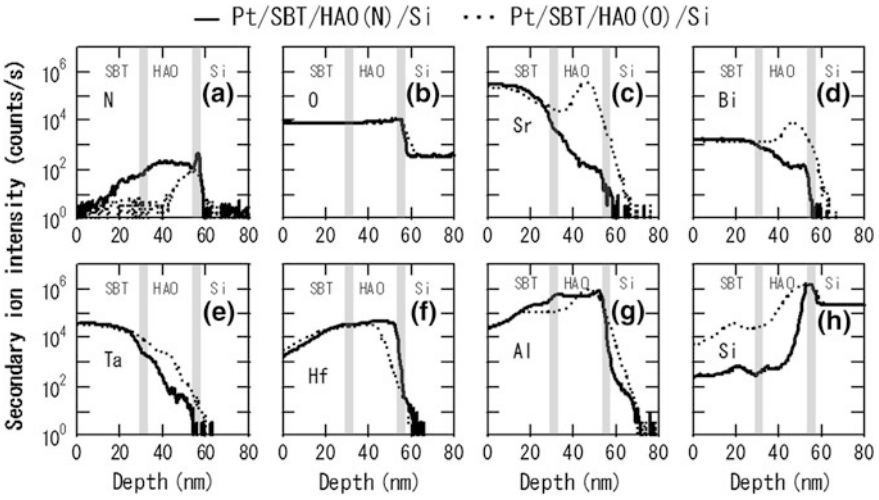

Fig. 2.16 SIMS profiles of Pt/SBT/HAO(N)/*p*-Si and Pt/SBT/HAO(O)/*p*-Si MFIS diodes. *Solid lines* were for Pt/SBT/HAO(N)/*p*-Si. *Dashed lines* were for Pt/SBT/HAO(O)/*p*-Si. Elements of **a** N, **b** O, **c** Sr, **d** Bi, **e** Ta, **f** Hf, **g** Al and **h** Si were studied. Modified from [27]

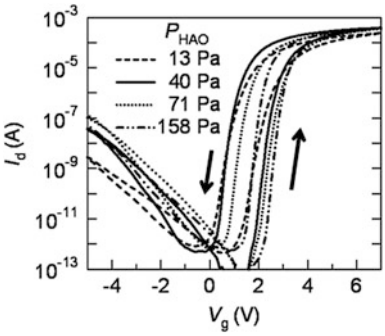

Fig. 2.17 I_d–V_g curves of *n*-channel Pt/SBT/HAO (x = 0.75)/Si FeFETs prepared at various P_{HAO} of 13, 40, 71 and 158 Pa during the HAO deposition. Thicknesses were 250 nm Pt, 450 nm SBT and 10 nm for the HAO. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [28]

P_{HAO} = 13, 40, 71 and 158 Pa were measured as shown in Fig. 2.17. The curves were drawn in counterclockwise directions which indicated ferroelectric polarization switching on *p*-Si substrates. Static memory windows (V_w) extracted from the I_d–V_g curves had broad peaks around P_{HAO} = 40 Pa. The largest V_w was about V_w = 1.5 V at V_g = 1 ± 6 V. Relatively small V_w at P_{HAO} > 40 Pa indicated that such large P_{HAO} on the contrary increased the total EOT of the HAO and IL. As shown in Fig. 2.18, cross-sectional STEM images of the FeFETs indicated the increasing tendency of the IL thickness and the HAO roughness as P_{HAO} was raised from 40 Pa. The rough HAO interface suggested that inter-diffusion of materials

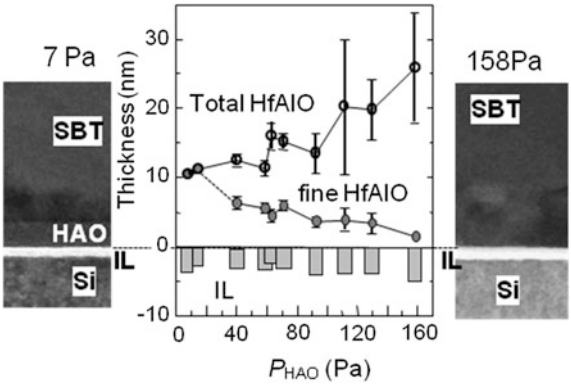

Fig. 2.18 Physical thicknesses of HAO and IL-SiO_2 measured by cross-sectional STEM images of *n*-channel Pt/SBT/HAO (x = 0.75)/Si FeFETs. They were prepared at various P_{HAO} ranged from 7 to 158 Pa during the HAO deposition. As-deposited HAO was 10 nm thick each. Modified from [28]

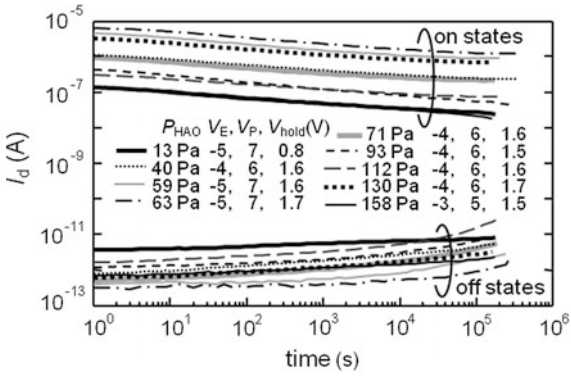

Fig. 2.19 I_d retentions of Pt/SBT/HAO/Si FeFETs in which the HAO layers were deposited in N_2 at P_{HAO} ranged from 13 to 158 Pa. Deposited thicknesses were 250 nm Pt, 450 nm SBT and 10 nm HAO common to all the FeFETs. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [28]. Unpublished data were added

between the HAO and the SBT became significant as the P_{HAO} was raised. At P_{HAO} = 13 Pa, the boundary between the SBT and the HAO was clear with showing the HAO thickness of 10 nm which was as same as the designed as-deposited thickness. As P_{HAO} was raised, however, the HAO thickness seemed increasing with unclear boundary between the SBT and the HAO. The IL also grew thick as the P_{HAO} was raised. As shown in Fig. 2.19, stable I_d retentions until at least 2×10^5 s were indicated for all the FeFETs made by P_{HAO} ranged from 13 to 158 Pa in spite of the thick IL and the rough HAO observed at $P_{HAO} > 40$ Pa as shown in Fig. 2.18. The I_d retentions were measured by the same way discussed in Sect. 2.2.3. The V_P, V_E and V_{hold} we used for investigating the I_d-retentions were described in Fig. 2.19. Thanks to the thick SBT, all the FeFETs even at $P_{HAO} > 40$ Pa seemed to have stable retentions despite the thick-grown HAO with rough morphology suggested in Fig. 2.18. However, $P_{HAO} \ll 40$ Pa during the PLD deposition would be appropriate for suppressing total EOT of the HAO and IL.

2.5 Nitriding and Oxinitriding Si of MFIS FeFET

2.5.1 *Direct Nitriding Si for Large Memory Window of FeFET*

As mentioned in Sect. 2.3, we investigated EOT reduction of the I-and-IL layers. In this study, for the purpose of increasing the ε_{IL}, thin silicon nitride (Si–N) was grown on the Si surface in advance before depositing the MFI stack [29]. Pt/SBT/HfO_2/Si-N/*p*-Si FeFETs were prepared and characterized. A rapid-thermal-nitridation (RTN) machine was custom-designed. Si–N was formed on the Si by lamp-annealing in NH_3 ambient. All the initial Si substrates were transferred into vacuum immediately after sacrificial SiO_2 layers on the Si surfaces were removed by BHF. Fabrication process except for introducing the RTN was the same as described in Sect. 2.2.1 except for introducing the RTN. The Si-N layers were formed on the Si in NH_3 at temperatures T_{RTN} ranged from 800 to 1190 °C. T_{RTN} dependence of the Si–N thickness was estimated by investigating cross-sectional STEM pictures of Si–N grown on Si at T_{RTN} = 800, 1020 and 1190 °C as shown in Fig. 2.20a–d. The T_{RTN} was calibrated in advance using a thermocouple connected on a Si wafer. The ambient NH_3 pressure during the RTN was fixed at 532 Pa. Times for increasing, keeping and decreasing the RTN temperatures were controlled as 50, 10 and 30 s below 400 °C, respectively. Finally the Pt/SBT/HfO_2 stacks were deposited on the Si–N/Si by the same process as introduced in Sect. 2.2.1. Thicknesses were 200 nm for the Pt, 450 nm for the SBT and 6 nm for the HfO_2. The gate areas were L = 10 μm and W = 200 μm formed by photolithography and Ar^+ milling. Reference FeFETs of Pt/SBT/HfO_2/Si were also prepared by the conventional process without using the RTN. In the reference FeFETs, thicknesses of the Pt, SBT and HfO_2 were designed as the same as those in the RTN-processed Pt/SBT/HfO_2/Si–N/Si FeFETs.

Figure 2.21a–f show I_d–V_g hysteresis curves of the Pt/SBT/HfO_2/SiN/Si FeFETs. The Si–N layers were grown at T_{RTN} = 880, 940, 1000, 1020, 1080 and 1160 °C. All the curves were drawn in counterclockwise directions. The T_{RTN} very much affected static memory windows V_w. The memory windows V_W at

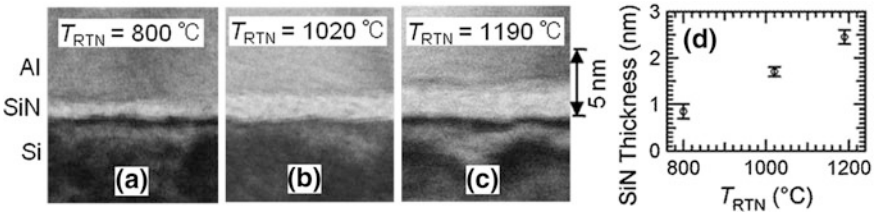

Fig. 2.20 Cross-sectional STEM pictures of Si–N/Si reference samples. The Si–N was grown on Si at **a** T_{RTN} = 800 °C, **b** 1020 °C and **c** 1190 °C. **d** T_{RTN} dependence of the Si–N thickness. Al was deposited for clear observations. Modified from [29]

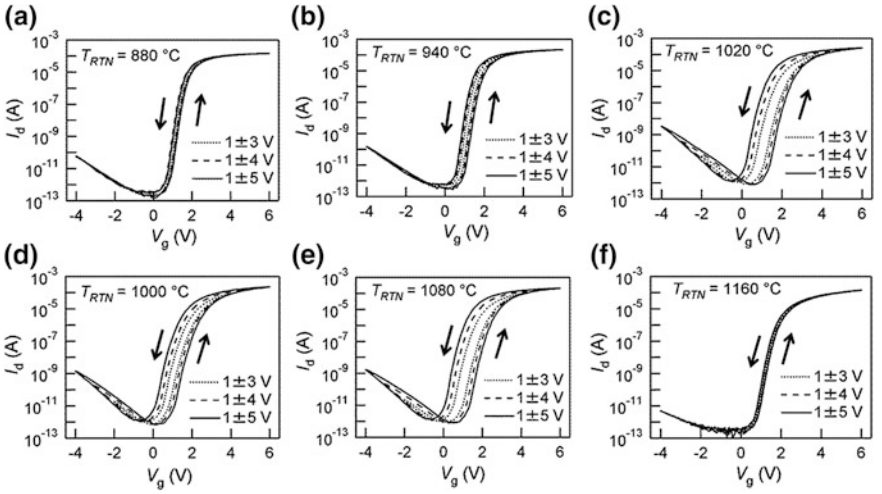

Fig. 2.21 I_d–V_g curves of Pt/SBT/HfO_2/Si–N/Si FeFETs in which the Si–N layers were prepared by RTN at various T_{RTN} of **a** 880 °C, **b** 940 °C, **c** 1000 °C, **d** 10,200 °C, **e** 1080 °C and **f** 1160 °C. Thicknesses were 200 nm Pt, 450 nm SBT and 6 nm HfO_2. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [29]

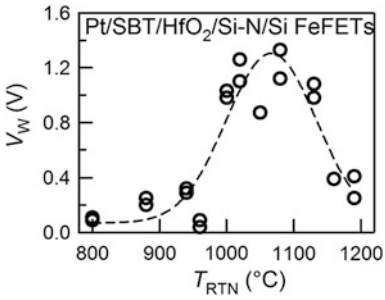

Fig. 2.22 T_{RTN} dependent V_w extracted from I_d–V_g hysteresis curves of Pt/SBT/HfO_2/Si–N/Si FeFETs. Thicknesses were 200 nm Pt, 450 nm SBT and 6 nm HfO_2. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [29]

V_g = 1 ± 5 V were extracted from the I_d–V_g of the FeFETs at various T_{RTN} and plotted in Fig. 2.22. The T_{RTN} dependent V_w showed a peak at the T_{RTN} ranged from 1020 to 1130 °C. The maximum V_w at V_g = 1 ± 5 V was V_w = 1.36 V when T_{RTN} = 1080 °C. It was about 10 % larger than of 1.24 V which was the averaged V_w of 16 reference Pt/SBT/HfO_2/Si FeFETs measured at V_g = 1 ± 5 V. In other words, introducing the RTN into the FeFET process increased the V_w by 10 %. The Pt/SBT/HfO_2/SiN/Si FeFET at T_{RTN} = 1080 °C showed stable on- and off-state I_d retained until at least 1.7×10^5 s or 2 days each as shown in Fig. 2.23. The I_d retentions were measured by the same way discussed in Sect. 2.2.3. The writing voltages were V_P = 5.5 V for the on state and V_E = −4.5 V for the off state. The I_d retention was measured with keeping $V_g = V_{hold}$ = 1.3 V, V_d = 0.1 V and $V_s = V_{sub}$ = 0 V.

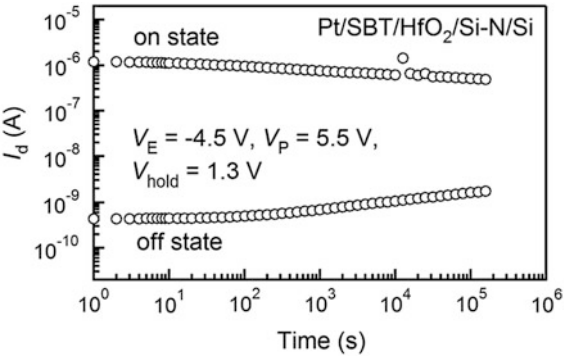

Fig. 2.23 T_{RTN} dependent V_w extracted from I_d–V_g hystereses of Pt/SBT/HfO_2/Si–N/Si FeFETs. Thicknesses were 200 nm Pt, 450 nm SBT and 6 nm HfO_2. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [29]

We investigated cross-sectional TEM to know the effect of the RTN process on the IL thickness. The cross-sectional TEM images indicated the same physical thickness of 3.5 nm for the two IL layers: one in the Pt/SBT/HfO_2/SiN/Si at T_{RTN} = 1020 °C and the other in the reference Pt/SBT/HfO_2/Si without using the RTN [29]. The initial Si–N thickness of 1.7 nm at T_{RTN} = 1020 °C was estimated as indicated in Fig. 2.20d. As shown in Fig. 2.24, backside SIMS analysis showed the element N had an intensity peak at the IL depth. The IL also included oxygen. The reason of the O inclusion in the IL was that the FeFET underwent the 800 °C annealing in O_2 for the SBT poly-crystallization. Judging from the cross-sectional TEM and the backside SIMS studies, the RTN process did not change the IL thickness but increase the ε_{IL} due to the nitrogen inclusion.

Gate leakage currents of the Pt/SBT/HfO_2/SiN/Si FeFETs at various T_{RTN} were also measured as shown in Fig. 2.25. Generally small I_g values were obtained at V_g = ±5 V. In detail, the FeFETs at around T_{RTN} = 800 and 1190 °C showed relatively low I_g. The small I_gs were due to abnormally thick IL of about 30 nm confirmed by cross-sectional STEM studies [29]. The STEM pictures also showed

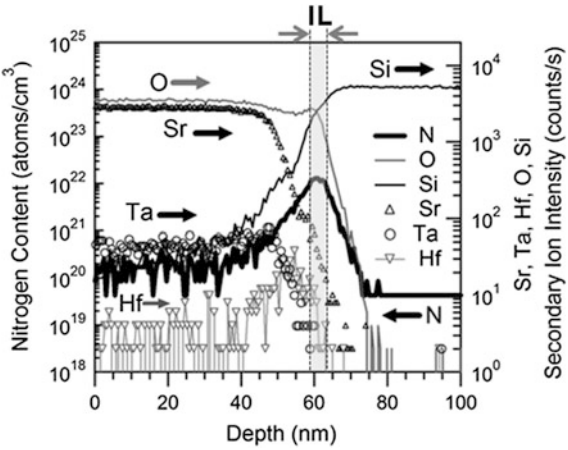

Fig. 2.24 Backside SIMS profile of a Pt/SBT/HfO_2/SiN/Si FeFET in which the Si–N grown at T_{RTN} = 1080 °C. Signal of Bi was less than the detection limit. Modified from [29]

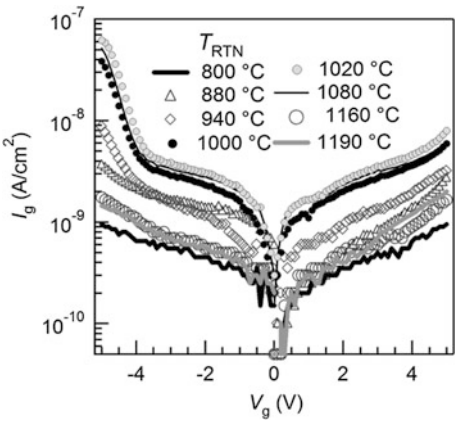

Fig. 2.25 Gate leakage currents of Pt/SBT/HfO_2/Si–N/Si FeFETs at various T_{RTN} ranged from 800 to 1190 °C. Modified from [29]

jagged boundaries between the IL and the Si of the FeFETs at T_{RTN} = 800 and 1190 °C. The Si surfaces might be irregularly eroded by the RTN and the subsequent poly-crystallization annealing for SBT at 800 °C. Figure 2.21a, f also supported that the very thick IL layers much reduced the V_w of the FeFETs at T_{RTN} = 880 and 1160 °C. Therefore the optimum T_{RTN} was around 1080 °C. The other T_{RTN} far from the optimum resulted in thick IL caused by irregular Si erosions.

2.5.2 *Oxinitriding Si for Improving the Si Interface of FeFET*

In Sect. 2.5.1, we introduced the RTN as a process to prepare Pt/SBT/HfO_2/Si-N/Si FeFETs which had larger V_w than reference Pt/SBT/HfO_2/Si FeFETs. On the other hand, however, subthreshold-voltage swing of $S = \ln 10 \cdot dV_g/d(\ln I_d)$ [24] was increased by the RTN. The reference Pt/SBT/HfO_2/Si FeFET usually had about S = 100 mV/decade while the Pt/SBT/HfO_2/Si-N/Si FeFET at T_{RTN} = 1080 °C showed S = 173 mV/decade. The large S might suggest an increase of Si surface-state density [24] caused by the direct nitriding the Si. In this work, we prepared and compared four kinds of FeFETs which had differently treated Si substrates such as reference-Si, Si-N/Si, SiO_2/Si and Si-O-N/Si [30].

The four kinds of substrates were prepared by the process using the RTN and rapid thermal oxidation (RTO) as follows. In every case, the initial Si substrate was transferred into vacuum immediately after sacrificial SiO_2 layer on the Si surface was removed by BHF. First, one out of the four which was named as the reference Si directly proceeded to the HfO_2 deposition. The reference Si underwent neither RTN nor RTO. Second, the Si–N/Si was prepared by RTN of the Si in 532 Pa NH_3 at T_{RTN} = 1080 °C. Third, the SiO_2/Si was made by RTO of the Si in 532 Pa O_2 at

the RTO temperature T_{RTO} = 1000 °C. Fourth, the Si–O–N/Si was prepared by a two-step heating, first by the RTO of the Si in 532 Pa O_2 at a fixed T_{RTO} = 1000 °C, and second by the RTN in 532 Pa NH_3 at various T_{RTN} ranged from 920 to 1150 °C. After the first RTO, the substrate for the Si–O–N/Si was once cooled below 400 °C and held in the process chamber during exchanging the ambient gas from O_2 to NH_3 via vacuum. In both the RTN and the RTO, the temperature was increased in 50 s to the target value, kept for 10 s at the target and decreased in 30 s below 400 °C. On the four kinds of substrates, Pt/SBT/HfO_2 stacks were commonly deposited by the same way as described in Sect. 2.2.1. Thicknesses were 200 nm for the Pt, 450 nm for the SBT and 6 nm for the HfO_2. The gate area sizes were L = 10 μm and W = 200 μm or W = 100 μm which were formed by photolithography and Ar^+ milling.

We optimized the T_{RTN} in preparing the Si–O–N/Si for maximizing V_w and minimizing S of the I_d–V_g curves. Figure 2.26 shows T_{RTN} dependences of V_w extracted from the I_d–V_g curves of the Pt/SBT/HfO_2/Si–O–N/Si FeFETs. The I_d–V_g curves were measured at V_g = 1 ± 3 V, 1 ± 4 V and 1 ± 5 V. The V_w had a broad peak at around T_{RTN} = 1050 °C as shown in Fig. 2.27. The largest V_w at V_g = 1 ± 4 V was V_w = 1.02 V. The S values of the I_d–V_d curves at V_g = 1 ± 4 V were plotted in Fig. 2.28. The S was the smallest S = 100 mV/decade around T_{RTN} = 1020 °C. Therefore in this work, T_{RTN} = 1050 °C was determined as the

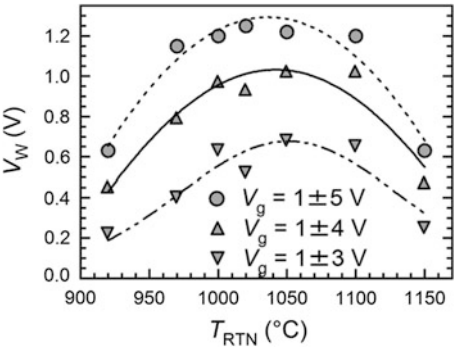

Fig. 2.26 T_{RTN} dependences of V_w extracted from the I_d–V_g curves of the Pt/SBT/HfO_2/Si–O–N/Si FeFETs measured at V_g = 1 ± 3 V, 1 ± 4 V and 1 ± 5 V. Modified from [30]

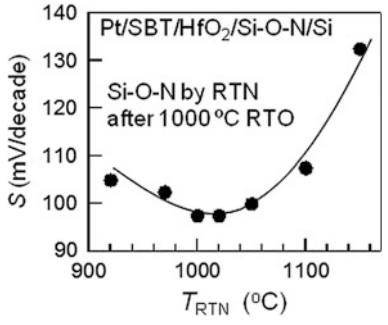

Fig. 2.27 T_{RTN} dependences of S extracted from the I_d–V_g curves of the Pt/SBT/HfO_2/Si–O–N/Si FeFETs measured at V_g = 1 ± 4 V. Modified from [30]

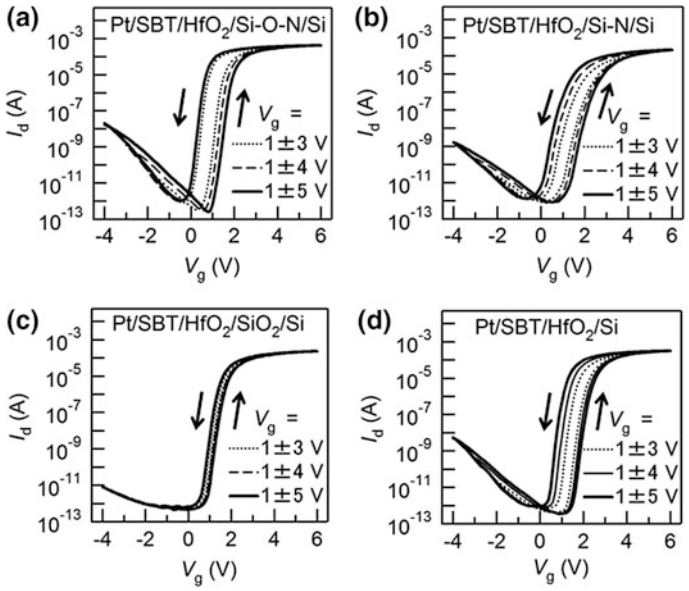

Fig. 2.28 I_d–V_g curves of FeFETs having the MFIS gate stacks such as **a** Pt/SBT/HfO_2/Si–O–N/Si, **b** Pt/SBT/HfO_2/Si–N/Si FeFETs, **c** Pt/SBT/HfO_2/SiO_2/Si and **d** Pt/SBT/HfO_2/(IL)/Si. Thicknesses were 200 nm Pt, 450 nm SBT and 6 nm HfO_2. The gate area sizes were L = 10 μm and W = 200 μm. Modified from [30]

best for obtaining the largest V_w and the smallest S of Pt/SBT/HfO_2/Si-O-N/Si FeFETs.

Static I_d–V_g curves were measured and compared among the four kinds of FeFETs having the following gate stacks: reference-Pt/SBT/HfO_2/Si, Pt/SBT/HfO_2/Si–N/Si, Pt/SBT/HfO_2/SiO_2/Si and Pt/SBT/HfO_2/Si–O–N/Si. As shown in Fig. 2.28, only the Pt/SBT/HfO_2/SiO_2/Si FeFET showed very small V_w among the four FeFETs. The small V_w suggested that the SiO_2 intentionally grown by the RTO induced the further thick SiO_2 grown on the Si finally. Particularly small I_g of the Pt/SBT/HfO_2/SiO_2/Si FeFET also implied the thick SiO_2 in the FeFET [30]. With regard to the S value, the Pt/SBT/HfO_2/Si–O–N/Si FeFET showed S = 100 mV/decade which was much smaller than S = 173 mV/decade of the Pt/SBT/HfO_2/Si–N/Si FeFET. The two-step Si annealing by first RTO and then RTN demonstrated in this study was found to be effective for preserving the good Si interface.

The Pt/SBT/HfO_2/Si–O–N/Si FeFET tended to show a large V_w especially at small V_g scan. As indicated in Fig. 2.28a, the FeFET had V_w = 0.64 V at V_g = 1 ± 3 V, which was the largest among the four FeFETs. The other three FeFETs in Fig. 2.28 showed (b) V_w = 0.51 V, (c) V_w = 0.09 V and (d) V_w = 0.42 V, at V_g = 1 ± 3 V. The large V_w at the small V_g scan as shown in

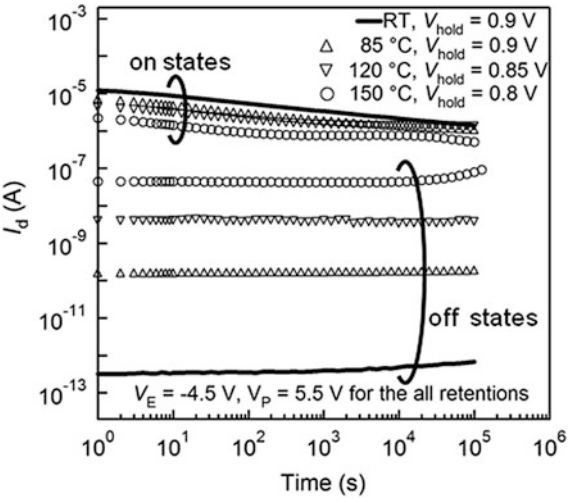

Fig. 2.29 I_d retentions of a Pt/SBT/HfO_2/Si–O–N/Si FeFET measured at room temperature, 85, 120 and 150 °C. The FeFET underwent T_{RTN} = 1050 °C. Thicknesses were 200 nm Pt, 450 nm SBT and 6 nm HfO_2. The gate area sizes were L = 10 μm and W = 100 μm. Modified from [30]. Unpublished data were added

Fig. 2.28a suggested that the Si–O–N reduced the EOT of the IL and relatively increased V_F across the SBT.

I_d retentions of the Pt/SBT/HfO_2/Si–O–N/Si FeFET were measured by the same way described in Sect. 2.2.3. The V_P, V_E and V_{hold} were described in Fig. 2.29. The retentions were measured at room temperature (RT), 85, 120 and 150 °C. The gate area sizes were L = 10 μm and W = 100 μm. The I_d retentions at the all temperatures remained stable until at least 1.0×10^5 s. As a conclusion of the section, forming the Si–O–N at the optimum T_{RTO} and T_{RTN} indicated a good potential to produce high quality FeFETs. By introducing the Si–O–N into the FeFET fabrication process, the operational voltages would be decreased with the S values kept small.

2.6 Using CSBT Instead of SBT in FeFET

We introduced the works for decreasing the I layer EOT in Sect. 2.4 and for decreasing the IL layer EOT in Sect. 2.5. In addition to the studies, we modified the F material for directly increasing the V_W of the FeFET as introduced in this section. We focused on $Ca_ySr_{1-y}Bi_2Ta_2O_9$ (CSBT(y)) among ferroelectric materials of bismuth-layered perovskite in expectation of the high-endurance nature as well as the $SrBi_2Ta_2O_9$ (SBT). Since some reports of CSBT indicated that MFM capacitors using the CSBT had larger coercive field (E_c) than the SBT [31–33], we began to investigate Pt/CSBT/HAO/Si FeFETs [34].

We fabricated and characterized Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs for demonstrating a larger V_w than the conventional Pt/SBT/HAO(x = 0.75)/Si FeFETs. We had a strong motivation to change the F material from the SBT to the

CSBT because we recently set the F thickness $d_F \leqq 200$ nm which was less than half of our early-stage $d_F = 400$ nm in 2002 [9–11]. The purpose of the reducing d_F was enabling the etching of the high-aspect gate stacks for prospective downsizing FeFETs [7, 8]. We had three expectations in applying the CSBT to the FeFETs. One was that the CSBT would have a similar nature to the SBT and would not show significant material diffusion with Si across the HAO. Second was that MFIS FeFETs using the CSBT might show a larger V_w than that using the SBT because a larger E_c of the CSBT than that of the SBT was reported in major *P-E* loops of the MFM capacitors [31–33]. The last was that the crystallization temperature of the CSBT was expected to be lower than that of the SBT because good ferroelectric properties of $CaBi_2Ta_2O_9$ (CBT or CSBT($y = 1.0$)) capacitances were reported which were annealed at 700 and 750 °C [35].

In order to optimize the Ca composition ratio y and the annealing temperature, we prepared Pt/CSBT(y)/HAO($x = 0.75$)/Si FeFETs where the y was varied as $y = 0$, 0.1, 0.2, 0.5 and 1.0. Fabrication process was basically the same as described in 2.1 except for using a custom-designed large-area PLD [36], replacing the SBT with the CSBT(y), thinning the F to 200 nm, and searching for the best annealing temperature T_{an} for the CSBT(y) poly-crystallization. The HAO($x = 0.75$) was deposited by the PLD in 15 Pa N_2 at the substrate temperature 220 °C. A ceramic target of $(HfO_2)_{0.75}(Al_2O_3)_{0.25}$ was used. The CSBT(y) was deposited by the PLD in 7 Pa O_2 at 415 °C using Ca–Sr–Bi–Ta–O ceramic targets with the element ratio Ca:Sr:Bi:Ta = y:1 − y:3:2. All the FeFETs were annealed in 1 atm O_2 for 30 min at various T_{an} from 748 to 833 °C for the CSBT(y) poly-crystallization. Gate areas of all the FeFETs had a fixed length $L = 10$ μm and a various widths of $W = 200$, 150, 100, 80, 50, 40, 20 and 10 μm formed by photolithography and Ar^+ milling. Thicknesses were 200 nm for the Pt, 200 nm for the CSBT(y) and 7 nm for the HAO($x = 0.75$).

We prepared numerous FeFETs of Pt/CSBT(y)/HAO($x = 0.75$)/Si with $y = 0$, 0.1, 0.2, 0.5 and 1.0. Figure 2.30 show the T_{an} dependence of the V_w values which were extracted from static I_d–V_g curves measured the FeFETs at $V_g = 1 \pm 5$ V. In each V_w–T_{an} curve for y, the individual Pt/CSBT(y)/HAO($x = 0.75$)/Si FeFETs underwent annealing at various T_{an}. The FeFETs with $y = 0$ using the SBT had the maximum $V_w = 0.75$ V at $T_{an} = 813$ °C. The FeFETs with $y = 0.1$ had the maximum $V_w = 0.89$ V at $T_{an} = 800$ °C. Those with $y = 0.2$ had the maximum $V_w = 0.84$ V also at $T_{an} = 800$ °C. When $y = 1.0$ using the CBT, however, the FeFETs showed almost zero V_w which was unexpected results from the MFM studies using the CBT with large E_c [35, 37, 38]. This case is a good example that MFM could not fully predict the behaviors of the F in MFIS. As shown in Fig. 2.31a–c, cross-sectional TEM pictures indicated that IL thickness of the Pt/CSBT($y = 0.1$)/HAO($x = 0.75$)/Si FeFETs became thick as the T_{an} was raised from 748 to 833 °C. The interfaces between the IL and the HAO($x = 0.75$) seemed clear in the all Pt/CSBT($y = 0.1$)/HAO($x = 0.75$)/Si FeFETs prepared at $T_{an} = 748$, 788 and 833 °C. However, the Pt/CBT(or CSBT($y = 1.0$))/HAO($x = 0.75$)/Si FeFET showed about 7 nm-thick IL exhibiting no clear interface across the IL, HAO($x = 0.75$) and CBT as indicated in Fig. 2.31d. The Si surface of the

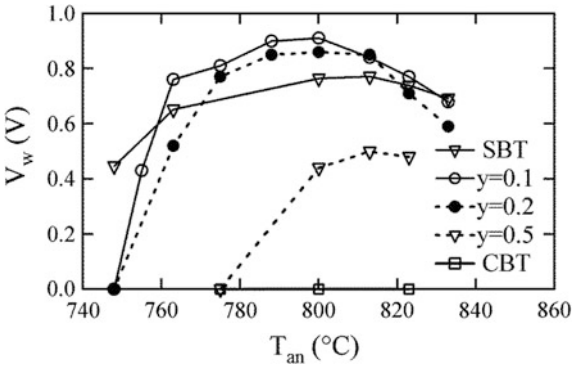

Fig. 2.30 Annealing-temperature dependence of static memory windows extracted from I_d–V_g curves of Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs. The Ca composition ratio y was varied as y = 0, 0.1, 0.2, 0.5 and 1.0. The CSBT(y = 1.0) was the CBT. The I_d–V_g curves were measured at V_g = 1 ± 5 V. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. The gate lengths were L = 10 μm. Modified from [34]

Pt/CBT/HAO(x = 0.75)/Si FeFET showed a wavy profile. The cross-sectional TEM study suggested that the pure CBT had material diffusions among the HAO (x = 0.75) and Si. Owing to the thick grown IL, the gate-leakage current of the Pt/CSBT(y = 1.0)/HAO(x = 0.75)/Si FeFET were as small as about 1/10 of the other FeFETs with y = 0, 0.1, 0.2 and 0.5 [34].

Electrical properties of Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs with y = 0, 0.1 and 0.2 were investigated. They were (1) I_d retentions, (2) endurances, and (3) pulse memory windows measured by a system updated from our conventional one described in Sect. 2.2. The three kinds of FeFETs with y = 0, 0.1 and 0.2 were annealed at each optimum T_{an} for maximizing V_w which were T_{an} = 813 °C for y = 0, and T_{an} = 800 °C for both y = 0.1 and 0.2 as indicated in Fig. 2.30.

1. I_d retentions of the FeFETs with y = 0, 0.1 and 0.2 were measured using a semiconductor parameter analyzer controlled by a Labview program. All of the on-and off-state I_d–t curves were stable for at least 4×10^5 s as shown in Fig. 2.32. The hold gate voltage values were V_{hold} = 1.1, 1.2 and 1.3 V for the FeFETs with y = 0, 0.1 and 0.2, respectively. The measurement procedure was basically the same as described in Sect. 2.2.3 except for fixing the writing or poling time at t_{pls} = 0.1 s. For investigating the on-state I_d–t, a programming V_g pulse was applied first. During the programming V_g pulse, we fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub}$ = 0 V. In the programming pulse, the V_g began from 0 V, raised to V_P = 6 V and kept for t_{pls} = 0.1 s, then finally stepped down to V_{hold}. Then on-state I_d retentions started to be measured till 4×10^5 s. At the time of every marker in the on-state I_d–t curve in Fig. 2.32, V_d was raised from 0 to 0.1 V and the on-state I_d was read out with keeping $V_g = V_{hold}$ and $V_s = V_{sub}$ = 0 V. In the other time, the FeFETs were held with $V_g = V_{hold}$ and $V_d = V_s = V_{sub}$ = 0 V. Similarly, for investigating the off-state I_d–t, erasing a V_g

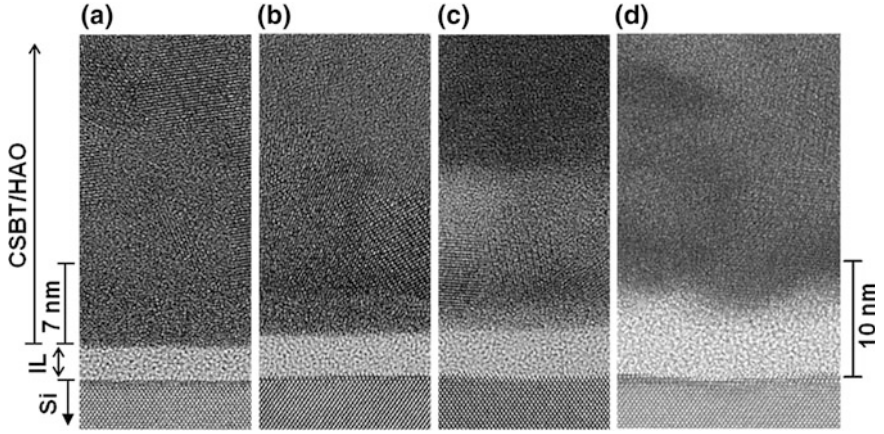

Fig. 2.31 Cross-sectional TEM pictures of Pt/CSBT(y = 0.1)/HAO(x = 0.75)/Si FeFETs prepared by annealing at **a** T_{an} = 748 °C, **b** T_{an} = 788 °C and **c** T_{an} = 833 °C. **d** Cross-sectional TEM picture of Pt/CSBT(y = 1.0)/HAO(x = 0.75)/Si FeFET prepared by annealing at T_{an} = 800 °C. The CSBT(y = 1.0) was the CBT. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. Modified from [34]

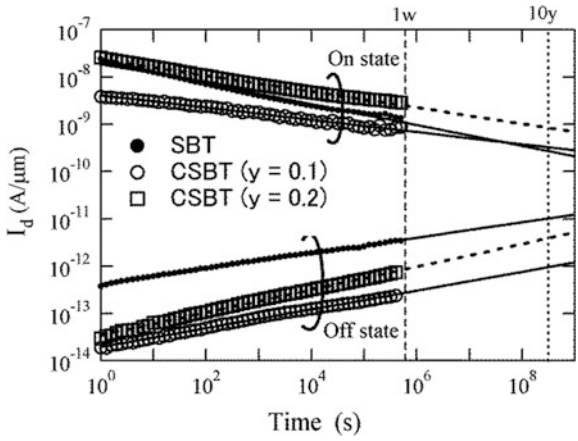

Fig. 2.32 I_d retentions of Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs with y = 0, 0.1 and 0.2. The FeFETs with y = 0, 0.1 and 0.2 were annealed at T_{an} = 813, 800 and 800 °C, respectively. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. The gate lengths were L = 10 μm. Modified from [34]

pulse was applied first. During the erasing V_g pulse, we fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub}$ = 0 V. In the erasing pulse, the V_g began from 0 V, reduced to V_E = −4 V and kept for t_{pls} = 0.1 s, then finally stepped down to V_{hold}. Then off-state I_d retentions started to be measured till 4×10^5 s. At the time of every marker in the off-state I_d–t curve in Fig. 2.32, V_d was raised from 0 to 0.1 V and the off-state I_d was read out with keeping $V_g = V_{hold}$ and $V_s = V_{sub}$ = 0 V. In the other time, the FeFETs were held with $V_g = V_{hold}$ and $V_d = V_s = V_{sub}$ = 0 V.

2. The V_{th} endurances of the FeFETs with y = 0, 0.1 and 0.2 were measured using a semiconductor parameter analyzer, a pulse generator and a dc voltage source

which were conducted by a Labview program. As shown in Fig. 2.33a–d, the FeFETs with $y = 0$, 0.1 and 0.2 showed no significant V_{th} shifts until at least 10^8 endurance cycles of 20 μs period 1 ± 5 V. The measurement procedure was basically the same as described in Sect. 2.2.4 except for reading not I_d but V_{th} values from the static I_d–V_g curves which were drawn every time after the accumulated numbers of endurance cycles were counted to 10^n with the n incremented from 0 to 8. In this work, endurance pulses were 20 μs period V_g pulses of alternately applied $V_P = 6$ V and $V_E = -4$ V which were outputted from a pulse generator. During the endurance pulses were applied, we fixed V_d, V_s and V_{sub} at $V_d = V_s = V_{sub} = 0$ V. After the accumulated numbers of endurance cycles were counted to 10^n at every marker in Fig. 2.33d, the pulse application was interrupted and V_d was raised from 0 to 0.1 V. Then a static I_d–V_g curve was drawn by scanning V_g from −4 to 6 V and back to −4 V (or $V_g = 1 \pm 5$ V), with keeping $V_s = V_{sub} = 0$ V. The I_d was normalized by the gate width W and was expressed in units of A/μm. Two V_{th} values corresponding to the programmed and erased states were extracted from the I_d–V_g loop where the V_{th} values were defined as the gate voltages which gave $I_d = 10^{-8}$ A/μm in the I_d–V_g loop. After recording the static I_d–V_g curve

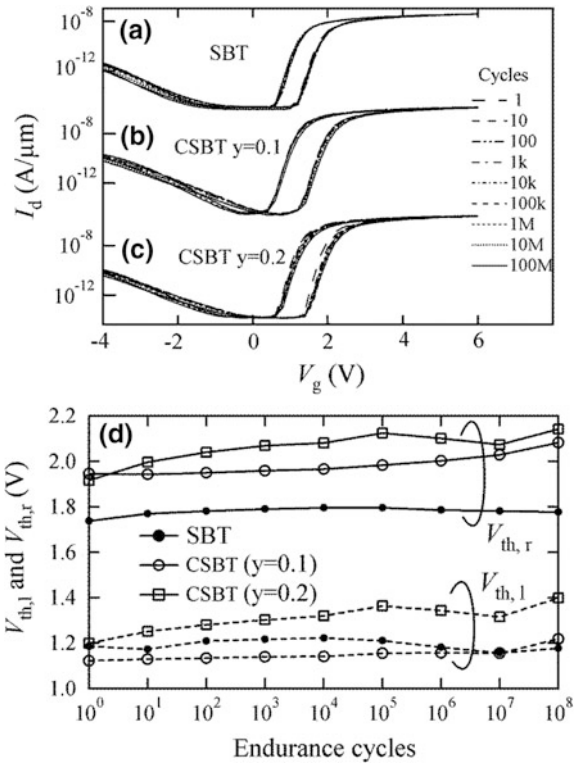

Fig. 2.33 V_{th} endurances of Pt/CSBT(y)/HAO($x = 0.75$)/Si FeFETs with $y = 0$, 0.1 and 0.2. The FeFETs with $y = 0$, 0.1 and 0.2 were annealed at $T_{an} = 813$, 800 and 800 °C, respectively. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. The gate lengths were $L = 10$ μm. Modified from [34]

corresponding to the 10^n cycles, V_d was reduced back to 0 V. Then the V_g endurance-pulse application was resumed.

3. The pulse memory windows of the FeFETs with $y = 0$, 0.1 and 0.2 were investigated. The pulse-memory-window measurement has essentially the same meaning as the writing speed measurement as discussed in Sect. 2.2.5. In order to discuss the practical ability of an FeFET, the memory window should be investigated by writing with a pulsed V_g not a static V_g. The pulse memory window was defined as a V_{th} difference (V_{plsW}) of $V_{plsW} = V_{thE} - V_{thP}$. The V_{thE} and V_{thP} were the V_{th} values of an FeFET at the erased and programmed states. The V_{thE} and V_{thP} were defined as the V_g values at $I_d/W = 10^{-8}$ A/μm. The V_{thE} was the V_{th} after a negative V_g pulse was applied for erasing the FeFET. The negative V_g pulse had a height V_E and a width t_{pls}. Similarly, The V_{thP} was the V_{th} after a positive V_g pulse was applied for programming the FeFET. The positive V_g pulse had a height V_P and the width t_{pls}. The measurement procedure was indicated in Fig. 2.34. A pulse generator and a dc voltage source were used for outputting the V_g wave in Fig. 2.34. The role of the dc voltage source was to give a trigger signal to the pulse generator. I_d values in read operation were measured by a semiconductor parameter analyzer. All the measurement systems were conducted by a Labview program. The V_{thE} and V_{thP} were measured in a cycle in Fig. 2.34 with fixing (V_E, V_P) and at increasing t_{pls} cycle by cycle.

For erasing the FeFET, a single negative V_g pulse was applied which started from a base V_{base}, reduced to V_E kept for t_{pls} and stepped back to the V_{base}. During the negative V_g pulse application, we fixed $V_d = V_s = V_{sub} = 0$ V. After the negative V_g pulse application, the V_d was raised to $V_d = 0.1$ V for reading. Then I_d was measured by static scanning V_g from one end of the read voltage (V_{readA}) to the other end (V_{readB}) with keeping $V_s = V_{sub} = 0$ V. The V_{thE} was determined as the V_g at $I_d = 10^{-8}$ A/μm in the I_d–V_g curve. In this work, we set as $V_{base} = 1.2$ V for the FeFETs with $y = 0.1$ and $y = 0$. The V_{base} was $V_{base} = 1.5$ V for the FeFET with $y = 0.2$. We used $V_{readA} = 2$ V and $V_{readB} = 1$ V.

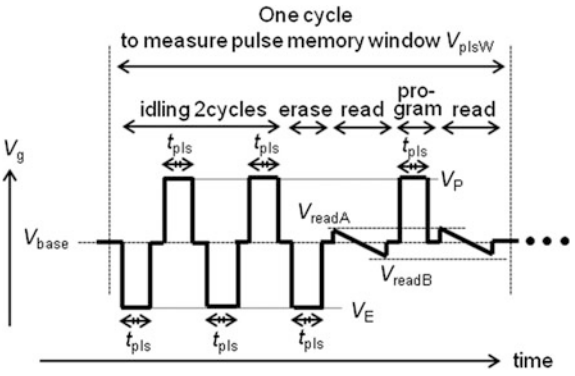

Fig. 2.34 Schematic view of the V_g wave form used for investigating V_{plsW} of FeFETs. The V_{plsW} was measured at t_{pls} elevated with (V_E, V_P) fixed

For programming the FeFET, a single positive V_g pulse was applied which started from the V_{base}, raised to V_P kept for t_{pls} and stepped back to the V_{base}. During the positive V_g pulse application, we fixed $V_d = V_s = V_{sub} = 0$ V. After the positive V_g pulse application, the V_d was raised to $V_d = 0.1$ V for reading. Then I_d was measured by static scanning V_g from one end of the read voltage (V_{readA}) to the other end (V_{readB}) with keeping $V_s = V_{sub} = 0$ V. The V_{thP} was determined as the V_g at $I_d = 10^{-8}$ A/μm in the I_d–V_g curve. Note that the read V_g range from V_{readA} to V_{readB} was common to the read after the erase and the read after the program. The small range was selected so that the read operation did not significantly affect the V_{thP} and V_{thE}.

The V_{thE} and V_{thP} obtained at various height combinations (V_E, V_P) with increasing t_{pls} were shown in Fig. 2.35a–c for the individual FeFETs with $y = 0$, 0.1 and 0.2. In all of Fig. 2.35a–c, the broken lines were for (V_E, V_P) = (−6, 8 V), the dotted lines were for (V_E, V_P) = (−5, 7 V) and the solid lines were for (V_E, V_P) = (−4, 6 V). In each (V_E, V_P), the V_{th} difference of $V_{thE} - V_{thP}$ became large as the pulse width t_{pls} was increased. At every t_{pls}, the larger the $V_P - V_E$ was, the wider the $V_{thE} - V_{thP}$ was. The increasing tendency of the $V_{thE} - V_{thP}$ as the writing-V_g-pulse width and amplitude indicated unsaturated-ferroelectric polarization in the FeFET as we have discussed since the early stage [17].

For all the FeFETs with $y = 0$, 0.1 and 0.2, pulse memory windows $V_{plsW} = V_{thE} - V_{thP}$ were plotted as a function of t_{pls} at every (V_E, V_P) in Fig. 2.36. As shown in Fig. 2.36, the FeFETs with $y = 0.1$ and 0.2 tended to show larger pulse memory windows than the FeFET with $y = 0$ at a common t_{pls} in every

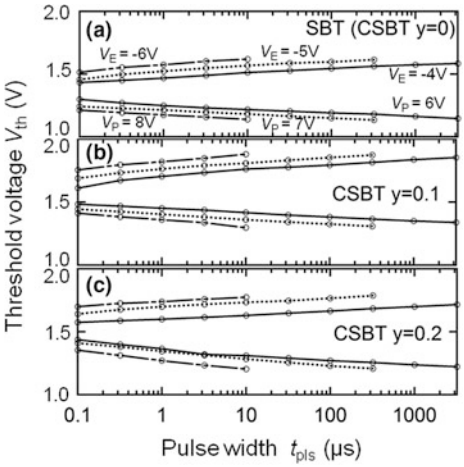

Fig. 2.35 Pulse width t_{pls} dependent V_{thE} and V_{thP} of three kinds of Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs with **a** $y = 0$, **b** $y = 0.1$ and **c** $y = 0.2$. The *broken lines* were for (V_E, V_P) = (−6, 8 V), the *dotted lines* were for (V_E, V_P) = (−5, 7 V) and the *solid lines* were for (V_E, V_P) = (−4, 6 V). The FeFETs with $y = 0$, 0.1 and 0.2 were annealed at T_{an} = 813, 800 and 800 °C, respectively. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. The gate lengths were $L = 10$ μm. Modified from [34]

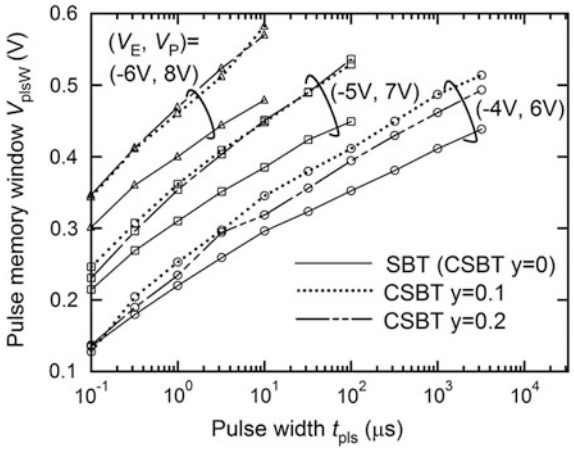

Fig. 2.36 Pulse width t_{pls} dependences of the pulse memory windows $V_{plsW} = V_{thE} - V_{thP}$ at (V_E, V_P) = (−4, 6 V), (−5, 7 V) and (−6, 8 V). The V_{plsW} versus t_{pls} were extracted from the $V_{thE} - t_{pls}$ and $V_{thP} - t_{pls}$ curves in Fig. 2.35a–c. The *solid lines* were for y = 0, the *dotted lines* were for y = 0.1 and the *broken lines* were for y = 0.2. The FeFETs with y = 0, 0.1 and 0.2 were annealed at T_{an} = 813, 800 and 800 °C, respectively. Thicknesses were 200 nm Pt, 200 nm SBT and 7 nm HAO. The gate lengths were L = 10 μm. Modified from [34]

(V_E, V_P). From the other view point, the t_{pls} of the FeFETs with y = 0.1 and 0.2 were shorter than that of the FeFET with y = 0 to show the same pulse memory window. For example when (V_E, V_P) = (−5, 7 V) and t_{pls} = 1 μs were fixed, the reference FeFET with y = 0 had V_{plsW} = 0.31 V while the FeFET with y = 0.1, 0.2 showed V_{plsW} = 0.35 V which was 13 % larger V_{plsW} than the reference FeFET. On focusing on the t_{pls} necessary to reach V_{plsW} = 0.4 V at (V_E, V_P) = (−5, 7 V), t_{pls} = 3 μs was for the FeFET with y = 0.2 and t_{pls} = 15 μs was for the reference FeFET with y = 0.

In conclusion of this section, the Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs with y = 0.1 and 0.2 showed good I_d-retentions and endurances equivalent to those of the reference FeFET with y = 0. The Pt/CSBT(y)/HAO(x = 0.75)/Si FeFETs with y = 0.1 and 0.2 had larger static memory windows and pulse memory windows than the reference FeFET with y = 0. Therefore replacing the SBT with the CSBT will be a good solution to preserve the MFIS FeFET qualities with reducing the F thickness. Reducing the F thickness lead to decreasing the gate-stack aspect ratio which was a strong requirement for downsizing the FeFETs.

2.7 Summary

Studies of Pt/CSBT(y)/HAO(x)/Si MFIS FeFETs were reviewed as follows.

In Sect. 2.2, the first Pt/SBT/HAO(x = 0.75)/Si FeFET was characterized by measuring 10^6 s-long retention, 10^{12} cycles-high endurance and 4×10^{-8} s writing speed. Detailed methods of the measurements were also explained. I_d–V_g curves and I_d-retentions measured at most 85 °C were introduced using *p*-channel FeFETs.

In Sect. 2.3, requirements to the M, F, and I layers in MFIS were discussed. Especially, the requirements to the I layer were high-temperature-proof, thin-deposited high-*k* material with higher barriers than the F layer against electrons and holes. The good candidate was the HAO(*x*).

In Sect. 2.4, the optimum preparation conditions of the HAO(*x*) were investigated. For securing amorphous and small-leakage HAO(*x*), the preferable x was smaller than 0.95. We often used $x \geqq 0.75$ by expecting both the small leakage and large dielectric constant. The ambient gas kind O_2 and N_2 during the HAO ($x = 0.75$) deposition were compared. The Pt/SBT/HAO(N)/Si showed $V_w = 0.9$ V while the Pt/SBT/HAO(O)/Si showed $V_w = 0.3$ V at $V_g = \pm 6$ V. The IL thickness in the Pt/SBT/HAO(O)/Si was as thick as 7.4 nm because the HAO(O) did not work sufficiently as a material-diffusion barrier. We also introduced effects of increasing ambient N_2 pressure P_{HAO} during the HAO($x = 0.75$) deposition in Pt/SBT/HAO/*p*-Si. In order to keep a clear interface between the SBT and HAO, $P_{HAO} \ll 40$ Pa was suitable.

In Sect. 2.5, direct nitriding Si was introduced as the way to increase the memory window of Pt/SBT/HAO($x = 0.75$)/Si FeFET. The Pt/SBT/HAO ($x = 0.75$)/Si FeFET using the Si–N tended to show a large subthreshold-voltage swing *S*. Oxinitriding Si was demonstrated as an improved way to decrease the *S* value of the FeFET.

In Sect. 2.6, we changed the F material from the SBT to CSBT(*y*) for increasing the V_W of the FeFET. The Pt/CSBT($y = 0.1,\ 0.2$)/HAO($x = 0.75$)/Si FeFETs showed larger static-memory windows than the reference Pt/SBT/HAO($x = 0.75$)/Si FeFET. The Pt/CSBT($y = 0.1,\ 0.2$)/HAO/Si also showed 13 % larger pulse memory windows than the reference. The Pt/CSBT($y = 0.1, 0.2$)/HAO($x = 0.75$)/Si FeFETs showed 10^8 cycles-high endurances and at least 4×10^5 s-long retentions which were equivalent to the reference Pt/SBT/HAO($x = 0.75$)/Si FeFET.

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