

Chapter 2

Key Principles of Power Converters

This chapter explains how linear regulators and switching converters are adopted in power processing from the very basic principles of power circuits. The switching process is dealt with and switching losses, efficiency, and snubber circuits are introduced. The concepts of continuous conduction and discontinuous conduction modes are explained.

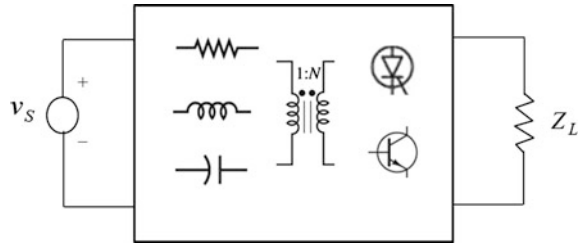
A converter, also quite often referred to as a ‘switching converter’ or ‘power converter’ to distinguish it from a signal converter, is composed of inductors (L), capacitors (C), resistors (R), transformers (T), and semiconductor switches (S), as shown in Fig. 2.1. It can be said that the purpose of a ‘modern’ converter is to convert and control power by semiconductor switches. Note that ‘old’ converters in the early 20th century were not made of semiconductor switches but rather electro-mechanical machines or electronic vacuum tube switches.

In this chapter, a few key principles for understanding the converter are provided from the very basic idea. Ideally, a converter

1. changes power without any power loss, i.e., power efficiency is 100 %,
2. takes zero response time with no transient overshoot, i.e., its operation is quite fast and stable,
3. has no harmonics and ripples,
4. is involved in no faults, i.e., it is maintenance free and has infinite lifetime,
5. has minimum size, weight, and cost,
6. operates in all-weather environments under harsh conditions.

Of course, there is no such ideal converter, and power electronic engineers are struggling to make converters close to it. More often, finding a suitable trade-off between the above mentioned six requirements is a practical issue that engineers encounter. More specifically, choosing the configuration of a converter and determining the parameters of circuit components, often called ‘design’, are major jobs for engineers.

Fig. 2.1 A converter is composed of LCR and TS in general



2.1 Evolution of Power Converters

2.1.1 Why Do We Need Power Control?

Let's see why we should control the power with a DC power circuit, as shown in Fig. 2.2. There are at least three cases where we need to control the power. First, the battery output voltage changes by aging, as shown in Fig. 2.2a. Many loads do not permit this voltage drop; then, we should have a countermeasure to address this problem. Second, the output voltage of a battery changes as the load current

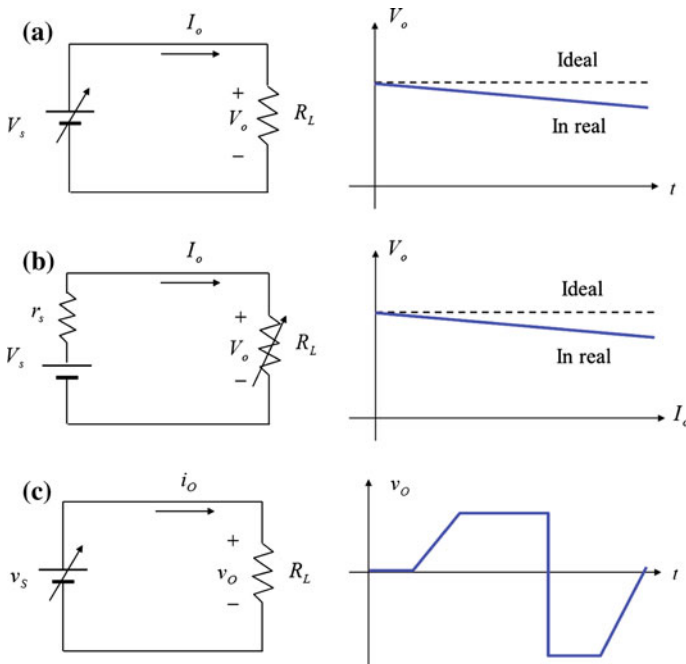


Fig. 2.2 The reasons why we need power control in a power system. **a** A battery voltage changes by aging. **b** The output voltage changes as the load current increases. **c** We want to vary the output as desired

increases, as shown in Fig. 2.2b. This voltage drop is inevitable due to the finite value of the internal resistance of the battery, which is of course not permitted for a voltage sensitive load. The third case is that we want to vary the output dynamically as desired, as shown in Fig. 2.2c. It is remarkable to see that the need for power control comes from the power source, load, and converter. This means that every component of a power system can be a source of problems that should be solved.

2.1.2 We Can Control the Power by a Time-Varying Resistor

Let's start with a very simple idea of controlling output power by a controllable variable resistor, as shown in Fig. 2.3. As the source voltage v_S fluctuates randomly, we need to control the resistor R_c so that the output voltage v_O can be regulated as desired. It is straightforwardly found that the DC (direct current) gain, often referred to as 'large signal gain', is as follows:

$$G_v \equiv \frac{v_O}{v_S} = \frac{R_L}{R_c + R_L}. \quad (2.1)$$

$R_c(t)$, which is now time-varying, can then be determined for given DC gain as follows:

$$R_c(t) = R_L \left(\frac{1}{G_v} - 1 \right) = R_L \left(\frac{v_S}{v_O} - 1 \right). \quad (2.2)$$

As identified from (2.2), v_O cannot be larger than v_S so far as $R_c(t)$ is non-negative, and the power control system involves inherent power loss in $R_c(t)$. Therefore, this type of converter can be applicable to voltage step-down conversion applications where power efficiency is not a serious problem.

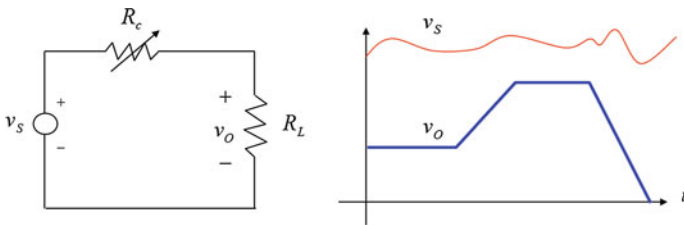


Fig. 2.3 An idea for controlling output power by a variable resistor

2.1.3 We Can Control the Power by a Power Transistor in Linear Mode

The ideal of controllable resistor can be implemented by using a transistor, as shown in Fig. 2.4. The output voltage can be determined by a simple equation, considering non-saturation conditions for the transistor, as follows:

$$v_O = v_Q - v_\gamma \quad \text{for} \quad v_S - v_O \geq v_\sigma \cong 0.2 \quad \therefore v_Q = v_O + v_\gamma \cong v_O + 0.7. \quad (2.3)$$

As identified from (2.3), the output voltage can be arbitrarily controlled under the restricted conditions of non-saturation. A very popular application is the linear regulator, where the output voltage is usually kept constant to a certain specified value, as shown in Fig. 2.4 as a dotted line. Feedback control is very often used in practice to achieve an accurate voltage regulation regardless of source voltage variation and load current change. Another application is the power amplifier, where the output voltage quickly follows the wanted voltage waveform, as shown in Fig. 2.4 as a bold line.

Over current protection for a small R_L , over voltage protection against high input voltage or output voltage due to inductive load characteristics, and over temperature protection for the power transistor are needed for practical applications. This is why we need a power control integrated circuit (IC) in power electronics.

Question 1

1. Determine the maximum amplitude of a sinusoidal output voltage of a power amplifier for a fixed V_s .
2. Calculate the power efficiency of the power amplifier for the maximum amplitude case of (1).

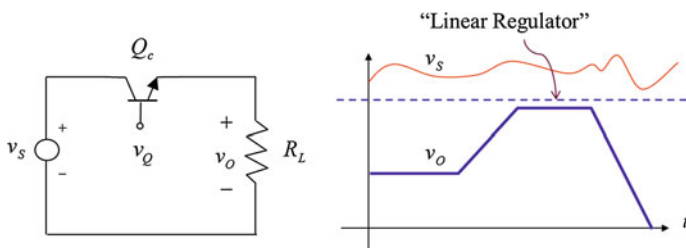


Fig. 2.4 An implementation example of the controllable resistor of Fig. 2.3

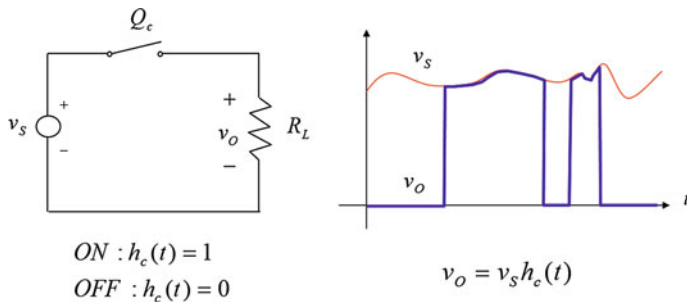


Fig. 2.5 An ideal power switch for controlling output power without any power loss

2.1.4 We Can Control the Power by a Power Transistor in Switching Mode

An innovative way of controlling output power without any power loss is to use an ideal power switch, as shown in Fig. 2.5. When the power switch is ON, then the voltage drop of the ideal power switch is zero. When the power switch is OFF, then the current of the ideal power switch is zero. Therefore, the power loss in the ideal switch becomes always zero, which results in 100 % power efficiency.

The idea of controlling power by an ideal power switch can be implemented by a power transistor, operating in switching mode, as shown in Fig. 2.6. Similar to the controllable resistor case, voltage step-down conversion is only possible and square wave type output voltage is obtained for this power switch method.

Furthermore, this switch mode power transistor is seldom used without proper measures in practice because of the leakage inductance, which exists for any power line of the order of 1 $\mu\text{H}/\text{m}$ for 1 nH/mm . For example, a 10 cm power line has 0.1 μH , which may destroy a power transistor of 1000 V voltage rating. One way of avoiding this unwanted high induced voltage from the leakage inductance is to use a power diode, as shown in Fig. 2.7. As soon as the ideal transistor is turned on or off, the ideal diode is turned off and on, which provides an alternative current path so that the current of the leakage inductor can be continuous. In this way, the

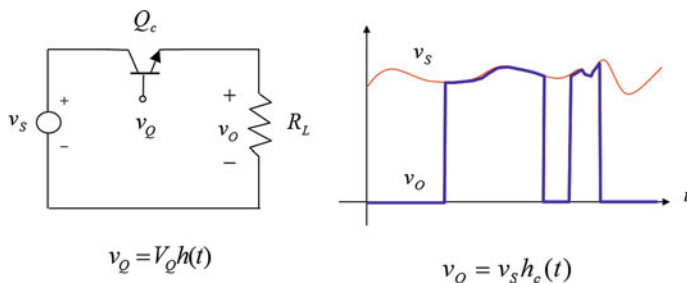


Fig. 2.6 Implementation of the ideal power switch of Fig. 2.5

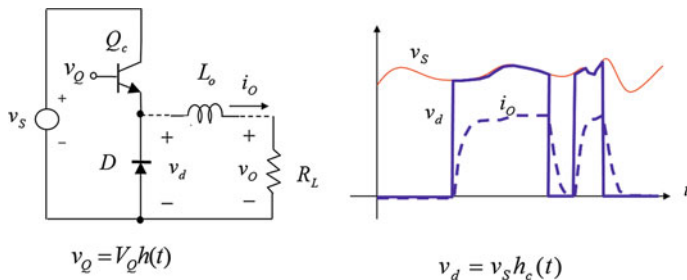


Fig. 2.7 A possible way of protecting the power transistor from the leakage inductance using a power diode

collector-emitter voltage stress of the transistor is safely constrained within the source voltage. The output current is accordingly determined by the leakage inductance and load, as depicted in Fig. 2.7.

The transistor-diode pair is referred to as a ‘switch cell’ because the switches do not operate separately but rather they operate like a system. Even though the switch mode transistor-diode pair is safely operating, this power circuit is not widely used except for a simple on/off control of power where large switching noise is not a problem in practice.

2.1.5 A Switching Converter with Input and Output Filters Is a Viable Solution

Instead of leakage inductance, a lumped inductor can be attached the switch cell. The switch cell with a filter can be called a basic ‘converter’, as shown in Fig. 2.8.

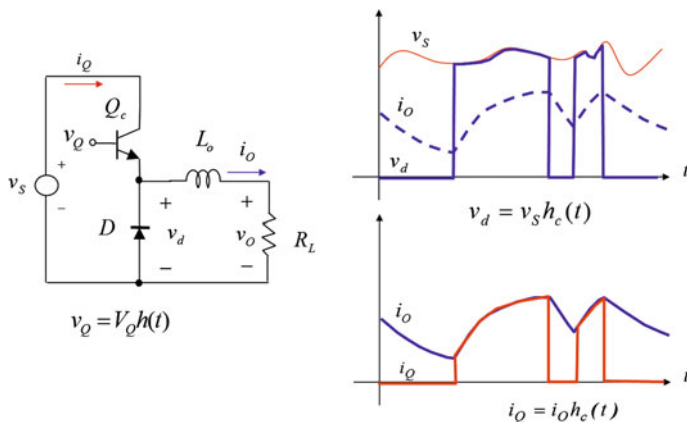


Fig. 2.8 A basic converter with an output inductor only

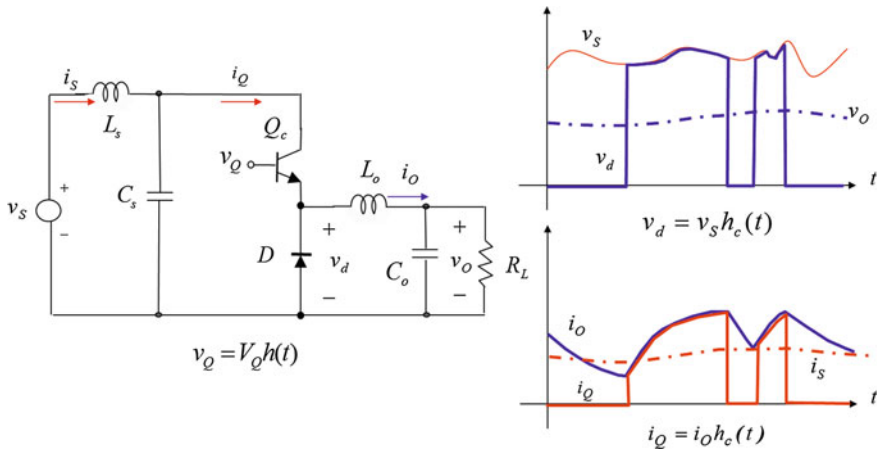


Fig. 2.9 A buck converter with input and output LC filters

Now, the output current can be continuous and the load voltage becomes smooth. One of the problems of this converter is that the input current i_Q contains large switching current, as shown in Fig. 2.8.

Therefore, we need to add an input filter to mitigate the switching harmonic current, and we need to strengthen the output filter as well, as shown in Fig. 2.9. The input and output LC filters eliminate the switching voltage and current generated from the switch cell. The step-down converter, as shown in Figs. 2.8 and 2.9, is called a buck converter when it is used in DC-DC power conversion, which is regarded as the most fundamental converter. Now we have smooth voltage and current waveforms of both source and load sides.

A remaining problem is that the system becomes too complicated, and consequently the design of circuit parameters and control of the system are not easy. For example, the system order of the buck converter of Fig. 2.9 is four, and it is not a simple task to find the dynamic (transient state response) and static (steady state response) solutions by 4×4 matrix manipulations. Note that the buck converter of Fig. 2.9 is one of the simplest converters, and the system order tends to be even higher than ten and the system is even time-varying. Of course, you do not have to worry about these problems. To make the complicated nature of the power circuit simple is the purpose of this book. An easy way of solving the problems will be provided for you.

2.1.6 What Are Allowable Switches and What Are not Allowed?

Concerning the switches in a switch cell, each switch must be of appropriate type to cope with the voltage and current directions of the source and load. Let me show

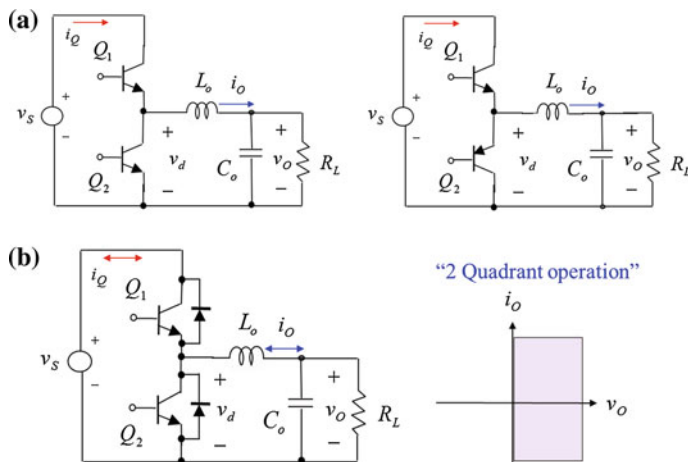


Fig. 2.10 Prohibited and permitted topologies of the buck converter example. **a** Prohibited topologies. **b** Permitted topology

you the configuration of a converter, also referred to as the ‘topology’, for the buck converter example. As shown in Fig. 2.10, the current flow of an inductor and the voltage polarity of a capacitor in the power circuit do not change in a period. The switch cell should cope with these properties; i.e., the switches Q_1 and Q_2 should provide the same output current direction at once. The switch Q_2 of Fig. 2.10a cannot provide forward current, and hence continuous output current flow is not guaranteed. However, the switch cell of Fig. 2.10b provides either positive or negative directions of output current flow at once, which is called as ‘two quadrant operation’ in power electronics. If the switch cell of Fig. 2.10b provides the step down voltage conversion function for the negative polarity of voltage, then it is called ‘four quadrant operation’. This type of converter is called a ‘chopper’ if it is used in AC-AC power conversion. Of course, the converters in Figs. 2.8 and 2.9 are for DC-DC applications because the voltage and current flow of the switch cell can be unidirectional only with the proposed transistor-diode pair. For the chopper applications, the switch cell should be made of bidirectional switches, which operate for both directions of voltage and current.

2.2 Understanding the Operation of Converters

Various aspects of the operation of converters are explained below.

2.2.1 CCM and DCM Analyses for an Ideal Switch Cell

The piecewise LTI circuit analysis, as introduced for the boost converter example in the previous chapter, will be briefly introduced for the buck converter example to see the similarities and differences between the two converters. For simplicity, a buck converter with an output LC filter is selected this time. Drawing piecewise LTI circuits is a good start for analyzing a converter even though it cannot show all features of the operation of a converter, as discussed in the previous chapter. The LTI circuits for the CCM and DCM are two and three, respectively, as shown in Figs. 2.11 and 2.12.

At the beginning of the analysis, usually parasitic circuit elements such as internal resistances in switches, inductors, and capacitors, parasitic capacitances in inductors, and parasitic inductances in capacitors are neglected. Moreover, the source voltage and output voltage are assumed to be perfectly constant; i.e., the output capacitance is large enough so that there is no switching ripple voltage in the output. The system is also assumed to be in the steady state; of course, this is not true and the dynamic response should be explored in many cases for practical applications.

The inductor current becomes a straight line and the positive change of S1 becomes the same as the negative change of S2 in the steady state for the CCM case of Fig. 2.11, as follows:

$$\Delta I_o \cong \frac{V_s - V_o}{L_o} DT \cong \frac{V_o}{L_o} (1 - D)T, \quad (2.4)$$

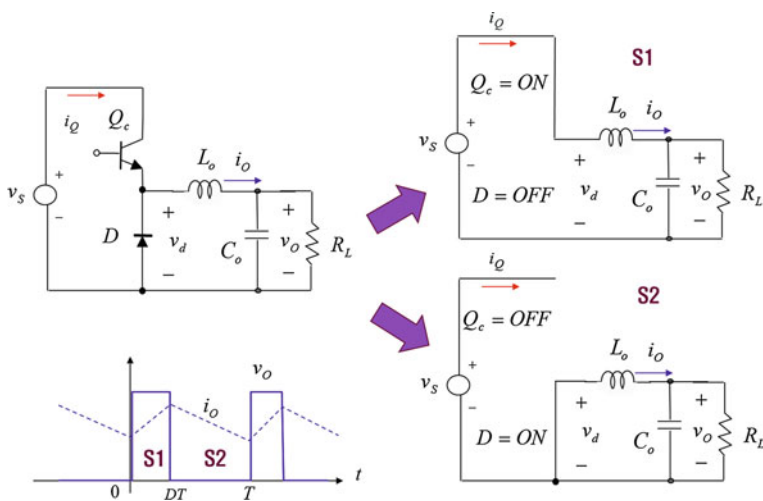


Fig. 2.11 Piecewise LTI circuits for the CCM operating buck converter

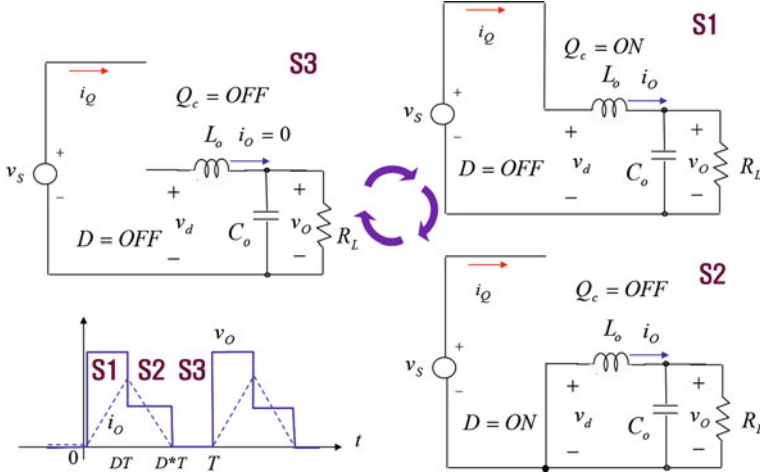


Fig. 2.12 Piecewise LTI circuits for the DCM operating buck converter

which results in a very simple DC gain.

$$G_V \equiv \frac{V_o}{V_s} \cong D. \quad (2.5)$$

We need one more equation to determine the unknown variables in (2.4), which is the following output equation:

$$V_o = I_o R_L \quad \text{or} \quad I_o = V_o / R_L \cong D V_s / R_L. \quad (2.6)$$

Then the minimum and maximum values of the inductor current become as follows:

$$I_{o,min} = I_o - \Delta I_o / 2, \quad I_{o,max} = I_o + \Delta I_o / 2. \quad (2.7)$$

From (2.7), $I_{o,max}$ is used to determine the inductor current rating to withstand magnetic saturation, whereas $I_{o,min}$ is used to determine the boundary condition between the CCM and DCM as follows:

$$I_{o,min} = I_o - \Delta I_o / 2 = 0 \quad \rightarrow \quad D_{BCM} = 1 - \frac{2L_o}{R_L T}. \quad (2.8)$$

As identified from (2.8), no BCM exists for the large L_o or small R_L for a given T which eventually makes D_{BCM} negative. In case the BCM exists, the buck converter operates in the CCM when $D > D_{BCM}$ and operates in the DCM when $D < D_{BCM}$.

In the DCM, the inductor current becomes zero at the time of D^*T , and (2.4) is slightly changed as follows:

$$\Delta I_o \cong \frac{V_s - V_o}{L_o} DT \cong \frac{V_o}{L_o} (D^* - D)T. \quad (2.9)$$

The output equation becomes, considering the average output current becomes the same as the load current, as follows:

$$I_o = \frac{V_o}{R_L} = \frac{\Delta I_o}{2} D^*. \quad (2.10)$$

From (2.9) and (2.10), the duty ratio of conduction D^* is determined.

$$D^* = \frac{L_o}{R_L T} + D. \quad (2.11)$$

Applying (2.11) to (2.9) results in a slightly complicated DC gain for the DCM as follows:

$$G_V \equiv \frac{V_o}{V_s} \cong \frac{K}{1 + K}, \quad \because K \equiv D^* D \frac{R_L T}{2L_o^2}. \quad (2.12)$$

Even though we have assumed the simplest case, the analyses of the most basic buck converter are not so simple. Actually, there are many more analysis and design issues to consider.

2.2.2 Practical Switching Characteristics of a Switching Cell

All practical power switches have finite on and off switching times, which results in temporary open or off circuits, as shown in Fig. 2.13. At the turn off timing of the transistor Q_c , the diode D is not yet turned on until the diode voltage v_d becomes negative, while the Q_c is about to turn off. If the Q_c is forcefully turned off before the D is turned on, an open circuit (A case) may occur. At the instant of turn on timing of Q_c , the D was conducting; hence, a short circuit (B case) may occur if the Q_c is forcefully turned on. Of course these open and circuits are theoretically not allowed, but practical switches with finite switching times are exposed to the danger of failures due to the high open voltage (A case) or large short current (B case) if not properly operated.

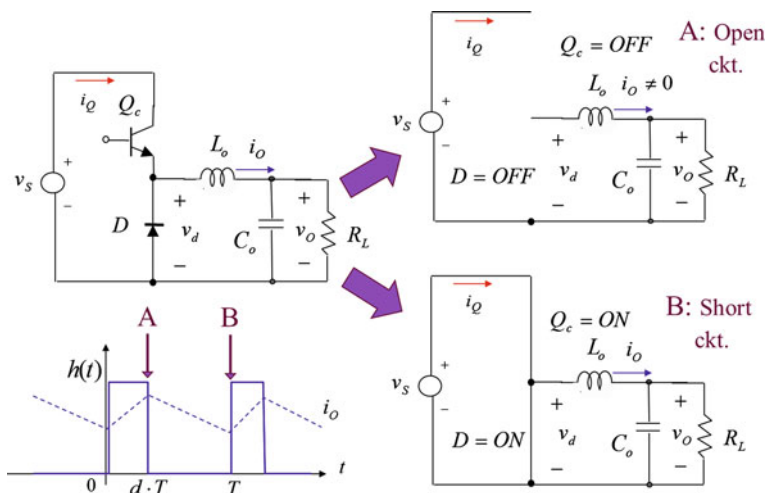


Fig. 2.13 Practical switches may be in danger of open or short circuit due to finite switching times

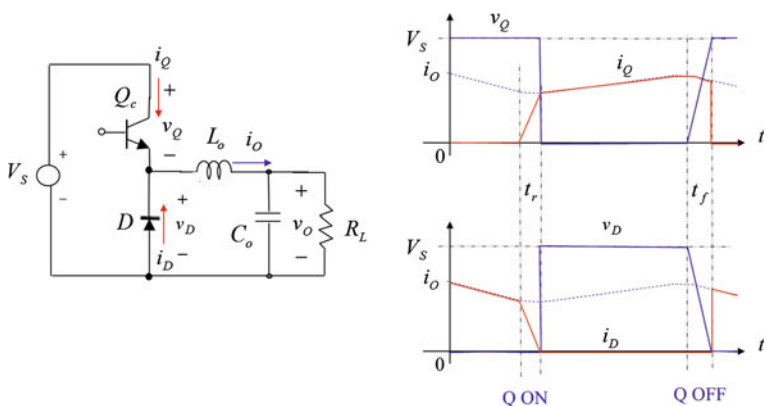


Fig. 2.14 Switching waveforms of a switch cell with finite switching times for an inductive load

As shown in Fig. 2.14, the switching waveforms of a switch cell with finite switching times can be drawn for an inductive load assuming an ideal DC source and load voltages. If the turn-on current and turn-off voltage of Q_c are of straight line change, then the circuit can be analyzed considering the following conditions:

$$v_Q + v_D = V_s \quad (2.13a)$$

$$i_Q + i_D = i_o. \quad (2.13b)$$

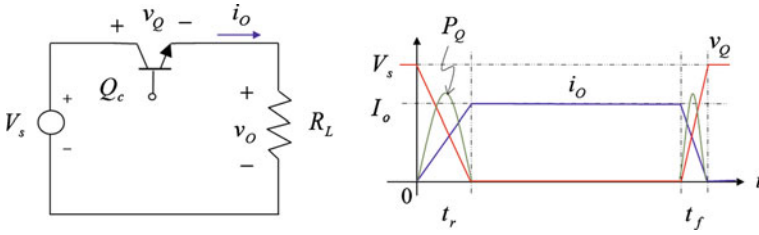


Fig. 2.15 Switching waveforms of a switch cell with finite switching times for a resistive load

The power loss during switching, called switching loss, can be calculated as follows:

$$\begin{aligned}
 P_{sw} = P_Q &= \frac{1}{T} \int_0^T v_Q i_Q dt \cong \frac{V_s I_o}{2} \frac{t_r + t_f}{T} \\
 \therefore \int_0^{t_r} v_Q i_Q dt &\cong \int_0^{t_r} V_s (I_o t / t_r) dt = V_s I_o t_r / 2 \\
 \therefore \int_0^{t_f} v_Q i_Q dt &\cong \int_0^{t_f} V_s (1 - t / t_f) I_o dt = V_s I_o t_f / 2.
 \end{aligned} \tag{2.14}$$

Note that the switching loss of the diode is zero because either the voltage or current of the diode becomes zero during the on and off switching periods. Therefore, the switching loss in the transistor P_Q is the same as the total switching loss P_{sw} of the switch cell in this case. Furthermore, we have not considered the conduction loss of the switches yet. As noticed from (2.14), the switching loss highly depends on the switching waveforms of the switch voltage and current, which is referred as switching trajectory.

Another switching case for a resistive load with finite switching times is shown in Fig. 2.15, where both the voltage and current of the transistor are assumed to vary simultaneously in straight lines.

The switching loss can be calculated as follows:

$$\begin{aligned}
 P_Q &= \frac{1}{T} \int_0^T v_Q i_Q dt \cong \frac{V_s I_o}{6} \frac{t_r + t_f}{T} \\
 \therefore \int_0^{t_r} v_Q i_Q dt &\cong \int_0^{t_r} (V_s - I_o R_L t / t_r) (I_o t / t_r) dt = V_s I_o t_r / 6.
 \end{aligned} \tag{2.15}$$

Comparing (2.15) to (2.14), the resistive load has three times less switching loss than the inductive load. The power efficiency of the converters, often referred to as ‘efficiency’, can be calculated from (2.14) and (2.15) as follows:

$$\eta \equiv \frac{P_o}{P_s} = \frac{P_o}{P_o + P_{sw}} = \frac{1}{1 + P_{sw}/P_o} \quad (2.16)$$

Applying the general efficiency equation of (2.16) to the inductive and resistive switching cases results in the following.

$$\eta_L = \frac{1}{1 + \frac{V_s I_o}{2} \frac{t_r + t_f}{T} \frac{1}{V_o I_o}} = \frac{1}{1 + \frac{t_r + t_f}{2T} \frac{1}{G_V}} \cong \frac{1}{1 + \frac{t_r + t_f}{2T} \frac{1}{D + t_f/(2T)}} = \frac{1}{1 + \frac{t_r + t_f}{2TD + t_f}} \quad (2.17a)$$

$$\eta_R \cong \frac{1}{1 + \frac{V_s I_o}{6} \frac{t_r + t_f}{T} \frac{1}{V_s I_o D}} = \frac{1}{1 + \frac{t_r + t_f}{6T} \frac{1}{D}} \quad (2.17b)$$

As noticed from (2.17a, 2.17b), the efficiency highly depends not only on the switching times and load types but also the duty ratio, which should be considered in cases where higher efficiency is required.

So far, it has been assumed in this section that there is no parasitic inductance and capacitance in a switch. In practice, switches in a switch cell involve lots of parasitics, which play important roles in every switching, as shown in Fig. 2.16. For the turn-on process of a switch cell, as denoted by S1, both the transistor and diode

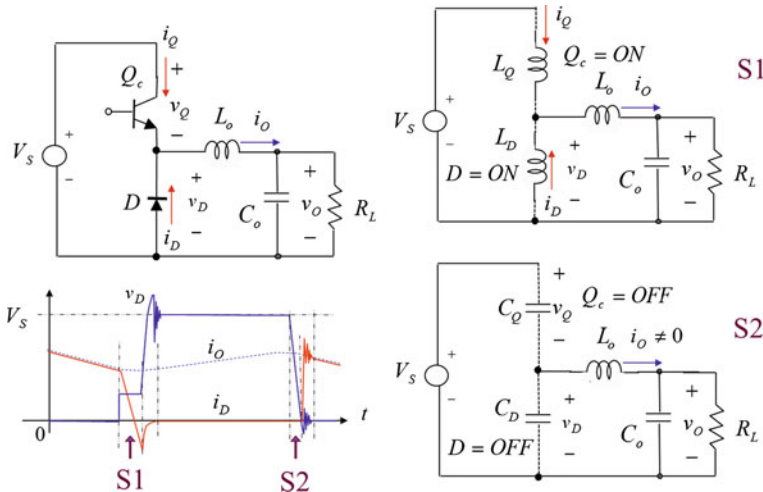


Fig. 2.16 Practical switching on/off processes, where switches involve parasitic inductances and capacitances

are turned on and a short circuit is established. The parasitic inductances of the switches L_Q and L_D then mainly determine the slope of current i_D until the reverse recovery of the diode ceases. Just after the reverse recovery process, a non-linear parasitic capacitance of the diode of a few pF gives rise to resonant ringing together with the parasitic inductances, which is typically a few MHz damping sinusoidal waveform.

Question 2

Can you try to analyze the parasitic resonant ringing phenomena?

For the turn-off process of the switch cell, as denoted by S2, both the transistor and diode are turned off and an open circuit is established. Then, the parasitic capacitances of the switches C_Q and C_D mainly determine the slope of the voltage v_D until the reverse recovery of the diode ceases. As soon as the diode is turned on, the parasitic inductance L_D gives rise to another resonant ringing together with the parasitic capacitances.

As I have explained a few aspects of a practical switching phenomenon, the switching process is never simple and easy to handle. But this switching process is quite important, perhaps the most important aspect, in the design of a switching converter because it determines the switching loss, power efficiency, and reliability of the switching converter. In particular, the switching trajectory determines the reliability of each switch because the junction temperature of a switch increases due to the switching loss. Therefore, the circuit fabrication of a switch cell should be very compact in size and length to reduce the parasitic inductances, and the selection of switches must be made considering the parasitic capacitances in order to have fast switching or less switching loss. Much more detailed analyses and measurements should be made in practice to build a long lasting reliable converter, which are left for practice.

2.2.3 *Snubber Circuits Are Often Used to Improve Switching Characteristics*

The reliability of switching devices in a converter is highly determined by the switching characteristics as mentioned above. One of the switching problems is the over voltage that arises from parasitic ringing, which should be mitigated or constrained. Another important switching problem is the large slope of the reverse recovery current of a diode, which results in high voltage spikes or breakdown of the main switch such as a transistor and silicon controlled rectifier (SCR). Two example snubber circuits are illustrated for an inductive load, as shown in Fig. 2.17.

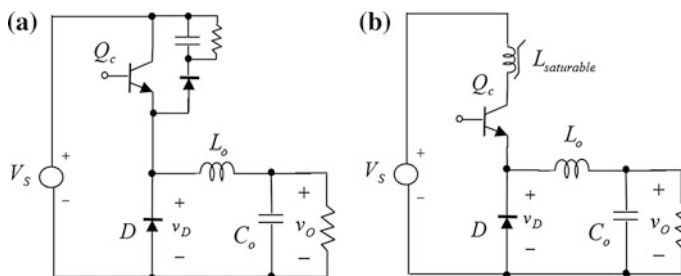


Fig. 2.17 Snubber circuits for an inductive load, protecting switches and improving switching characteristics. **a** For over voltage protection. **b** For di/dt limit

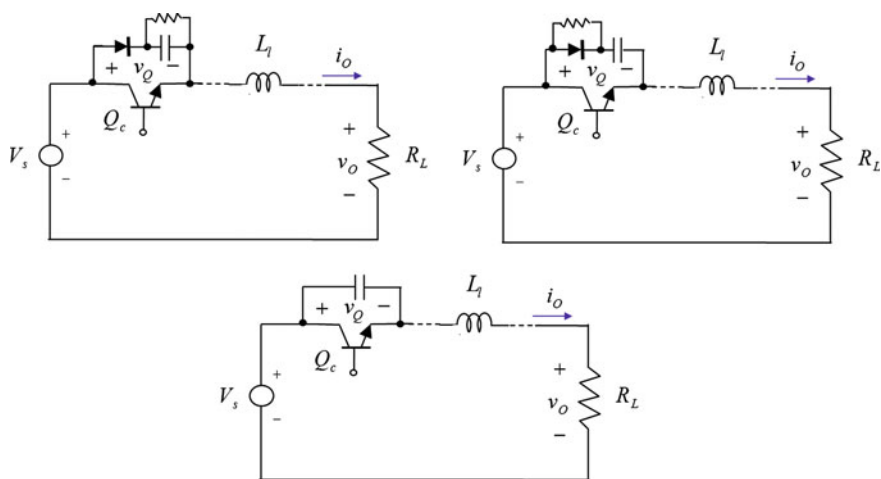


Fig. 2.18 Snubber circuits for a resistive load, protecting the switch from a stray inductance

As explained for the single switch resistor case of Fig. 2.6, the line inductance L_l may give rise to a high voltage spike when the transistor is turned off, and the snubber circuits, as shown in Fig. 2.18, can protect the switch from voltage breakdown.

Phasor Power Electronics

Rim, C.T.

2016, XIV, 249 p. 193 illus., 54 illus. in color., Hardcover

ISBN: 978-981-10-0535-0