Chapter 2
CMOS Transistor Reliability and Variability Mechanisms

Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the nanometer regime have resulted in major reliability issues due to high electric field phenomenon. These include hot carrier injection (HCI) [1, 2], gate oxide breakdown (BD) [3, 4], and negative bias temperature instability (NBTI) [5, 6]. These reliability mechanisms cause the MOS transistor parameter drifts; namely, threshold voltage shift and mobility degradation. A brief discussion on the MOS device reliability is described as follows.

2.1 Hot Electron Effect

When the electric field at the drain edge of the MOS transistor is very high, avalanche breakdown may occur. Impact ionization in the drain depletion region generates many energized electrons. These high energy carriers may damage interfacial layer and create interface traps and oxide trapped charges [7] which degrade device parameters such as an increase in threshold voltage. Figure 2.1 displays the drain current degradation versus drain-source voltage subjected to different stress times. At given drain-source voltage V_{DS} and gate-source voltage V_{GS}, the drain current decreases with stress time as shown in Fig. 2.1.

2.2 Gate Oxide Breakdown

High electric field across the gate insulator could induce time-dependent dielectric breakdown. The formation of random defects and conduction path within the gate dielectric increases the gate leakage and noise. For ultrathin gate oxide transistors under constant gate voltage stress, the soft breakdown could be observed before hard breakdown [8]. Compared with hard breakdown (HBD), SBD becomes more

J.-S. Yuan, *CMOS RF Circuit Design for Reliability and Variability*,
SpringerBriefs in Reliability, DOI 10.1007/978-981-10-0884-9_2

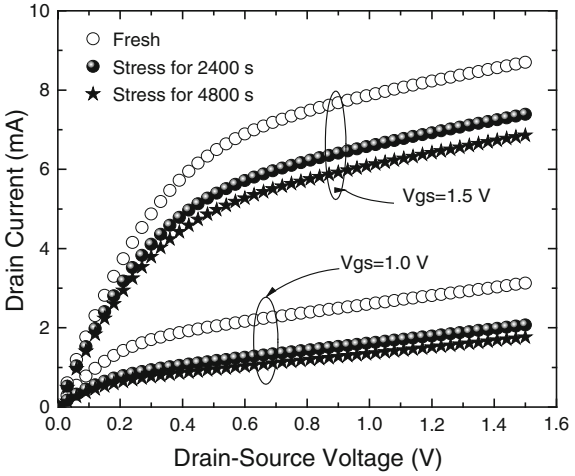

Fig. 2.1 Drain current degradation due to hot electron stress (© IEEE)

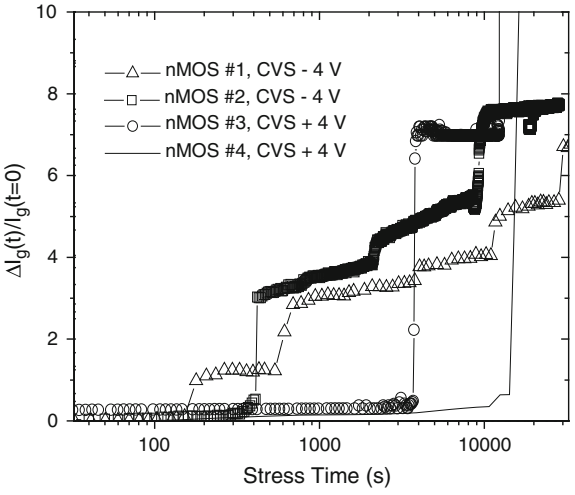

Fig. 2.2 Normalized I_g versus stress time. The nMOS is under positive or negative constant gate bias (© IEEE)

prevalent for thinner oxides and for oxide stress at relatively lower voltages. In addition, hot carrier injection could trigger more SBD in addition to conventional Fowler–Nordheim (FN) tunneling [9].

Figure 2.2 shows the normalized gate leakage current as a function of stress time under constant voltage (CVS). The gate soft breakdown degrades the threshold voltage and mobility of the MOSFET as observed by the current–voltage characteristics [10].

2.3 Negative Bias Temperature Instability

Negative bias temperature instability is related to a build up of positive charges occurring at the Si/SiO_2 interface or in the oxide layer for p-channel transistors under negative gate bias. The reaction–diffusion model [11] illustrates the holes in the inversion layer of pMOSFETs reacting with the Si–H bonds at the SiO_2/Si interface. The hydrogen species diffuse away from the interface toward the polysilicon gate. This causes the threshold voltage instability of pMOSFETs. The NBTI effect is enhanced at higher temperatures. Note that NBTI is a degradation of transistor performance for pMOSFETs, where positive bias temperature instability (PBTI) transistor occurs for nMOSFETs with high-k dielectrics [12].

To investigate the oxide breakdown and hot electron effect on the nMOS transistors at various stress conditions, accelerated DC voltage stress is employed. Figure 2.3 shows the drain current versus drain-source voltage and Fig. 2.4 displays the transconductance versus gate voltage of the 65 nm nMOS during 220 min of hot electron stress at V_{GS} = 0.35 V and V_{DS} = 2.0 V. At high drain-source voltage, hot carrier injection occurs because of high electric field and impact ionization at the drain region of MOSFETs. Again, these high energy carriers may introduce damage by creating interface traps and oxide trapped charges and can cause degradation of device parameters such as an increase in threshold voltage and a decrease in transconductance. At a given drain voltage, the drain current decreases with stress time and at a given gate voltage, the transconductance decreases with stress time due to hot electron degradation.

The 65 nm NMOS is also measured under gate oxide stress at V_{GS} = 2.9 V and V_{DS} = 0 V. The results are shown in Fig. 2.5. After significant oxide stress effect resulting from high gate voltage, the transconductance shifts down rapidly in the initial 60 min as seen in Fig. 2.5. The off-state stress effect is evaluated in Fig. 2.6.

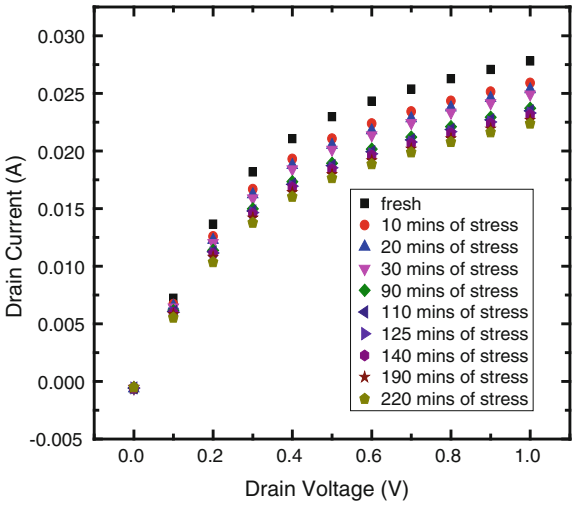

Fig. 2.3 I_D-V_D at different stress times (DC stress at V_{GS} = 0.35 V ad V_{DS} = 2.0 V)

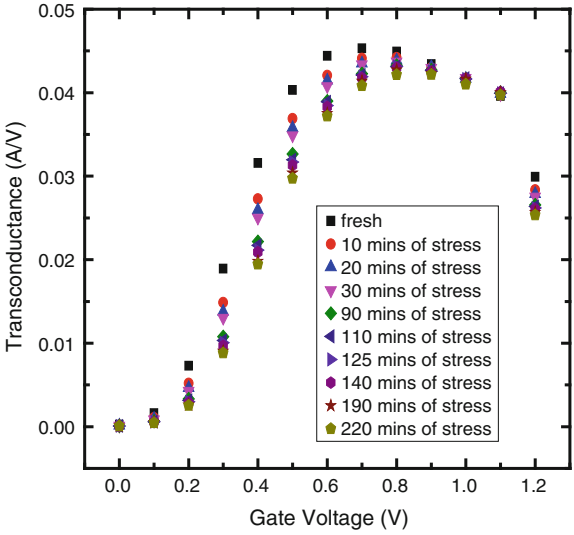

Fig. 2.4 Transconductance at different stress times (DC stress at V_{GS} = 0.35 V ad V_{DS} = 2.0 V)

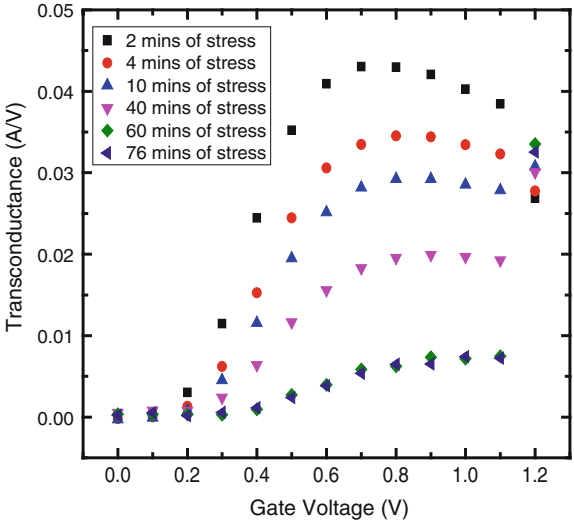

Fig. 2.5 Transconductance versus gate voltage (oxide stress at V_{GS} = 2.9 V ad V_{DS} = 0 V)

The 65 nm nMOS was stressed at V_{GS} = 0 V ad V_{DS} = 2.8 V. High drain-source voltage results in high electric field in the drain region, which may trigger hot electron injection into the gate oxide to degrade the drain current. High drain-gate voltage may also induce gate oxide breakdown close to the drain edge. As shown in Fig. 2.6, the transconductance degrades quickly after only 30 min of off-state high drain voltage stress. After 30 min of stressing, the transconductance collapses possibly due to oxide hard breakdown accelerated by hot electron injection during off-state.

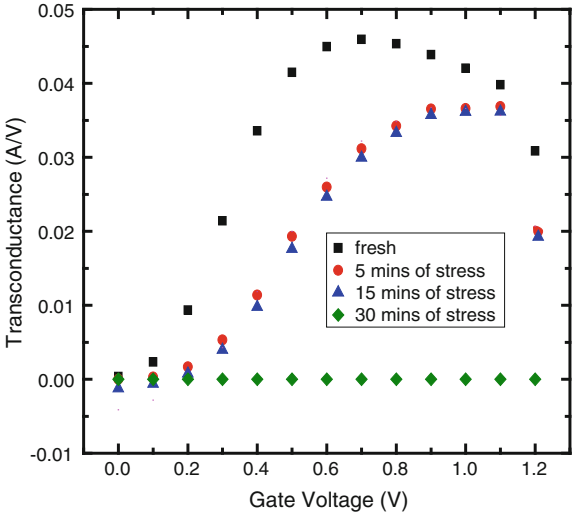

Fig. 2.6 Transconductance at different stress times (DC stress at V_{GS} = 0 V ad V_{DS} = 2.8 V)

2.4 Process Variability

Process variations were originally considered in die-to-die variations. For nanoscale transistors, intra die variations are posing the major design challenge as technology node scales. The intrinsic device parameter fluctuations that result from process uncertainties have substantially affected the device characteristics. Process variability comes from random dopant fluctuation, line edge roughness, and poly gate granularity [13, 14]. The threshold voltage fluctuation due to random doping profile is approximated as [15]:

$$\sigma^2_{Vt,\text{doping}} = \frac{2q^2 t^2_{\text{ox}}}{WL\varepsilon^2_{\text{ox}}} \int_0^{W_D} N_A(x)(1 - \frac{x}{W_D})^2 \text{d}x \tag{2.1}$$

where q is electron charge, t_{ox} is the oxide capacitance, W is the channel width, L is the channel length, ε_{ox} is the oxide permittivity, and N_A is the acceptor doping. With shrinking of gate length, the deviation of threshold voltage is expected to be larger.

A computational effective device simulator [16] is used into demonstrate random doping fluctuation effect on the MOSFET model parameter variation. A 22 nm LDD NMOS transistor is constructed as an example to illustrate the threshold voltage fluctuation. From Fig. 2.7, it is seen that the acceptor dopant causes positive V_T fluctuation with peak value of 0.0045 V located around the center of the channel. Due to the random doping fluctuation, the standard deviation (STD) of V_T for the 22 nm MOSFET is computed to be 0.031 V or its corresponding spread (STD/Mean) of 6.9 %.

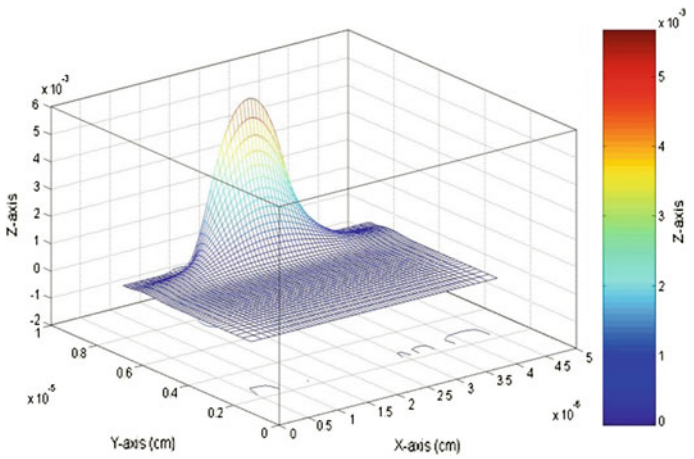

Fig. 2.7 Sensitivity function distribution of V_T versus acceptor (© IEEE)

CMOS technology continues device scaling for high integration. However, as feature sizes shrink and chip designers attempt to reduce supply voltage to meet power targets in large multi-core systems, parameter variations are becoming a serious problem. Parameter variations can be broadly classified into device variations incurred due to imperfections in the manufacturing process and environmental variations and on-die temperature and supply voltage fluctuations. Smaller feature size further makes CMOS circuits more vulnerable to process, supply voltage, and temperature (PVT) variability. Large design margin is then needed to insure circuit robustness against reliability issues. Using PVT and long-term reliability resilience design is becoming an essential design requirement for the future technology nodes and may reduce overdesign, while increasing yield and circuit robustness.

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http://www.springer.com/978-981-10-0882-5

CMOS RF Circuit Design for Reliability and Variability

Yuan, J.-S.

2016, VI, 106 p. 101 illus., Softcover
ISBN: 978-981-10-0882-5