

Chapter 2

Analog Signals Conditioning and Discretization

2.1 Introduction

In control systems it is necessary to observe the work of the controlled object. This is usually achieved in power electronics systems by measuring currents and voltages [7, 112]. This chapter is devoted to the problems of processing the analog current and voltage signals to convert them into digital form in power electronics systems [89, 90]. The problems discussed in this chapter, the author believes, are essential for the proper operation of control systems.

2.2 Analog Input

Typical circuits of analog inputs for measuring voltages and currents are shown in Fig. 2.1. In the voltage measurement circuit (Fig. 2.1a), voltage from the voltage divider (R_1 , R_2) goes through the amplifier input and the antialiasing filter to the sample-and-hold circuit (SH) and analog-to-digital converter (A/D). Finally digital signal $x_1(nT_s)$ corresponding to the measured voltage is sent to the processor control system. A similar process takes place in the current measurement circuit (Fig. 2.1b), where instead of a voltage divider, current transducer is applied. Current measurement issues are discussed in Sect. 2.3.

2.2.1 Galvanic Isolation

In low-power electronics systems it is possible to use measurement systems electrically coupled with the control system. This is often the cheapest and best option, especially if accuracy is taken into account. However, usually in high-power systems galvanic isolation in measurements is required. It should be noted that the

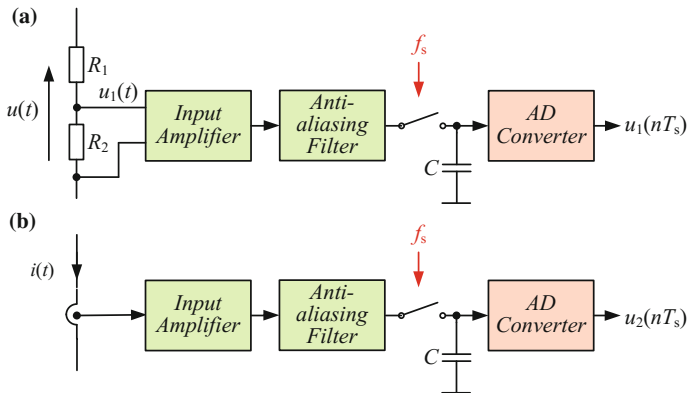
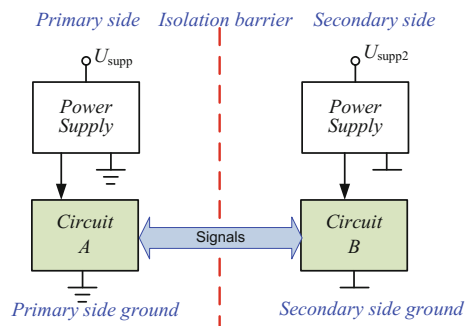


Fig. 2.1 Analog input of A/D converter: **a** voltage measurement, **b** current measurement

application of galvanic isolation always deteriorates the quality of the signal, but it is often necessary. A system with galvanic isolation is shown in Fig. 2.2, consists of two circuits, A and B, with signals between circuits are connected through an isolation barrier. The signals can be transmitted through an isolation barrier using optical wave, sound wave, radio wave, capacitive coupling, inductive coupling, or mechanical coupling (piezoelectrics). Circuits A and B are supplied by separate power supply units. Reasons for the use of galvanic isolation include:

- **Protection from high voltages.** Isolation provides a dielectric barrier that acts as an insulator against high voltages in power electronics circuits where higher power levels are required. It is also important for safety reasons.
- **Break ground loop.** Galvanic isolation breaking the ground currents (return path) of an electrical circuit to only one side of the barrier, enabling a noise-free environment for sensitive measurements on the other side. Galvanic isolation is increasing noise immunity.
- **Level translation.** Enabling noise-free data transfer between circuits that operate at different voltage rails is a common challenge for electronics designers.

Fig. 2.2 System with galvanic isolation



For example, the control gates of transistors in the inverter is a key issue in power electronics circuits. Although there are many non-isolated level shifters available to circumvent this problem, using an isolator provides several solid advantages. Isolators are the most noise-free and robust solution, and they prevent parasitic paths that may inadvertently switch devices on or off.

- **Protection from high common voltage.** Galvanic isolation protects parts of circuit working with different voltage level. This eliminates the need for a level shifter, however, requires the use of additional galvanically isolated power supply.

2.2.2 Common Mode Voltage

Measurements in power electronics systems are very difficult due to a very high slew rate of common mode voltage. The common mode voltage swings of several hundred volts in tens of nanoseconds are common in modern switching inverters. The isolation amplifier should be designed to ignore very high common mode transient slew rates (of at least from 10 to 25 kV/ μ s or more).

Figure 2.3 depicts an isolation amplifier connected to one leg of a power inverter.

During the operation of the inverter, the potential of point A voltage changes from -500 to 500 V in a time equal to 100 ns. The slew rate of voltage change can be determined by the equation

$$SR = \frac{du(t)}{dt} \approx \frac{\Delta U}{\Delta t} \quad (2.1)$$

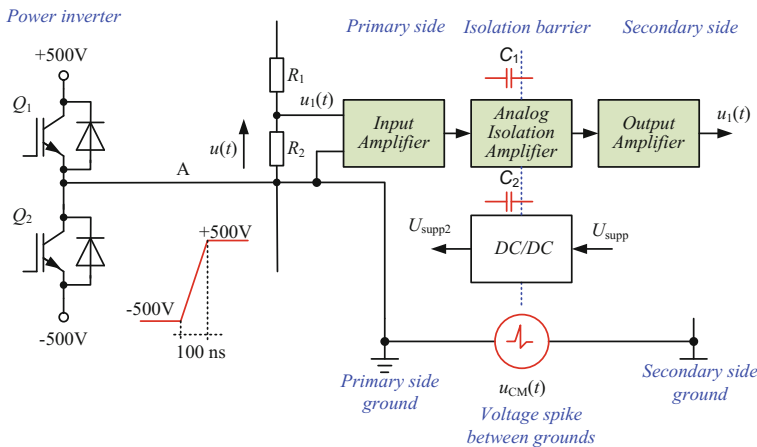
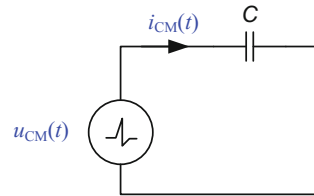


Fig. 2.3 Circuit for illustration of common mode voltage

Fig. 2.4 Simplified circuit for common mode current



Capacitor C_1 represents the resultant common mode (parasitic) capacitance on the signal path, capacitor C_2 represents the resultant common mode (parasitic) capacitance in the DC/DC converter. The circuit of an isolation amplifier for a common mode (parasitic) current calculation can be simplified to the circuit shown in Fig. 2.4. Thus, the value of parasitic current can be calculated by equation

$$i_{CM}(t) = C \frac{du_{CM}(t)}{dt} \approx C \frac{\Delta U_{CM}}{\Delta t} , \quad (2.2)$$

where: C —resultant common mode (parasitic) capacitance.

As an example, for $SR = 10 \text{ kV}/\mu\text{s}$ and $C = 10 \text{ pF}$ common mode current the value is 10 mA. It is a too high value especially for sensitive electronics input circuits, such as optoelectronic devices.

Common mode rejection (CMR) is a measure of the ability of a device to tolerate common mode noise. Usually common mode rejection is specified as common mode transient rejection (CMTR). CMTR describes the maximum tolerable rate-of-rise (or fall) of a common mode voltage, usually given in kilovolts per microsecond ($\text{kV}/\mu\text{s}$). The specification for CMTR also includes the amplitude of the common mode voltage $u_{CM}(t)$ that can be tolerated.

For example, Avago's optoelectronic circuits (former produced by Hewlett Packard) are an industry reference solution [10, 11]. Figure 2.5 shows two types of single-transistor optocouplers a classical (Fig. 2.5a) and with an internal Faraday shield (Fig. 2.5c). The internal components of the optocouplers are marked by the green dashed lines. $u_{CM}(t)$ represents a voltage spike across the optocoupler isolation path between the primary side ground and secondary side ground. $E(t)$ represents a signal voltage applied across the input side. The common mode current $i_{CM}(t)$ flows through isolation barrier and changes output transistor base current $i_B(t)$. Figure 2.5b shows simplified waveforms for common mode voltage response for the classical optocoupler. This type of failure is avoided by adding an internal Faraday shield as shown in Fig. 2.5c. Referring to Fig. 2.5c, the parasitic distributed capacitances, C_1 and C_2 are shown across the LED anode to secondary side ground and LED cathode to secondary side ground. The common mode current flown through capacitor C_1 changes the LED current during common mode transients. For instance, if the LED is on, then during a positive transient (i.e., $du_{CM}(t)/dt > 0$), the LED current will be decreased. For fast enough transients, this may turn the LED off. Figure 2.5d shown simplified waveforms for common mode voltage response for

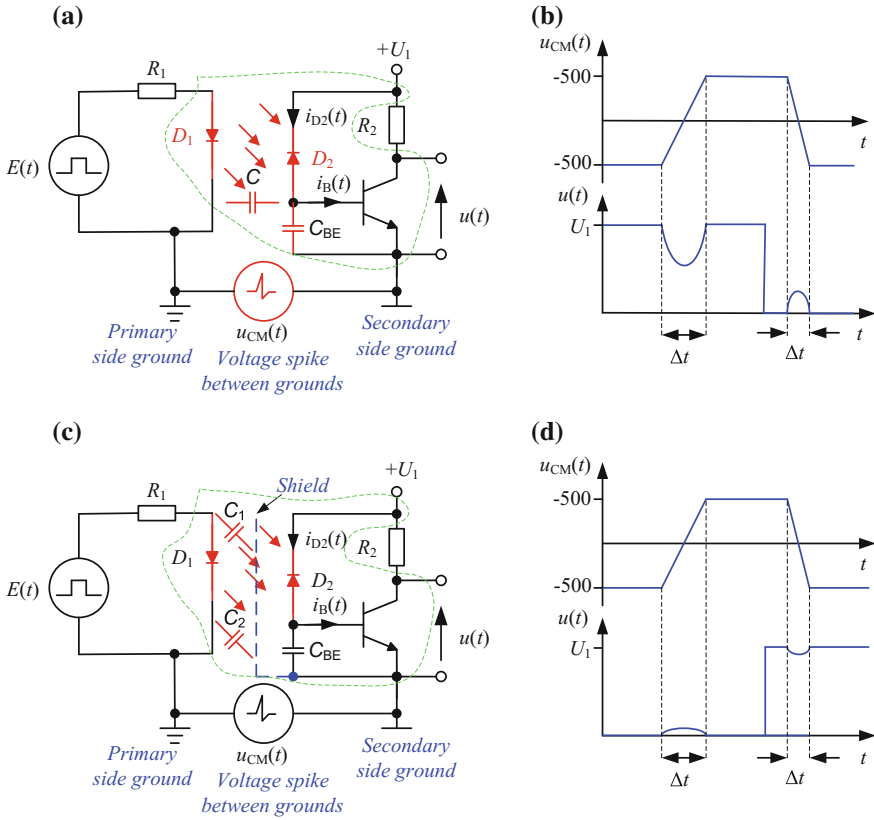


Fig. 2.5 Optocouplers: **a** a classical optocoupler, **b** simplified waveforms for common mode voltage response for classical circuit, **c** a optocoupler with shield, **d** simplified waveforms for common mode voltage response for circuit with shield

circuit with the internal Faraday shield. This type of failure is avoided by ensuring that C_1 and C_2 are small. Also, the printed circuit board and connections should be designed to minimize the parasitic capacity.

2.2.3 Isolation Amplifiers

Topologies of isolation amplifiers are shown in Fig. 2.6. A topology with analog isolation amplifier is depicted in Fig. 2.6a. In this solution solution is mostly used either an optical or electromagnetic separation. The cheapest one is optical separation with linearization. The advantage of such a system is the small signal delay. A typical example of solution with optical separation is the integrated circuit (IC),

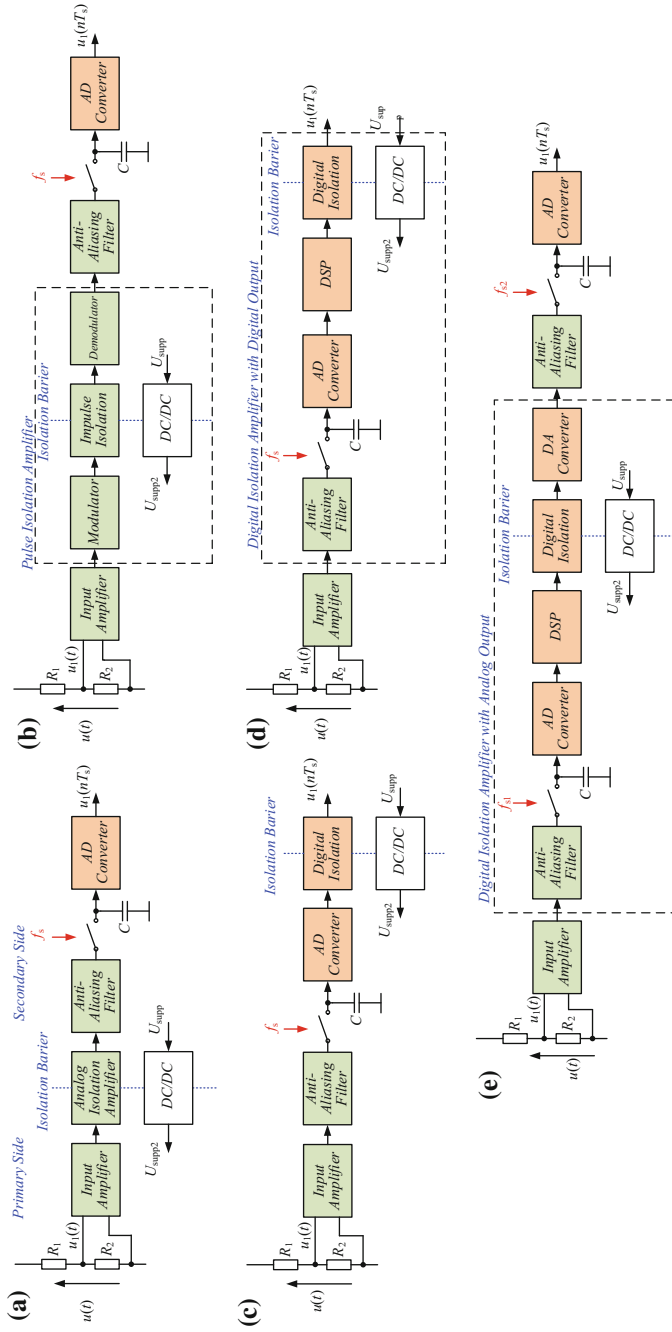
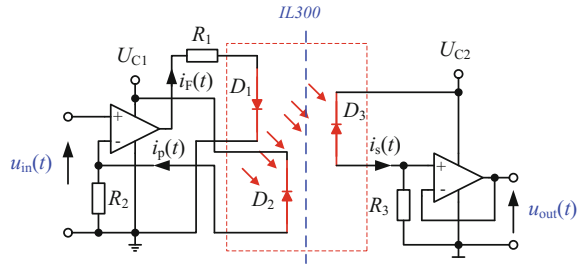


Fig. 2.6 Signal isolation technique typologies: **a** an analog solution, **b** a pulse solution, **c** a digital, **d** a digital with DSP, **e** a digital with DSP and analog output

Fig. 2.7 Isolation amplifier with feedback IL300



IL300 from Vishay [107] (originally introduced by Siemens). The IC Fig. 2.7 consists of an LED D_1 irradiating an isolated feedback photodiode and an output photodiode D_3 in a bifurcated arrangement. The feedback photodiode D_2 captures a part of the LEDs flux and generates a control signal $i_p(t)$ that can be used to serve the LED drive current $i_F(t)$. This technique couples AC and DC signals and compensates for the LED's non-linear, time, and temperature characteristics. The IC achieves the following parameters: 0.01% servo linearity, wide bandwidth, >200 kHz, high gain stability, 0.005 %/°C typically.

The time and temperature stability of the coupler transfer function is insured by using matched PIN photodiodes D_2 and D_3 that accurately track the output flux of the LED. In alternative solutions the transformer is used, which allows the transfer of AC signals and DC signals by adding the Hall sensor. Primary circuits are supplied by an isolated DC/DC converter.

The most common used topology of the insulation circuit is shown in Fig. 2.6b. In this system an isolation pulse amplifier is applied. It consists of an input modulator, pulse signal isolator and demodulator. Such systems give high accuracy at a low price. In typical applications the modulation frequency is in the range of 10 kHz–1 MHz. The use of modulation prolongs the typical impulse response time and causes the occurrence of modulation components in the output signal. In applications with transformer isolation, the transformer can also be used to transfer energy to supply the primary side circuits.

Examples of industrial integrated circuits include: isolation amplifier with capacitive isolation ISO124, ISO121 [93, 96], Si8920 [83, 84], classical isolation amplifier with transformer isolation AD215 [4], isolation amplifier with optical isolation barrier HCPL-7800 [8].

An interesting solution has been applied in the ISO121, through the use of precision isolation amplifiers with duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2×1 pF differential capacitive barrier. Simplified block diagram of ISO121 is shown in Fig. 2.8. The IC achieves the following parameters: 0.01% max nonlinearity, bandwidth, 6 kHz, high gain stability and $150 \mu\text{V}/^\circ\text{C}$ maximum offset voltage drift. The IC, shown in Fig. 2.9, is built into a ceramic barrier, where modulator and demodulator are placed at the ends and two 1 pF matched barrier capacitors are placed in the middle. This IC has excellent reliability.

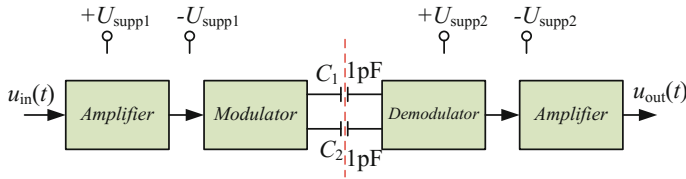


Fig. 2.8 Simplified block diagram of ISO121

Fig. 2.9 Precision isolation amplifier with capacitor barrier isolation

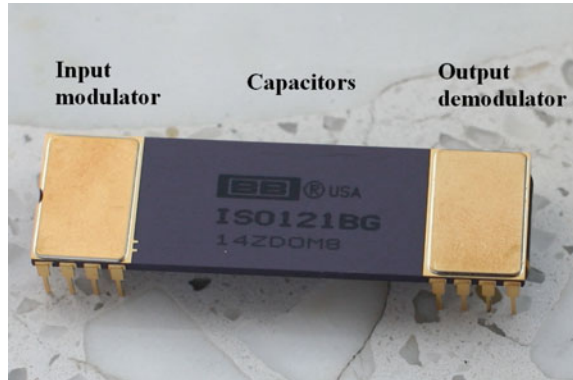
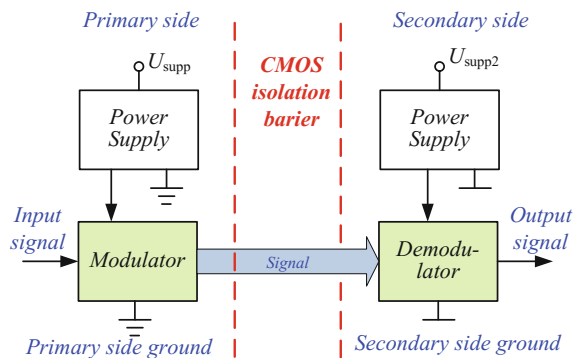


Fig. 2.10 Si8920 isolation amplifier with capacitor barrier isolation



The Si8920 is a low-cost galvanically isolated analog amplifier [83, 84] from Silicon Laboratories. The block diagram of the Si8920 IC is shown in Fig. 2.10. The low-voltage differential input ± 100 mV, with nonlinearity: 0.1% full scale, is good for measuring voltage across a current shunt resistor or for any application where a sensor must be isolated from the control system. The amplifier has very high common-mode transient immunity: $75 \text{ kV}/\mu\text{s}$, it is important for power electronics application. Another advantage of this circuit is that it has low signal delay: $0.75 \mu\text{s}$, especially important for feedback circuit. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes

Table 2.1 Comparison of isolation amplifiers

Signal isolation technique	Accuracy	Delay	Power consumption	Relative cost	Typical signal ranges
Analog, optoelectronic isolation	0.5–5%, High nonlinearity and temperature drift	Low	Low	Low	DC to 200 kHz
Analog with transformer isolation	0.5–5%	Low	Low	Low	AC, 50–200 kHz
Pulse, optoelectronic isolation	0.01–0.5%	Moderate	Low	Low	DC to 100 kHz, output with signal containing residuals of the modulation component
Pulse with transformer isolation	0.01–0.5%	Moderate	Moderate	Low	DC to 300 kHz, output with signal containing residuals of the modulation component
Pulse with capacitive isolation	0.01–0.5%	Moderate	Moderate	Low	DC to 300 kHz, output with signal containing residuals of the modulation component
With A/D converter on primary side	Depending on the A/D converter, possible error correction	Low	Moderate-High	Moderate	DC to 100 kHz, difficult realization of simultaneous sampling
With A/D converter and DSP on primary side	Depending on the A/D converter	Moderate	High	High	DC to 100 kHz, difficult realization of simultaneous sampling
Digital transducer on primary side with analog output	Depending on the A/D and D/A converters, possible error correction	High	High	High	DC to 50 kHz, double signal conversion, difficult realization of simultaneous sampling

compared to other isolation technologies. Despite the use of typical plastic enclosure (DIL8) it supports up to 5 kV_{RMS} withstand voltage per UL1577 standard.

In the next solution the A/D converter was moved to the primary side. Hence signal to the secondary side is transmitted in digital form (Fig. 2.6c). Such a solution

allows the elimination of errors introduced by the insulation system. But in the case of multi-channel systems it is difficult to synchronize the sampling moments. Optically isolated sigma delta modulator HCPL-7860 [9] with digital output is the simplest example of such a solution.

In the next circuit (Fig. 2.6d) is an added DSP to allow local measurement error correction and additional algorithms. In another topology (Fig. 2.6e) a digital isolation transducer is used. In this design the input signal is converted to digital form and in this form it is sent to the secondary side, then it is converted to analog from. In this configuration, as in the previous one, it is possible to correct an error. The disadvantages of this system are the high price and the double signal conversion causing signal delay. Comparison and summary of the galvanic isolation techniques are presented in Table 2.1.

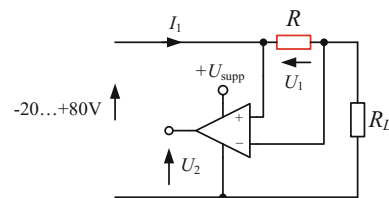
2.3 Current Measurements

Current sensors are often used to provide essential information to power electronics control systems. Current transducers convert measured current to a proportional AC or DC voltage or milliamp signal. These devices should have extremely low insertion impedance. There are also current transducers with digital output and in the author's opinion they will play an increasing role in current measurement systems in future. There are several techniques that are typically used for measuring currents: sense resistor (resistive shunt), current transformer, current transformer with Hall effect sensor, current transformer with magnetic modulation and air coil.

2.3.1 A Resistive Shunt

A sense resistor is inserted in series with the load. Through Ohm's law, $U = IR$, we know the voltage drop across the resistor is proportional to the current. This system is very simple and provides very accurate measurements, given that the resistance value has a tight tolerance. To maintain low dissipation power voltage across sense resistors, the resistance value should be very low, therefore they also require a high quality amplifier, such as instrumentation amplifiers, to generate an exact signal.

Fig. 2.11 Current measurement with high common mode amplifier



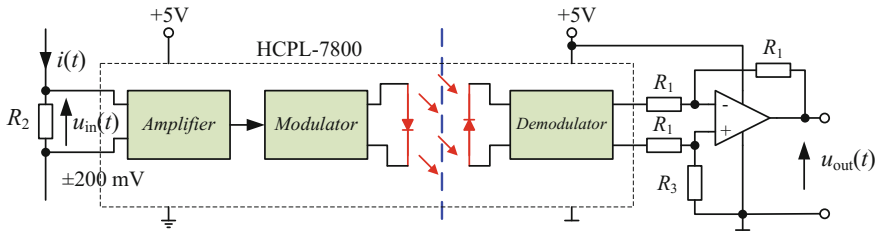


Fig. 2.12 Simplified diagram of HCPL-7800 current measurement circuit

kind of measurement does not provide galvanic isolation, so in some applications an isolation amplifier needs to be used. For larger currents sense resistors with high performance thermal packages have been used. In the last few years there has been extensive development of portable battery-powered electronic devices, and as a result a high demand for current measurement systems has been created. It is a typical way of measuring battery currents, thus, there has arisen a great demand for simple and inexpensive measurement systems. Figure 2.11 shows a measurement system with an amplifier with a unique high common mode ratio to allow for work above the positive supply voltage (U_{supp}) and under the negative supply voltage of amplifier. Common mode voltage of such amplifiers achieves -20 – 80 V. A typical voltage value U_2 is several hundred millivolts. Many manufacturers produce such circuits, for example: integrated circuit INA270 from Texas Instruments [97], AD8210 from Analog Devices [5] etc. Due to the voltage range, this kind of amplifier is also widely used in automotive applications. For current sensing in power electronics circuits the HCPL-7800 family isolation amplifier was designed [8]. The HCPL-7800 utilizes delta sigma modulator converter technology, chopper stabilized amplifiers, and a fully differential circuit topology. Figure 2.12 depicts a simplified diagram of a current measurement circuit. In a typical implementation, currents flow through an external resistor and the resulting analog voltage drop is sensed by the HCPL-7800. The HCPL-7800 input voltage range is equal to ± 200 mV. A differential output voltage is created on the other side of the HCPL-7800 optical isolation barrier. This differential output voltage is proportional to the input current and can be converted to a single-ended signal by using an operational amplifier as shown in Fig. 2.12. The HCPL-7800 was designed to ignore very high common-mode transient slew rates (of at least 10 kV/ μ s). A similar solution can be achieved using newer IC Si8920 [83, 84] from Silicon Laboratories, which was described in the previous section.

2.3.2 Current Transformers

Current transformers are relatively simple and passive (self-powered) devices, and do not require driving circuitry to operate. They are two-wire components with voltage or current output. The primary current (AC) will generate a magnetic field. The field

Fig. 2.13 Current transformer

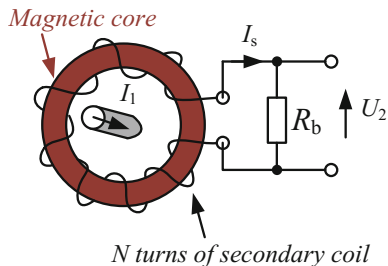
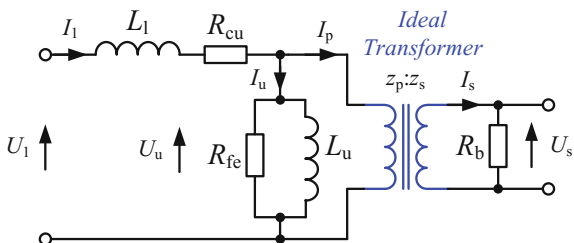


Fig. 2.14 Simplified equivalent circuit of current transformer



is concentrated by magnetic core. The secondary coil is coupled with the primary coil by magnetic field. This is the principle that governs all transformers. Current transformers are designed to measure AC current and typically work between 20 and 400 Hz, although some units will work in the kilohertz range. Inductive current transducers are available in both solid-core and split-core configurations. For an ideal transformer, the secondary current magnitude is proportional to ratio of the primary number of turns z_p (typically from one to several) to secondary number of turns z_s (typically thousands), thus, the secondary current I_s for an ideal transformer can be calculated by the equation

$$I_s = \frac{z_p}{z_s} I_p \quad (2.3)$$

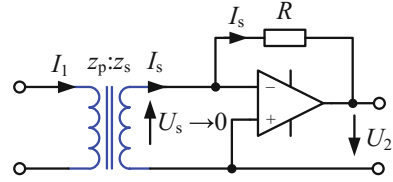
The current transformer is shown in Fig. 2.13. The secondary current is then sensed through a sense resistor R_b to convert the output into a voltage U_2 .

For a real transformer this equation is more complicated. Figure 2.14 shows a simplified version of a low frequency current transformer model of electric circuit. This model is called the high side equivalent circuit model because all parameters have been moved to the primary side of the ideal transformer. In this circuit: L_l —resultant windings leakage inductance, R_{cu} —resultant windings resistance, R_{fe} —resistance which represents power losses in transformer core (mainly due to hysteresis), L_u —main transformer inductance, magnetizing inductance.

Hence, for this transformer model secondary current should be calculated by the equation

$$I_s = \frac{z_p}{z_s} (I_1 - I_u) \quad (2.4)$$

Fig. 2.15 Current converter with minimized current transformer output voltage



Magnetizing current i_u will give an error in the current transformation of the secondary side. In order to reduce the error, voltage at the output should be very small. Another way to decrease magnetizing current is by increasing the core size. Figure 2.15 shows a circuit which minimizes current transformer output voltage and hence reduces current error.

The presented current transformer model has sufficient accuracy only for low frequency use, while for high frequency use it has to be more complicated for example in [17]. Current transformers are one of the simplest and relatively cheap solutions for current measurements but they have one major disadvantage in that they can not transform DC. Therefore, in applications that require measurements of the DC current, other techniques should be used.

2.3.3 Transformer with Hall Sensor

A simplified diagram of an open loop Hall effect current sensor is depicted in Fig. 2.16. The sensor measures DC, AC and complex current waveforms while providing galvanic isolation. The Hall effect current sensor consists of three basic components: the magnetic core, the Hall effect sensor, and signal conditioning circuitry. The Hall sensor is located in the magnetic core gap. The magnetic flux created by the primary current I_1 is concentrated in a magnetic circuit and measured in the air gap using a Hall sensor.

$$U_H = \frac{k}{d} I_C B + U_{off} \quad (2.5)$$

where: k —the Hall constant of the conducting material, d —the thickness of the sensor, I_C —constant current, B —magnetic flux density, and U_{off} is the offset voltage of the Hall generator in the absence of an external field. Such an arrangement is referred to as a Hall generator and the ratio k/dI_C is generally described as the Hall generator sensitivity. The output signal from the Hall device is then conditioned to provide an exact representation of the primary current at the output. The relation between primary current and the magnetic flux density, B , is non linear. Therefore, a magnetic core in the linear region is used. Within the linear region of the hysteresis loop of the material used for the magnetic circuit, the magnetic flux density, B , is proportional to the primary current, I_1 , and the Hall voltage, U_H , is proportional to the magnetic flux density. Therefore the output of the Hall generator is proportional

Fig. 2.16 Open loop Hall effect current sensor

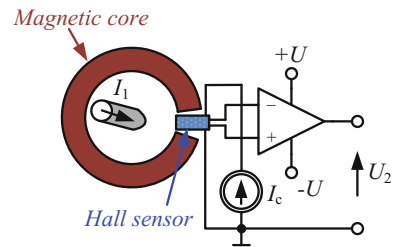
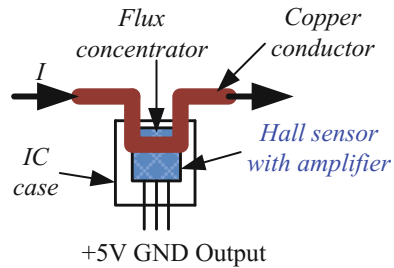


Fig. 2.17 IC current sensor from Allegro Microsystems



to the primary current, plus the Hall offset voltage, U_{off} . The advantages of open loop transducers include: low cost, small size, low weight, low power consumption and very low insertion power losses. The accuracy is limited by the combination of:

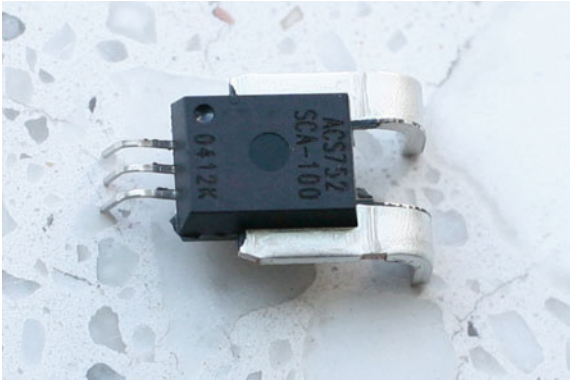
- DC offset at zero current (hall generator, electronics, or remanent magnetization (remanence) of core ferromagnetic material)
- gain error (current source, hall generator, core gap)
- linearity (core material, hall generator, electronics)
- big influence of temperature changes
- output noise
- bandwidth limitation (attenuation, phase shift, current frequency)

This type of sensor is widely used, and among the producers are: LEM Components, ABB, Honeywell, Allegro Microsystems, ChenYoung, etc. Especially noteworthy is Allegro's sensor, which is constructed in the form of a monolithic integrated circuit with flux concentrator [2, 3, 27]. A typical schematic diagram of such sensor is shown in Fig. 2.17.

An example of the fully integrated circuit is Hall effect-based linear current sensor ACS752SCA-100 from Allegro Microsystems [2], with 3 kV_{RMS} voltage isolation and a low-resistance current conductor ($130\text{ }\mu\Omega$) and single $+5\text{ V}$ supply on the secondary side. The current sensor is shown in Fig. 2.18, on the right side are two primary current terminals. The sensor has a primary sensed current range from -100 to $+100\text{ A}$, this current is converted to the output voltage signal with a sensitivity of 20 mV/A .

To reduce magnetic core and Hall sensor errors a closed loop topology was introduced. Simplified diagram of a closed loop Hall effect current sensor is depicted

Fig. 2.18 IC current sensor
ACS752SCA-100



in Fig. 2.19. In a closed loop topology, the Hall sensor drives the output amplifier current to a secondary coil, which will generate a magnetic flux to cancel the primary current magnetic flux. So the resultant flux should be equal to zero. The secondary current, which is proportional to the primary current by the secondary coil ratio, can then be measured as voltage across a sense resistor. By keeping the resultant flux in the core at zero, the errors associated with offset drift, sensitivity drift and saturation of the magnetic core will also be significantly decreased. Closed-loop Hall effect current sensors also provide the shortest response times. However, in such devices, the nominal secondary coil current from several milliamps to hundreds of milliamps, thus power consumption is much higher in closed loop Hall sensor devices than in open loop topologies. In the closed loop configuration the maximum current magnitude is limited by a finite amount of compensation current in the device. The closed loop topology is widely used, for example Lem, ABB, and this type of transducer is widespread in industrial applications, with many manufacturers now supplying it. Good examples are the above mentioned typical industrial current transducers: LA 55-P [56] from LEM Components, ESM1000 from ABB [1], CSNB121 from Honeywell [42], CYHCS-SH from ChenYoung [25], etc. Figure 2.20 shows closed

Fig. 2.19 Closed loop Hall
effect current sensor

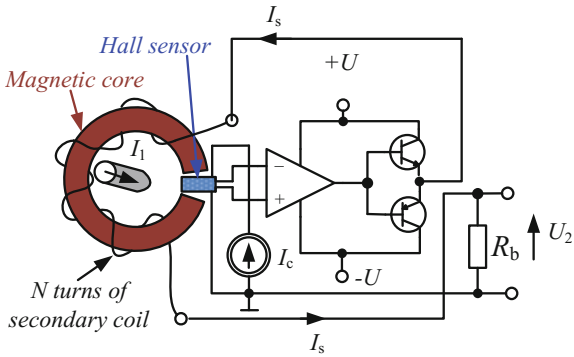
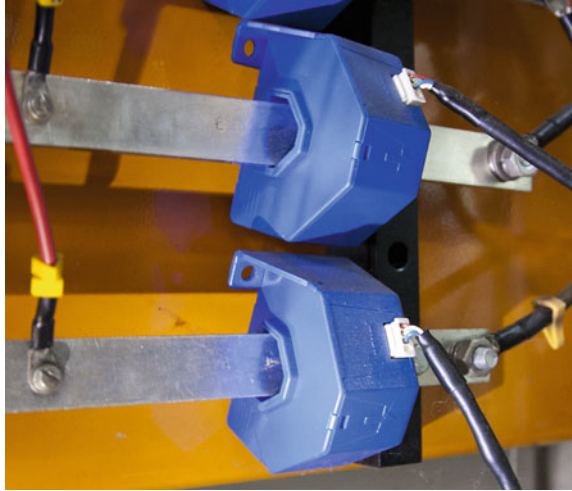


Fig. 2.20 Closed loop Hall current sensors in APF



loop Hall effect current sensors LA 205 [57] mounted on the current rail in APF EFA1 [92].

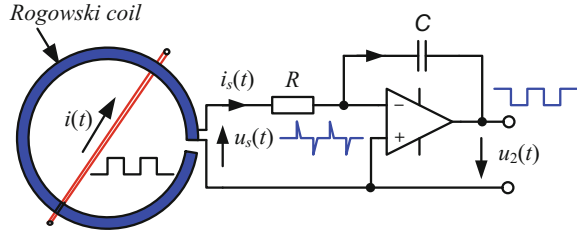
2.3.4 Current Transformer with Magnetic Modulation

Certain power electronics applications such as: medical equipment, meter or accessories for measuring equipment, require a precision current transducer. In order to eliminate the shortcomings associated with Hall effect, sensors are also developed with magnetic modulation topologies allowing the measurement of a DC component. These topologies have one, two or three magnetic cores, for example, the high precision current transducer ITB 300-S from LEM Components [80]. Features of current transformers with magnetic modulation include:

- high global accuracy,
- high linearity < 1 ppm,
- high temperature stability,
- low cross-over distortion,
- wide frequency range,
- low noise on the output signal.

2.3.5 Current Transducer with Air Coil

A Rogowski coil allows the measurement of alternating current (AC). The principle of Rogowski coil operation is well described by Ray and Davis in [76–78]. The

Fig. 2.21 Rogowski coil measurement circuit

Rogowski coil measurement circuit is depicted in Fig. 2.21. It consists of a helical coil of wire wrapped around a straight conductor whose current $i(t)$ is to be measured, since the voltage that is induced in the coil is proportional to the rate of change (derivative) of current in the straight conductor. The coil output signal is connected to an integrator circuit, so that the achieved output signal is proportional to the current. The voltage induced in the coil is given by the equation

$$u_s(t) = \mu_0 N M \frac{di(t)}{dt} = S \frac{di(t)}{dt} , \quad (2.6)$$

where: μ_0 —permeability of free space, N —turns/meter, M —cross-sectional area [m^2], S —coil sensitivity [Vs/A]. In next the stage the coil voltage is integrated by the integrator, so that transducer output voltage is

$$u_2(t) = -\frac{1}{RC} \int u_s(t) dt = -S_T i(t) , \quad (2.7)$$

Fig. 2.22 Rogowski coil in the laboratory

where: S_T —transducer sensitivity [V/A]. Rogowski coil features are:

- no magnetic saturation,
- high overload capacity,
- good linearity,
- light weight,
- low thermal losses,
- AC measurement with wide dynamic range.

Figure 2.22 shows Rogowski coil and integrator in the laboratory. The free end is normally inserted into a socket adjacent to the cable connection but can be unplugged to enable the coil to be looped around the conductor or device carrying the current to be measured. Application of an induction coil without magnetic core allows for the elimination of errors associated with non-linear magnetic material. But the lack of a magnetic field concentrator causes the measuring system to be very sensitive to

Table 2.2 Comparison of current sensing techniques

Current-sensing technique	Galvanic isolation	Accuracy	Power dissipation	Relative cost	Typical current ranges
Transformer	Yes	0.1–5%	Low-Moderate	Low	Up to 15 kA, AC
Sensing resistor	None	0.01–5% mainly depends on resistor tolerance	Moderate-High	Low	Up to 500 A, DC-100 kHz
Sensing resistor with high common mode amplifier	None	0.01–5%	Moderate-High	Low	Up to 200 A, DC-100 kHz, common voltage from –20 to 100 V
Open loop Hall effect sensor	Yes	5–10%	Low	Low	Up to 15 kA, DC-50 kHz
Closed loop Hall effect sensor	Yes	1-5%	Moderate-High	Moderate-High	Up to 15 kA, DC-200 kHz
Transformer with magnetic modulation	Yes	0.001–0.5%	High	High	Up to 700 A, DC-500 kHz
Rogowski coil—one air coil	Yes	1–2%	Low	Low	Up to 10 kA, 10 Hz–100 kHz
Two air coils	Yes	0.5–1%	Low	Low	Up to 10 kA, 10 Hz–100 kHz

external interference fields. The use of two inductive coils allows for the partial elimination of this phenomenon [55]. The induced voltages from coils are then integrated in order to obtain both amplitude and phase information for the measured current. In this solution, in comparison to the Rogowski coil, accuracy is independent of the position of the cable in the aperture and of external fields.

2.3.6 Comparison of Current Sensing Techniques

Table 2.2 presents the basic features of current transducers considered in this chapter. The discussed transducers have analog outputs, but it should be noted that currently the development of transducers with digital output are under development. They can be equipped with their own processors, allowing for compensation of some errors. Parallel to an industrial solution of current sensing techniques Hartman et al. [40] designed an alternative which consists of a wideband current transformer and a demagnetizing circuit. The sensor concept is capable of measuring AC currents with dc offset, having periodic zero crossings, as given in power-factor-corrected (PFC) circuits.

2.4 Selected Parameters of Digital Control Circuit

An example of a power electronic circuit with an open-loop multirate digital control circuit is depicted in Fig. 2.23. The circuit may be a part of the control system for DC/DC, DC/AC, AC/DC and AC/AC converters or active power filters etc. [46, 47, 89, 90]. An open system was chosen because of its simpler analysis. In the closed-loop circuit, the impact of feedback should be taken into account.

Analog input signal $x(t)$ (Fig. 2.23) is converted to digital form $x(n)$ by an A/D converter with sampling ratio f_{s1} and b_1 -bit resolution [89, 90]. In the next stage, a digital control algorithm using DSP is executed. The algorithm is calculated with b_2 -bit resolution and sampling ratio f_{s2} . Finally, output control signal $y(n)$ is transferred to a digital PWM with b_3 -bit resolution and sampling ratio f_{s3} . The PWM controls output power switches S_1 and S_2 . The switches work with switching frequency f_c . The digital PWM with two power switches S_1 and S_2 and an analog output filter L_c , C_c works as a digital-to-analog (D/A) power converter. It converts energy from a direct current source (DC) to the output. Typically the main issue is the quality of the output voltage and current. Therefore, the following signal parameters should be considered:

- f_{s1} , f_{s2} , f_{s3} —signal sampling ratios,
- b_1 , b_2 , b_3 —signal resolutions (in bits),
- f_c —transistor switching frequency,
- THD —total harmonic distortion ratio,

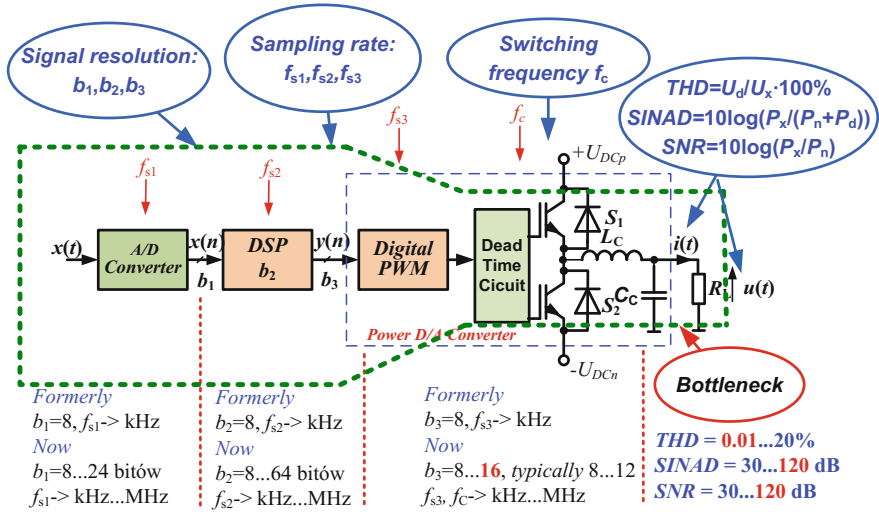


Fig. 2.23 An example of a power electronic circuit with an open-loop multirate digital control circuit

- **SNR**—output signal-to-noise ratio
- **SINAD**—output signal to noise and distortion ratio.

Finally, the required **SINAD** value of output current or voltage of power electronics circuit are dependent on the application. For example, for battery charger **SINAD** value equal to 30 dB is sufficient. However, for the high-quality audio power amplifier, the **SINAD** value should be bigger than 100 dB. As we can see the spread of parameters of digital control systems for power electronics circuits is very high. Nowadays there is a huge offer of A/D converters and DSPs, so it is easy to choose circuits with adequate parameters: b_1 , b_2 , f_{s1} and f_{s2} . The only considerable limitation may be the price of those circuits. The last stage, with digital PWM, is still a “bottleneck” of the whole system, especially for high resolution, for example, high-quality power audio amplifier with parameters: $f_{s3} = 44.1 \text{ kHz}$ and $b_3 = 16 \text{ bit}$, the clock frequency of PWM counters can be calculated using the equation

$$f_h = f_{s3} 2^{b_3} \approx 2.8 \text{ GHz} \quad (2.8)$$

The calculated value of clock frequency is too high for ordinary digital circuits, therefore, resolution of digital PWM should be reduced. However, it will result in deterioration of the signal-to-noise ratio. A solution to this problem is shown in this chapter.

2.5 Total Harmonic Distortion

Total harmonic distortion (*THD*) ratio is a form of nonlinear distortion in circuits in which harmonics (signals whose frequency is an integer multiple of the input signal) are generated. A wide class of nonlinear circuits can be described by the equation

$$y(t) = a_1x(t) + a_2x(t)^2 + a_3x(t)^3 + \cdots + a_kx(t)^k \quad (2.9)$$

In linear circuits only a_1 coefficient is nonzero. For example a nonlinear circuit described by equation $y(t) = x(t) - 0.2x(t)^3 + 0.15x(t)^5 + 0.11x(t)^7 - 0.05x(t)^9$ the response for DC input signal in the range from -1 to 1 is shown in Fig. 2.24. MATLAB[®] program for the nonlinear circuit simulation is shown in Listing 2.1.

Fig. 2.24 The static characteristics of nonlinear circuit, response for input signal range from -1 to 1

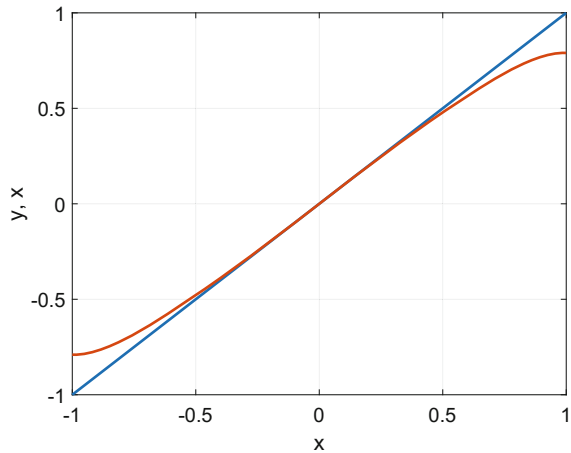
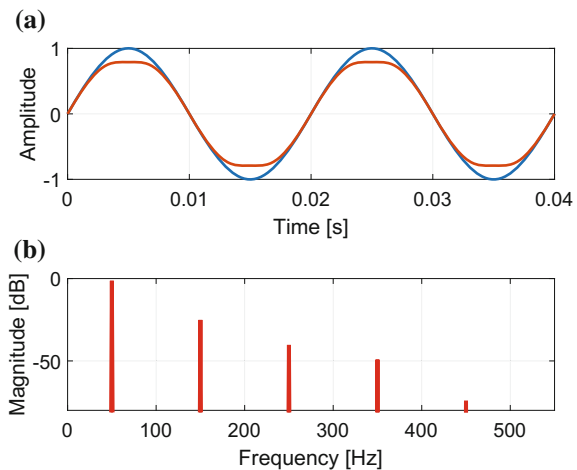


Fig. 2.25 The nonlinear circuit response for sinusoidal signal, $f = 100$ Hz: **a** the input and the output signal waveforms, **b** spectrum of the output signal



The response for unity amplitude sinusoidal signal, $f=100\text{Hz}$, is depicted in Fig. 2.25. The waveforms of input and output signal are presented in Fig. 2.25a. The output signal distortion causes generation of signal harmonics. The spectrum of the output signal is shown in Fig. 2.25b.

Listing 2.1 Nonlinear circuit

```

0  clear all; close all;
1  roz_fon=18; grub_lin=2;
2  N=2^12; % number of samples
3  fs=12800; % sampling frequency
4  f1=50; f_1k=round(f1/(fs/N))*fs/N; % line frequency
5  A1=1;
6  t=(0:N-1)/fs; % time vector
7  a=[1 0 -0.2 0 0.15 0 -0.11 0 -0.05]; % coefficients
8  %% ----- Response for DC -----
9  x=((0:N-1)/N)*2-1; % input signal -1...1
10 y=a(1)*x+a(2)*x.^2+a(3)*x.^3+a(4)*x.^4+a(5)*x.^5 + ...
11    +a(6)*x.^6+a(7)*x.^7+a(8)*x.^8+a(9)*x.^9;
12 plot(x,x,x,y,'LineWidth',grub_lin);
13     set(gca,'FontSize',[roz_fon],'FontWeight','d'),
14     xlabel('x'); ylabel('y,x'); grid on;
15 %% ----- Response for sinusoidal signal 100 Hz -----
16 x=A1*sin(2*pi*f_1k*t); % input sinusoidal signal
17 y=a(1)*x+a(2)*x.^2+a(3)*x.^3+a(4)*x.^4+a(5)*x.^5+...
18    +a(6)*x.^6+a(7)*x.^7+a(8)*x.^8+a(9)*x.^9;
19 % spectrum
20 w_y=fft(y)/N*2; w_y_dB=20*log10(abs(w_y)+eps);
21 f=(0:N-1)*fs/N;
22 subplot(211);
23     plot(t,x,t,y,'LineWidth',grub_lin); grid on;
24     set(gca,'FontSize',[roz_fon],'FontWeight','n'),
25     set(gca,'Xlim',[0 2/f_1k]); xlabel('Time-[s]');
26     ylabel('Amplitude'); title('(a)');
27 subplot(212);
28     plot(f,w_y_dB,'r','LineWidth',grub_lin+1); grid on;
29     set(gca,'Ylim',[-80 0]); set(gca,'Xlim',[0 11*f_1k]);
30     set(gca,'FontSize',[roz_fon],'FontWeight','n'),
31     xlabel('Frequency-[Hz]'); ylabel('Magnitude-[dB]');
32     title('(b)');

```

THD ratio is measured in percents or in decibels (dB), and harmonic distortion is calculated as the ratio of the level of the harmonic to the level of the original frequency

$$THD = \frac{\sqrt{\sum_{k=2}^N U_k^2}}{U_1} . \quad (2.10)$$

where: U_1 —amplitude of first (or fundamental) harmonic, U_k —amplitude of k -th harmonic, and expressed in dB

$$THD_{dB} = 20 \log \frac{\sqrt{\sum_{k=2}^N U_k^2}}{U_1} . \quad (2.11)$$

In power electronics systems other distortion factors [13, 41] are also used, one of which is weighted harmonic distortion ratio in which the importance of harmonics decreases as the frequency increases

$$WTHD = \frac{\sqrt{\sum_{k=2}^K \left(\frac{U_k}{k}\right)^2}}{U_1} . \quad (2.12)$$

2.6 Sampling of Analog Signal

Sampling is an essential part of signal processing. It enables A/D transformation of the analog signal to occur. However useful this process is, some precautions need to be taken to ensure that the output signal is not changed significantly. Therefore, while sampling the analog signal at discrete intervals, $T_s = 1/f_s$, the signal sampling frequency f_s (also called signal sampling speed) must be carefully chosen to ensure an accurate representation of the original analog signal. It is evident that the more samples are taken (faster signal sampling rates), the more accurate the digital representation is. Hence if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. The discussion in this chapter focuses on periodic and uniform sampling. An example of a sample and hold circuit (SH) (also called sampling circuit or track and hold (TH) circuit) is shown in Fig. 2.26 and an illustration of an analog sinusoidal signal sampling process is presented in Fig. 2.27.

The history of the mathematical background of sampling theory goes back to the 1920s, when it was founded by Nyquist [65, 66] of Bell Telephone Laboratories. This original work was shortly supplemented by Hartley [39] and Whittaker. These papers formed the basis for the pulse code modulation (PCM) work and were followed in 1948 by Shannon who wrote a paper on communication theory [82]. The sampling

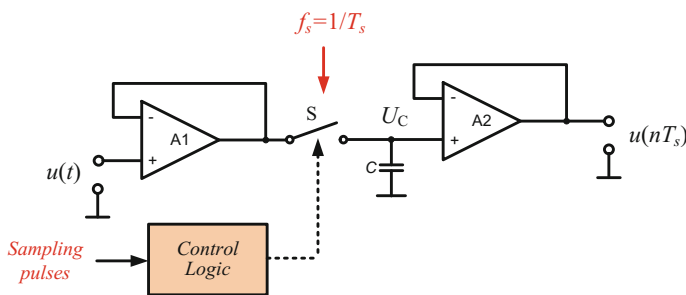
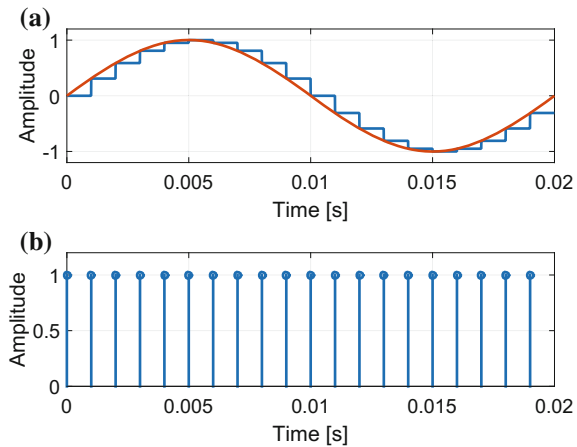


Fig. 2.26 A sampling circuit

Fig. 2.27 Illustration of analog sinusoidal signal sampling process: **a** input signal and sampled signal, **b** sampling pulses



theory was discovered independently by Kotelnikov from the Soviet Union in 1933 [51]. Simply stated, the sampling theory criteria require that the sampling frequency must be at least twice the highest frequency contained in the analog signal, otherwise the information about the analog signal will be lost. If the sampling frequency is less than twice the maximum analog signal frequency, a phenomenon known as aliasing will occur. It is a source of spurious signals occurring within the anti-aliasing filter as a result of the high signal bandwidth available in today's ADCs. The main purpose of using an anti-aliasing filter is to limit the input signal's bandwidth to eliminate high-frequency components. Therefore it is required that in data sampling systems the input signal's spectrum frequency must not exceed one-half of the sample clock frequency. An ideal anti-aliasing filter would pass all signals within the band of interest and block all signals from outside of that band. It is the quality of the anti-aliasing filter which is the major factor in the signal-to-noise ratio (SNR). The SNR typically expressed in decibel, can be determined by the Eq. 1.12.

When the half sampling frequency $f_s/2$ is only slightly higher than f_b for signal band $0 - f_b$ (as happens in the classic system), the anti-aliasing has to have very sharp amplitude characteristics and a high damping factor in the stop-band. This results in the anti-aliasing filter being very complicated and expensive. Currently, the development of integrated circuit (IC) manufacturing technology has led to the fact that fast digital circuits are freely available and cheap. Therefore, in modern systems the value of the sampling rate f_s can be much higher than f_b (this is called oversampling), so the requirements for the anti-aliasing filter are much lower. The spectra of a sampling signal process with aliasing occurrence are shown in Fig. 2.28.

The background of digital signal processing useful for A/D and D/A conversion is described by Oppenheim and Schaffer [67], Proakis and Manolakis [74], Lyons [58], Rabiner and Gold [75], Zolzer [110, 111] and many others [14, 35, 37, 38, 43, 53, 54, 106]. Some interesting technical problems with A/D conversion are described in Data Translation [31, 32] and Analog Devices [48–50] (by Kester) technical reports and

Fig. 2.28 Impact of aliasing on the signal dynamics

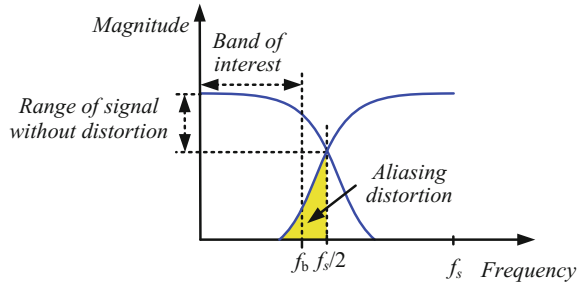
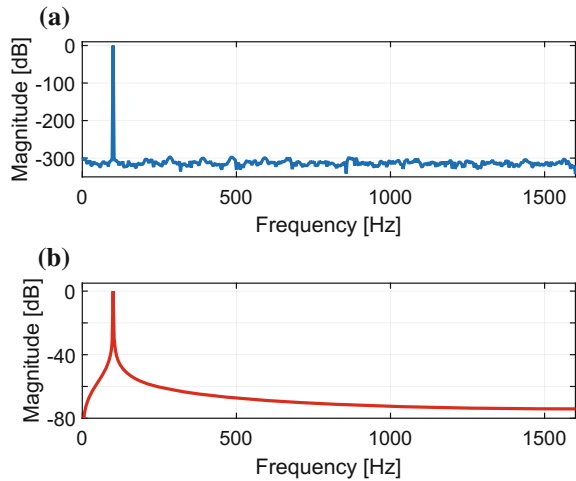


Fig. 2.29 Spectra of sinusoidal signals:
a coherent sampling,
b non-coherent sampling



books. Other problems about signal oversampling and signal sampling rate changes are discussed in Chap. 3.

2.6.1 Synchronization of Sampling Process

The properties of the majority of digital signal processing algorithms (e.g. DFT) to a large extent depend on whether the processed signal is sampled coherently [90]. Coherent sampling refers to a certain relationship between input frequency, f_{in} , sampling frequency f_s , N_{per} —integer number of signal periods in block of N signal samples

$$f_s = N_{per} \frac{f_{in}}{N} . \quad (2.13)$$

With coherent sampling one is assured that the signal magnitude in an DFT is contained within one DFT bin, assuming single input frequency. For example, Fig. 2.29

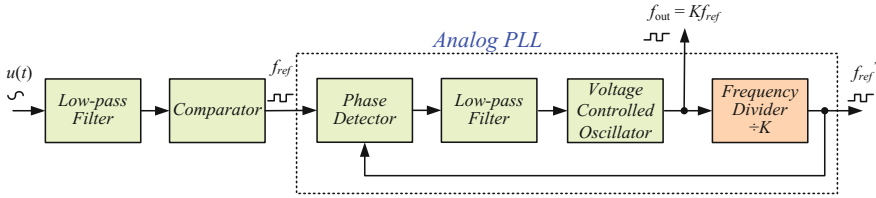


Fig. 2.30 Analog synchronization circuit with PLL

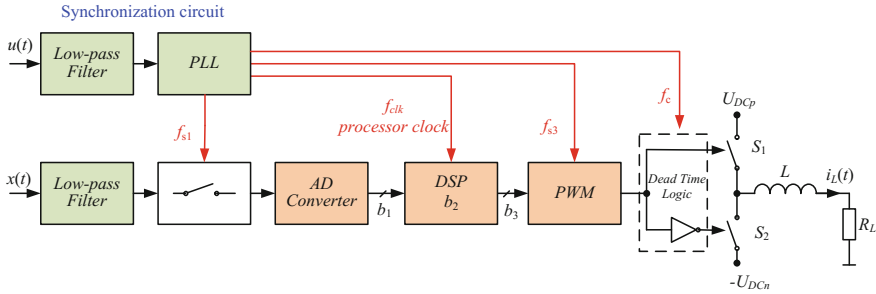


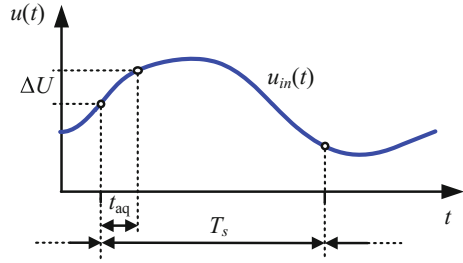
Fig. 2.31 Full synchronized control circuit

shows the spectrum of the same signal with coherent sampling (Fig. 2.29a) and non-coherent sampling (Fig. 2.29b). Therefore, in the author's opinion, for systems connected to the power network it is expedient to use synchronization.

In Fig. 2.30 a block diagram of an analog phase-locked-loop (PLL) circuit is depicted. Using this circuit it is possible to generate signal with frequency K times bigger than input frequency. A PLL circuit can track a reference frequency and it can generate a frequency that is a multiple of the input frequency. The phase of both signals are synchronized too. The PLL generates output signal with frequency

$$f_{out} = K f_{ref} \quad , \quad (2.14)$$

where: f_{ref} —reference input frequency, K —integer frequency multiplication factor. While designing the analog synchronization circuit, the output of the power electronic device should be taken into consideration. In most cases it is a pulse width modulator (PWM) generating pulse controlled output switches (typically transistors). When the modulation frequency is independent of the reference system frequency (e.g., power line frequency), it will certainly result in generation of low frequency components. This is an effect of the beat frequency between the reference and modulation frequency. Hence, in the author's opinion, the input and output should be synchronized, which will minimize errors and eliminate unwanted components. The block diagram of such a solution is depicted in Fig. 2.31.

Fig. 2.32 Signal acquisition process

In the author's opinion, the same situation occurs during simulation tests, and if it is possible a coherent frequency of test signals should be used. A simple listing of the MATLAB program for coherent frequency calculation is shown in Listing 2.2.

Listing 2.2 Coherent frequency calculation

```

1  N=2048;      % length of signal block
2  fs=10000;    % sampling frequency
3  f=50;        % required frequency of the signal
4  f_koh=round(f/(fs/N))*fs/N; % nearest coherent frequency

```

2.6.2 Maximum Signal Frequency Versus Signal Acquisition Time

The signal acquisition time is the time required by the circuit to settle to its final value after it is paced in the hold mode. Signal acquisition time t_{aq} relates to A/D converters which use a sample-and-hold (or track-and-hold) circuit on the input to acquire and hold (to a specified tolerance) the analog input signal, see Brannon and Barlow [19]. For an A/D converter without a sample-and-hold circuit on the input, the signal acquisition time is equal to the converter conversion time t_c . The only exception concerns flash converters with well matched comparators. An illustration of a sampling process is shown in Fig. 2.32, assuming that the amplitude of the input signal in the acquisition process does not change more than half of the LSB of the A/D converter. Assuming maximum signal change during sampling process

$$\Delta U \leq 0.5\Delta = 0.5 \frac{A_p}{2^{b-1}} = \frac{A_p}{2^b} \quad . \quad (2.15)$$

The analog input sinusoidal signal with amplitude A_p and frequency f

$$u_{in}(t) = A_p \sin(2\pi f t) \quad . \quad (2.16)$$

The maximum speed of the signal change is determined by the equation

$$\left. \frac{du_{in}(t)}{dt} \right|_{max} = 2\pi A_p f \quad . \quad (2.17)$$

Assuming that

$$t_{aq} \ll 1/f \quad . \quad (2.18)$$

ΔU_{in} can be determined from

$$\Delta U_{in} = 2\pi A_p f t_{aq} \quad . \quad (2.19)$$

As a result of a straightforward algebraic manipulation we obtain an equation describing the maximum signal frequency

$$\Delta U_{in} \leq \Delta U \quad , \quad (2.20)$$

$$2\pi A_p f t_{aq} \leq \frac{A_p}{2^b} \quad , \quad (2.21)$$

$$f \leq \frac{1}{2\pi 2^b t_{aq}} \quad , \quad (2.22)$$

2.6.2.1 Example—Acquisition Time

With maximum signal frequency for a number of bits $b = 16$, acquisition time $t_{aq} = 10$ ns, and determined from the above inequality the maximum signal frequency is $f < 242.8$ Hz. As explained, this is one of the most important factors in the A/D conversion.

Using the A/D converter with a very small value of acquisition time meeting the requirements of Eq. 2.22 is very difficult and expensive. Therefore systems are used where the acquisition time is much greater. Of course, in a single channel system, there will be differences in the signal sampling moment, and often the requirements of Eq. 2.22 can be omitted. However, in such a case, in multi-channel systems it is vital to provide the same value of acquisition time for all channels.

2.6.3 Errors in Multichannel System

In multichannel systems it is very important that the input signals are simultaneously sampled to reduce amplitude and phase errors. Multichannel A/D converters with a sampling circuit have three very common architectures, which are depicted in a two channel version in Fig. 2.33. Among the three presented solutions the two use simultaneous sampling (Fig. 2.33a, b) and the other uses sequential sampling

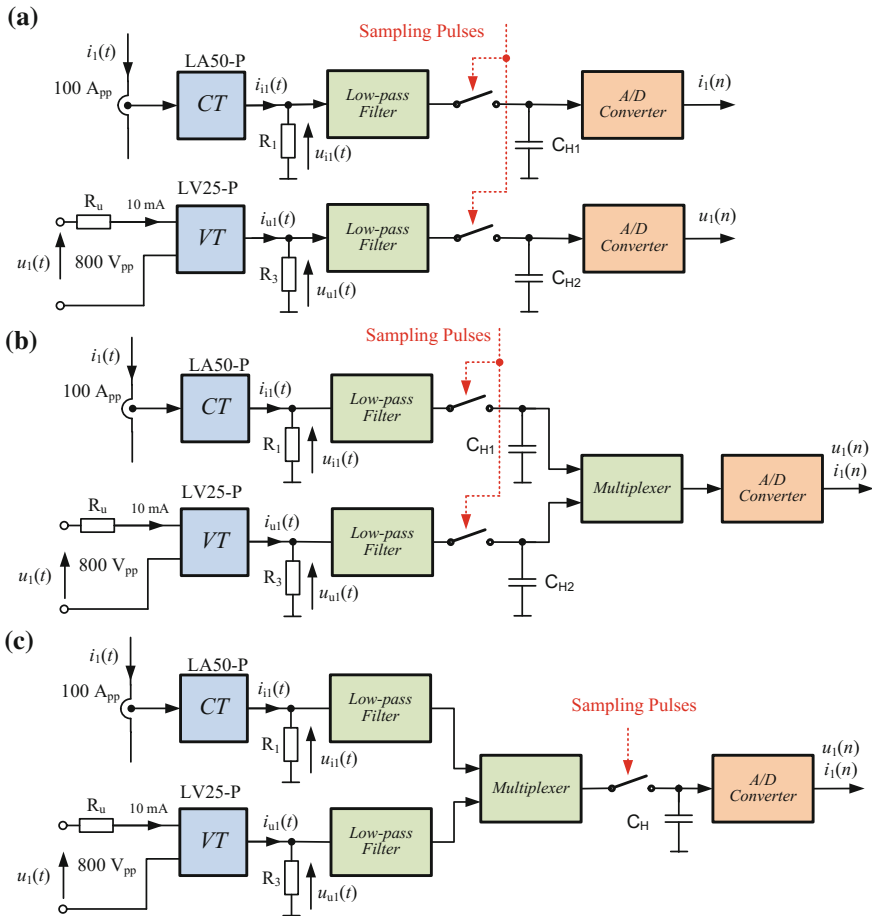
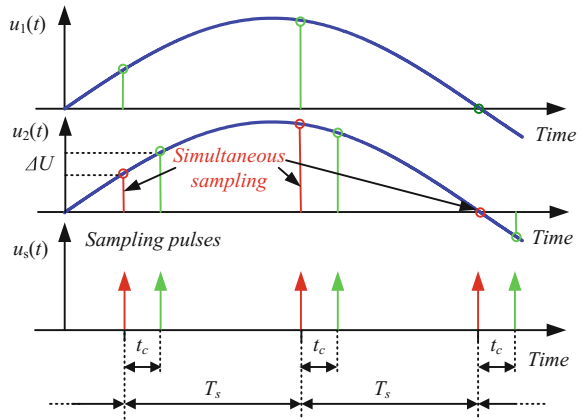


Fig. 2.33 Two-channel sampling circuits: **a** simultaneous sampling with A/D converter in each channel, **b** simultaneous sampling with single A/D, **c** sequential sampling

(Fig. 2.33c). A two-channel sequentially sampling analog-to-digital converter is depicted in Fig. 2.33a. In this circuit current $i_1(t)$ is converted to a current signal $i_{i1}(t)$ using galvanically isolated current transducer CT, and in the same way a voltage signal using galvanically isolated voltage transducer VT is processed. Then the signals pass through anti-aliasing low-pass filters and are simultaneously sampled. After this the A/D converters process and convert them to digital form. This solution is the fastest and the most comfortable for control circuit designers, however, it is also the most expensive. An alternative solution is a system with a single A/D converter with a few simultaneous sample-and-hold circuits. A block diagram of such a solution for the two channels is shown in Fig. 2.33b.

Fig. 2.34 Sequential and simultaneous sampling of two-channel sampling circuit



In comparison to the previous solution, this circuit is the simplest and hence can be cheaper. However, the errors associated with different capacitor hold times in sample-and-hold circuits will appear and deteriorate the accuracy of the system. The third circuit uses only one sampling circuit and A/D converter for all channels (Fig. 2.33c). The main disadvantage of a sequentially sampling A/D converter is the time error between channel samples. An illustration of this phenomenon is shown in Fig. 2.34, where two sample signals in time misalignment are shown. Discussion of simultaneous sampling vs. sequential sampling is found for example in Data Translation reports [31, 32]. In the author's opinion the best solution is a simultaneously sampling A/D converter, however, if it cannot be applied, the sequentially sampling A/D converter with time alignment has to be used. The benefits of simultaneous sampling compared to sequential sampling include:

- less jitter error,
- higher bandwidth of the system,
- less channel-to-channel crosstalk,
- less settling time.

2.6.4 Amplitude and Phase Errors of Sequential Sampling A/D Conversion

Due to the fact that typical A/D converters built-in microprocessor or separate IC allow only sequential sampling. Therefore errors in such a solution will be considered. Two sinusoidal input signals with the same frequency f and A_p amplitude

$$u_1(t) = A_p \sin(2\pi f t) \quad , \quad u_2(t) = A_p \sin(2\pi f (t + t_c)) \quad . \quad (2.23)$$

Difference of signals for sequential sampling with time difference t_c (Fig. 2.34)

$$\begin{aligned}\Delta U(t) &= u_1(t) - u_2(t) = 2A_p \cos\left(\frac{2\pi f t + 2\pi f(t + t_c)}{2}\right) \sin\left(\frac{2\pi f t - 2\pi f(t + t_c)}{2}\right) \\ &= 2A_p \cos(2\pi f t + \pi f t_c) \sin(-\pi f t_c) .\end{aligned}\quad (2.24)$$

Maximum of $\Delta U(t)$ is when derivative is equal zero

$$\frac{du(t)}{dt} = 4A_p \pi f \sin(2\pi f t + \pi f t_c) \sin(\pi f t_c) = 0 . \quad (2.25)$$

So the derivative is zero when

$$2\pi f t + \pi f t_c = 0 \rightarrow t = -0.5t_c . \quad (2.26)$$

Maximum value of signal error can be calculated by the formula

$$\begin{aligned}\Delta U_{max} &= \Delta U(t)|_{t=-0.5t_c} = 2A_p \cos\left(\frac{2\pi f(-0.5t_c) + 2\pi f t_c}{2}\right) \sin(-\pi f t_c) \\ &= 2A_p \cos(0) \sin(-\pi f t_c) \\ &= 2A_p \sin(-\pi f t_c) .\end{aligned}\quad (2.27)$$

However, phase error can be determined from the equation

$$\Delta\phi = \frac{t_1}{T} 360 - \frac{t_1 - t_c}{T} 360 = 360 t_c f . \quad (2.28)$$

2.6.4.1 Example—Sequential Sampling

With maximum signal frequency for sequential sampling for an A/D conversion time $t_c = 5 \mu\text{s}$, signal amplitude $A_p = 1$ and signal frequency $f = 50 \text{ Hz}$ it is possible to determine from the above equation: maximum signal error is $\Delta U = 1.57 \text{ mV}$, phase error $\Delta\phi = 0.09$, and results for the 50th harmonics ($f = 2500 \text{ Hz}$): $\Delta U = 39.26 \text{ mV}$ and $\Delta\phi = 4.5$. The result will be worse in multichannel systems with sequential sampling, where the A/D conversion time t_c for the last channel will be multiplied by the number of channels.

For b -bit system signal error should be less than

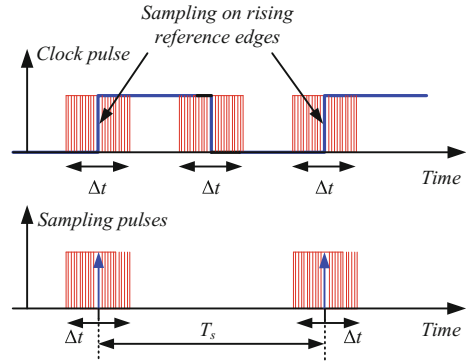
$$\begin{aligned}|\Delta U_{max}| &\leq 0.5\Delta , \\ 2A_p \sin(\pi f t_c) &\leq \frac{A_p}{2^b} ,\end{aligned}\quad (2.29)$$

Assuming

$$t_c \ll 1/f . \quad (2.30)$$

Finally

Fig. 2.35 Sampling clock with jitter



$$t_c \leq \frac{1}{\pi f 2^{b+1}} \quad (2.31)$$

The result is similar to the one obtained in Sect. 2.6.2.

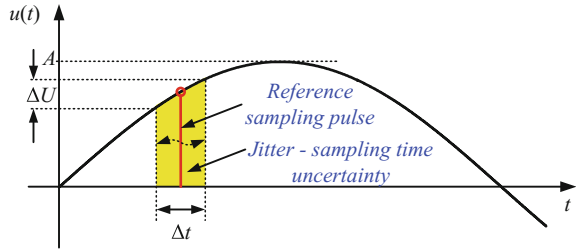
Another source of errors in multi-channel systems are the channel crosstalk and channel-to-channel offset. Channel-to-channel offset is the difference in the characteristics of analog input channels which causes measurement error, as if small voltage were added to or subtracted from the input signal. Channel crosstalk is the leakage of signals between analog input channels in a data acquisition system. Channel crosstalk has the potential to increase uncorrelated noise in the A/D conversions, reducing the signal to noise ratio (*SNR*), while coupled signals can create spurs similar to harmonic terms, reducing spurious free dynamic range (*SFDR*) and total harmonic distortion (*THD*).

2.6.5 Sampling Clock Jitter

An important factor in the sampling process is the sampling clock in the A/D converter. Due to hardware error and noise the sampling moments in real A/D converters are uncertain. Problems of sampling signal uncertainty are described by many authors [12, 18, 19, 62, 79, 90]. Variation in the sampling time is known as aperture uncertainty, or jitter, and will result in an error voltage that is proportional to the magnitude of the jitter and the input signal slew rate. In other words, the greater the input frequency and amplitude, the more susceptibility to jitter in the clock source. Figure 2.35 shows a sampling pulse clock with jitter.

Figure 2.36 shows how jitter generates a signal error.

$$\Delta U = \Delta t \frac{du(t)}{dt} \quad (2.32)$$

Fig. 2.36 Sampling time uncertainty—jitter

The maximum value of voltage error for sinewave of frequency f and amplitude A is at zero crossing

$$\Delta U_{max} = \Delta t \left. \frac{du(t)}{dt} \right|_{max} = 2\pi f A \Delta t \quad . \quad (2.33)$$

This error cannot be corrected later because it is already attached to the sampling sequence that is being processed for digitization and will impact the overall performance of the A/D converter and finally of the control system, as shown in Eq. 2.33. Assuming that

$$\Delta U_{max} < 0.5\Delta \quad , \quad \Delta U_{max} < \frac{A}{2^b} \quad . \quad (2.34)$$

then

$$\Delta t < \frac{1}{2\pi f 2^b} \quad . \quad (2.35)$$

Finally

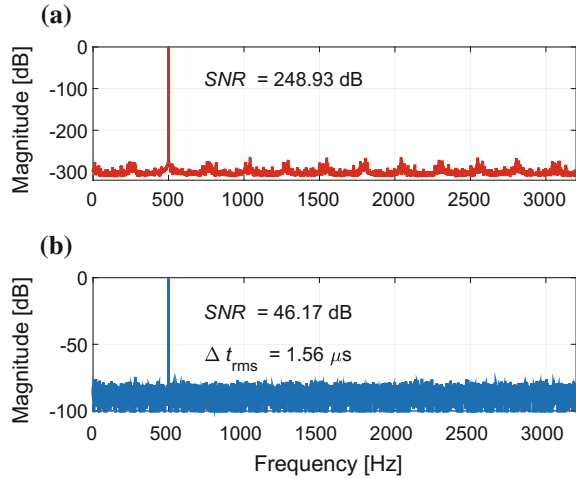
$$SNR_{jitter} = -20 \log(2\pi f \Delta t_{rms}) \quad , \quad (2.36)$$

where: t_{rms} —root means square of time jitter.

2.6.5.1 Example—Jitter

This case illustrates deterioration of signal quality by jitter. Assuming the following parameters: sampling frequency $f_s = 6400$ Hz, signal frequency $f = 500$ Hz, jitter value $\Delta t_{rms} = 1.57 \mu s$, signal-to-noise ratio SNR the value calculated from the formula 2.36 is equal to $SNR = 46.18$ dB. For such assumed values a simulation in the MATLAB environment was also made. In Fig. 2.37 the results of the simulation are shown. The spectrum presented in Fig. 2.37a is for sinusoidal signal, which was coherently sampled without jitter, the $SNR = 248.93$ dB of this signal is only limited by the MATLAB arithmetic accuracy. The spectrum of signal sampled with jitter is shown in Fig. 2.37b. In this case the value of signal-to-noise ratio calculated on the basis of simulation is equal to $SNR = 46.17$ dB and it is almost equal to the value

Fig. 2.37 Spectra of coherent sampled signals: break **a** without jitter, **b** with jitter



calculated by formula 2.36. The MATLAB program for calculation this example is described in Listing 2.3.

Listing 2.3 The jitter calculation

```

1  clear all; close all;
2  N=2^14; fs=6400; Ts=1/fs; font=10;
3  f=500; fkoh=round(f/(fs/N))*fs/N; %koherent signal frequency
4  t=(0:N-1)*Ts; A_jitter=0.01*Ts;
5  tjitter=randn(1,N)*A_jitter; % normal (or Gaussian) distribution
6  A_jitter_rms=(sum(tjitter.^2)/N)^0.5; % RMS value of jiitter
7  SNR_calc=-20*log10(A_jitter_rms*2*pi*fkoh); % SNR from equation
8  wej_jitter=1.0*sin(2*pi*fkoh*(t+tjitter)); % signal with jitter
9  wej=1.0*sin(2*pi*fkoh*t); % signal without jitter
10 w_wej=fft(wwej)/N*2; w_wej_jitter=fft(wwej_jitter)/N*2;
11 w_wej_dB=20*log10(abs(w_wej)+eps);
12 w_wej_jitter_dB=20*log10(abs(w_wej_jitter)+eps);
13 f=(0:N-1)*fs/N;
14 %% SNR from spectrum
15 n=round(fkoh/(fs/N)); % find number of signal bin
16 SNR=20*log10((sum(abs(w_wej([1:n, n+2:(N/2-1)]).^2)))^0.5);
17 C = num2str(-SNR, '%3.2f');
18 SNR_jitter=-20*log10((sum(abs(w_wej_jitter([1:n, n+2:(N/2-1)]).^2)))^0.5);
19 A = num2str(SNR_jitter, '%3.2f'); B = num2str(SNR_calc, '%3.2f');
20 figure('Name','Spectra','NumberTitle','off')
21 subplot(211), plot(f,w_wej_dB,'r','linewidth',2); grid on;
22 set(gca,'fontSize',font); title('(a)'); ylabel('Magnitude_[dB]');
23 axis([0 fs/2 -320 0]);
24 text(700,-75,['\it{SNR}_{rm}=',C,'_dB'], 'FontSize',font);
25 subplot(212), plot(f,w_wej_jitter_dB,'r','linewidth',2); grid on;
26 set(gca,'fontSize',10); title('(b)'); ylabel('Magnitude_[dB]');
27 xlabel('Frequency_[Hz]'); axis([0 fs/2 -100 0]);
28 text(700,-15,['\it{SNR}_{rm}=',A,'_dB'], 'FontSize',font);
29 text(700,-35,['\it{SNR}_{calc}=',B,'_dB'], 'FontSize',font);

```

```

30 D = num2str(A_jitter_rms*1e6,'%3.2f');
31 text(700,-60,['\it\Delta_t\rm_{rms}=\ ',D,'_\mus'], 'FontSize',font);
32 print('jitter_matlab.pdf','-dpdf');

```

2.7 Signal Quantization

In the process of A/D conversion the amplitude resolution of digital signal is limited to digital representation. In most cases the b -bit fixed-point system is used, which eliminates the excess of digits by discarding them or by rounding off the number. An illustration of the sampling and quantization process of a sinusoidal analog signal is shown in Fig. 2.38.

In Fig. 2.39 spectra of quantized analog sinusoidal signals are shown, for $f = 700\text{Hz}$, $f_s = 12800\text{Hz}$, $b = 7$ bit (Fig. 2.39a) and $b = 14$ bit (Fig. 2.39b).

The digital signal is a sequence of numbers in which each number is represented by a finite number of digits

$$x(n) \longleftrightarrow x(nT_s), \quad -\infty < n < \infty, \quad (2.37)$$

where: n —number of samples, $x(n)$ discrete signal obtained by sampling of analog signal $x(t)$ every T_s period of time. The amplitude of the signal corresponding to the least significant bit (LSB) is determined by the equation

Fig. 2.38 Analog sinusoidal signal sampling and quantization process: **a** input signal and sampled signal, **b** sampling pulses

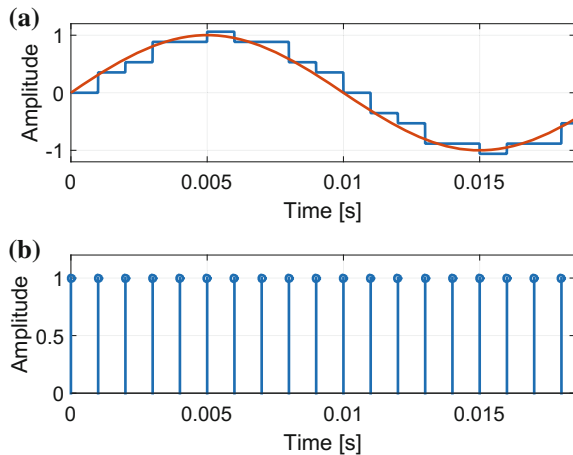


Fig. 2.39 Spectra of quantized analog sinusoidal signals: **a** for $b = 7$ bit, **b** for $b = 14$ bit

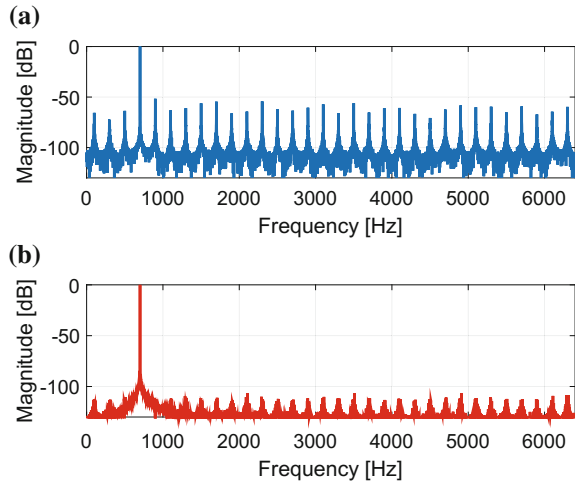
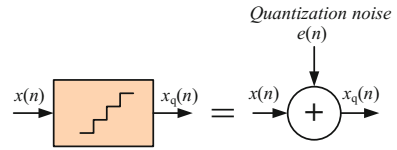


Fig. 2.40 The additive linear model of quantization process



$$\Delta = \frac{A_p}{2^{b-1}} \quad , \quad (2.38)$$

where: A_p —maximum amplitude of converted signal. The Δ is also called quantization step size and resolution. The additive linear model of quantization process is shown in Fig. 2.40.

The quantization error is defined by equation

$$e_q(n) = x_q(n) - x(n) \quad , \quad (2.39)$$

$e_q(n)$ in the rounding quantization process is limited to the range of $-\Delta/2$ to $\Delta/2$, that is

$$-\frac{\Delta}{2} \leq e_q(n) \leq \frac{\Delta}{2} \quad , \quad (2.40)$$

Signal quantization adds noise to the signal, which deteriorates the signal dynamic range. For a sinusoidal signal and quantization noise, which are uniformly distributed, in fixed-point b -bit system, the noise power can be calculated by

$$P_n = \frac{\Delta^2}{12} \quad . \quad (2.41)$$

When a full-scale sine-wave is used as the input signal, SNR can be written as

$$SNR = 10 \log \left(\frac{P_x}{P_n} \right) = 10 \log \left(\frac{\frac{A_p^2}{2}}{\frac{\Delta^2}{12}} \right) = 10 \log \left(\frac{3}{2} 2^{2b} \right) \cong 1.76 + 6.02b \quad . \quad (2.42)$$

2.7.1 Dynamic Range of Signal

The dynamic range of a signal processing system can be defined as the ratio of the maximum sustainable signal level without overflow (or other distortion) to minimum signal level

$$DR = 20 \log \left(\frac{|X_{max}|}{|X_{min}|} \right) \quad . \quad (2.43)$$

where: $|X_{max}|$ —maximum amplitude of the signal (in digital systems typically the most significant bit, MSB, is used), $|X_{min}|$ —minimum amplitude of the signal (least significant bit, LSB, in digital systems).

2.7.2 Signal Headroom

The SNR value from Eq. (2.42) is only possible when the signal amplitude is equal to A_p ; in practice it is not possible to work with such high amplitude. It is therefore necessary to leave an adequate margin to exceed the value of the signal and additional space for the signal pulse components called signal headroom. Figure 2.41 shows an illustration of this phenomenon, where A_{p1} is nominal amplitude of the input signal, and A_{p2} is an extended amplitude of the input signal.

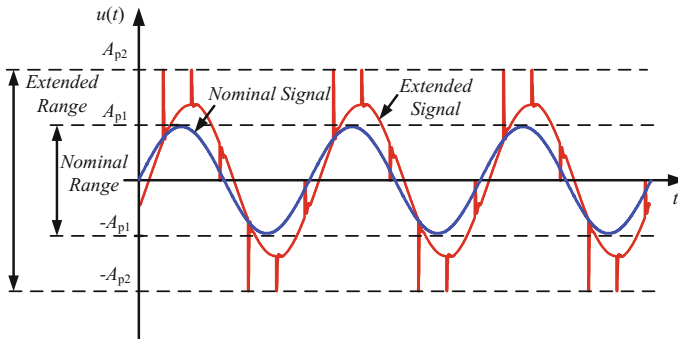


Fig. 2.41 Signal headroom

Therefore, in real systems, the value of SNR will be lower than is apparent from the number of A/D converter bits and can be calculated by the formula

$$\begin{aligned}
 SNR &= 10 \log \left(\frac{\frac{A_{p1}^2}{2}}{\frac{\Delta^2}{12}} \right) = 10 \log \left(\frac{\frac{A_{p1}^2}{2}}{\frac{A_{p2}^2}{\frac{2^{2b-1}}{12}}} \right) \\
 &= 10 \log \left(\left(\frac{A_{p1}}{A_{p2}} \right)^2 \frac{3}{2} 2^{2b} \right) \\
 &\cong 1.76 + 6.02b + 20 \log \left(\frac{A_{p1}}{A_{p2}} \right) .
 \end{aligned} \tag{2.44}$$

2.7.2.1 Example—Signal Headroom

A 12-bit A/D converter is used for measuring load current in a shunt switching compensator (active power filter) circuit for maximal value of load current equal to 100 A. Theoretically for a typical 12-bit A/D converter it is possible to achieve $SNR \approx 72$ dB. Practically, with 30% signal headroom we can achieve $SNR \approx 69$ dB. The situation can be even worse if the value of the load current is less. For example, if the load current is equal to 20 A then $SNR \approx 58$ dB.

2.7.3 Noise Shaping Technique

Figure 2.42 shows the spectra for the different methods of D/A conversion. The spectrum of the classical method of D/A conversion is shown in Fig. 2.42a. In the assumed model of quantization noise, spectral density is constant throughout the band 0 to f_b . By using oversampling, the noise power in band 0 to f_b can be determined from the expression

$$P_{nb} = P_n \frac{2f_b}{f_s} , \tag{2.45}$$

where: P_n —noise power in band 0 to $f_s/2$.

Therefore, for D/A conversion with oversampling, the expression for the signal-to-noise ratio (2.42) can be modified to form

$$SNR = 1.76 + 6.02b + 10 \log \frac{f_s}{2f_b} . \tag{2.46}$$

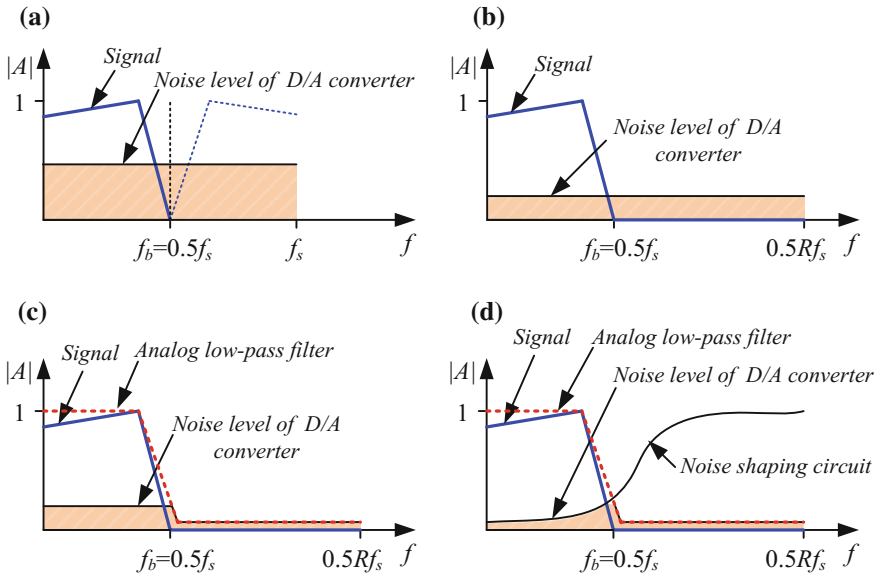


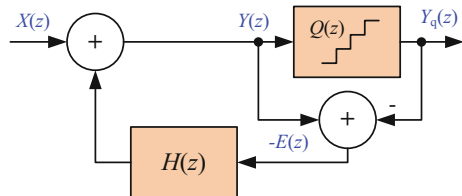
Fig. 2.42 Spectra of D/A conversions: **a** classical method, **b** method with oversampling, **c** method with oversampling and analog filter, **d** method with oversampling, analog filter and noise shaping circuit

Doubling the sampling rate increases the signal to noise ratio by 3 dB.

Out-of-band noise can be suppressed by the output analog low-pass filter as shown in Fig. 2.42c. Further increasing the signal to noise ratio can be achieved by the use of the digital noise shaping circuit. With this solution, the noise is moved outside the band of interest. The spectrum of such a solution is shown in Fig. 2.42d.

The noise shaping circuit works by putting the quantization error in a feedback loop. Different circuit architectures can be used for spectral shaping of the quantization noise, i.e., for moving it away from the band of interest toward higher frequencies [21]. Noise shaping circuits with feedback were first presented by Cutler [28] in 1954, and their detailed analysis was done by Spang and Schultheiss [91]. A block diagram of a quantization noise shaping circuit using a linear quantizer model with feedback [91, 103] is shown in Fig. 2.43. Output signal can be calculated as

Fig. 2.43 Noise shaping circuit



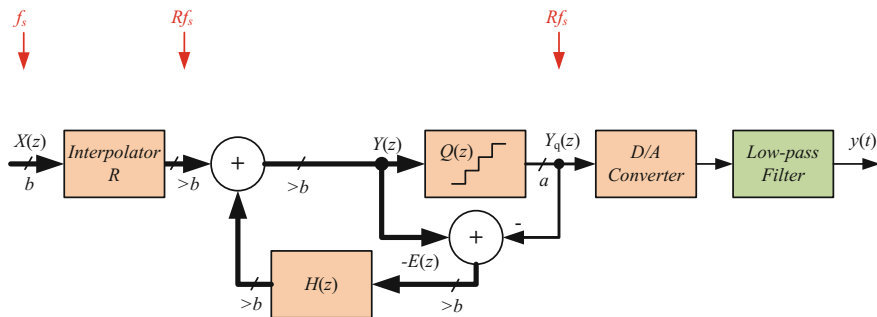


Fig. 2.44 D/A converter with oversampling and noise shaping

$$Y(z) = X(z) - H(z)E(z) \quad , \quad (2.47)$$

and quantization error is calculated from

$$-E(z) = Y(z) - Y_q(z) \quad . \quad (2.48)$$

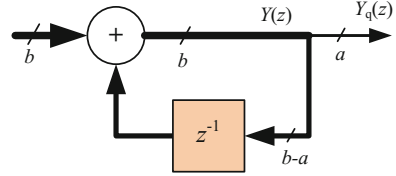
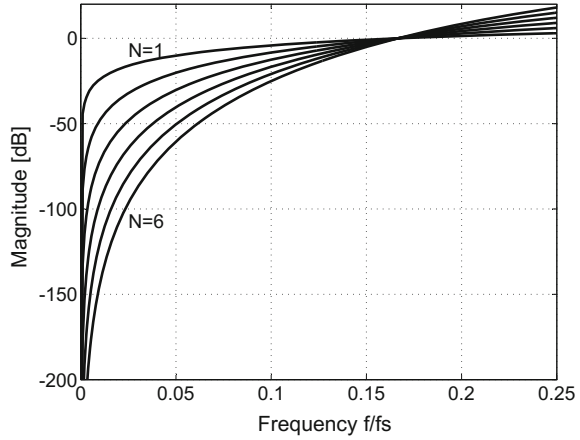
Finally the output quantized signal is calculated by formula

$$Y_q(z) = X(z) - \overbrace{(1 + H(z))}^{H_n(z)} E(z) = X(z)H_s(z) + E(z)H_n(z) \quad , \quad (2.49)$$

where: $H_s(z) = 1$ —transfer function for signal, $H_n(z) = 1 - H(z)$ —transfer function for noise. A properly designed circuit with noise shaping has flat frequency response $H_s(z)$ in the signal frequency. On the other hand, $H_n(z)$ should have high attenuation in the frequency band of interest and a low attenuation in the rest of the band. For a low oversampling ratio R , an efficient way to increase the signal to noise ratio is by using a second-order loop filter.

A block diagram of the processing of b -bit digital signal $X(z)$ of the sampling rate f_s by means of a -bit D/A converter to the analog signal is shown in Fig. 2.44. Digital input signal $X(z)$ with a resolution of b -bit is interpolated by a factor of R , and produces a signal with a resolution of b -bit or more. For example, for the SHARC digital signal processor has 32/40-bits resolution. Then the resolution of the signal is reduced to a -bits and the difference of signals $Y(z)$ and $Y_q(z)$ is transformed by a system of noise shaping transfer function $H(z)$.

In the simplest case, $H(z) = z^{-1}$ is only delay, to the input signal $X(z)$ is added to this portion of the signal, which has not been processed in the previous cycle. A block diagram of such a system, with the b -bit input samples the D/A converter converts only the oldest a -bits, and the remaining bits are added to the next sample, as shown in Fig. 2.45. The transfer function of the noise $H_n(z)$ in the simplest case can be the FIR (Finite Impulse Response) filter and the N -th order is defined by the equation

Fig. 2.45 Simplest noise shaping circuit**Fig. 2.46** Frequency characteristics of noise shaping circuits

$$H_n(z) = (1 - z^{-1})^N \quad (2.50)$$

The frequency characteristics of noise attenuation of the noise shaping circuits described by the above Eq.(2.50) for the orders $N=1-6$ is shown in Fig. 2.46. Figure 2.47 shows the block diagrams of noise shaping circuits of the first and second order. In order to prevent overflow of numbers in circuits amplitude limiters are introduced.

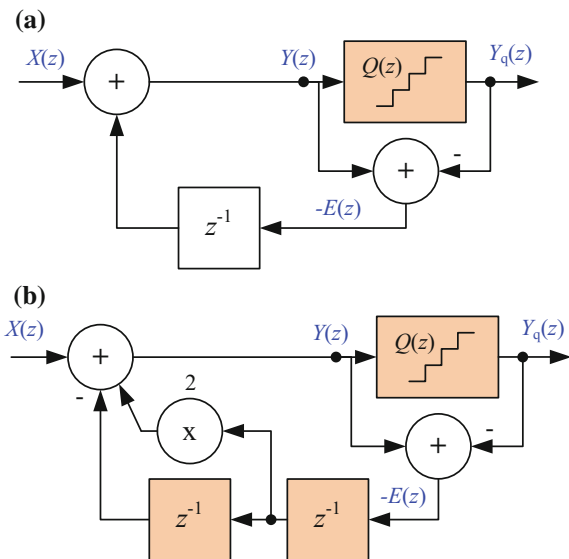
The presented noise shaping method is one of several techniques, another example is the commonly used the delta-sigma modulator [22, 23, 64, 71, 81]. The author has applied the noise shaping circuit for high quality digital class-D audio amplifier [85, 88].

The noise shaping technique for D/A conversion shown in this section can be also used for A/D conversion.

2.7.4 Dither

The resolution of A/D and D/A conversion can be increased by adding to the input signal a low-level noise signal; this signal is called a dither [64, 68, 71, 81, 85]. It is an intentionally applied form of noise signal used to randomize quantization error.

Fig. 2.47 Noise shaping circuits: **a** first order, **b** second order



Dither is routinely used in the processing of both digital audio and digital video data, and is often one of the last stages of audio production of compact discs. Figure 2.48a shows circuit with analog dither added before the A/D converter, but after the SH circuit. Similarly, a digital dither signal may be used to improve the D/A conversion as shown in Fig. 2.48. It can also be successfully used in power electronics systems. The amplitude of this signal must be small in order to avoid reduction of the dynamic range of the signal. The author's research shows that it should have an amplitude in the range from 0.5 to 2LSB [85]. Figure 2.49 depicts a simple digital circuit where dither $D(z)$ signal is added to input signal $X(z)$ before its quantization. Application of a dither signal can also improve the performance of the noise shaping circuit as shown in Fig. 2.50a. A pseudorandom signal is added outside the loop feedback, so that it will not be followed by the tracking loop. Simulation studies carried out by the author [85] shows that the optimum pseudorandom signal amplitude in terms of obtaining the greatest signal to noise ratio $SINAD$ is about 0.3LSB. The amplitude of the random signal to be added is so small due to the fact that noise shaping circuit has a feedback loop that reduces the size of the quantization step.

Adding to the input signal pseudorandom signal degrades SNR , therefore it would be beneficial to change the amplitude depending on the amplitude of the input signal. For input signals with large amplitudes, the amplitude of the random signal is reduced. The block diagram of such a circuit is shown in Fig. 2.50b. The amplitude of the random signal $d(nT)$ can be modulated depending on the input module [63] according to the equation

$$d_m(nT_s) = (1 - \sqrt{|x(nT_s)|})^2 d(nT_s) \quad . \quad (2.51)$$

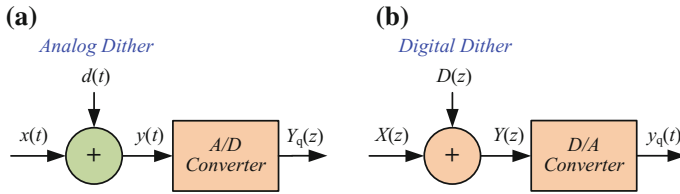


Fig. 2.48 Dither circuits: **a** the A/D conversion, **b** the D/A conversion

Fig. 2.49 Digital dither circuit

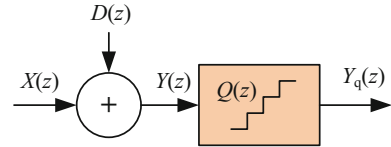
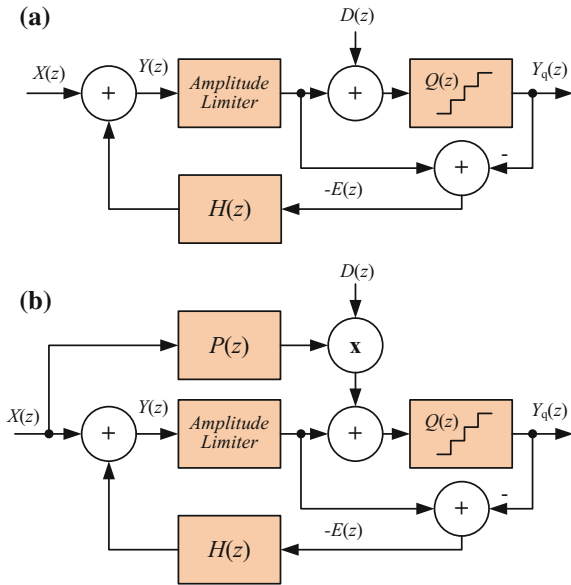


Fig. 2.50 Dither circuits with noise shaping circuit: **a** with constant level of the dither, **b** with dynamic level of the dither



2.7.5 Propagation of Quantization Noise

An important issue is the resultant signal to noise ratio after passing through a circuit with different signal resolutions in subsequent steps. In analog systems, the Friis noise formula [34] is used for such analysis, and is independent of the signal level. In the case of quantization noise, it depends on the number of bits and the signal range. Figure 2.51 presents an example of a typical open-loop control system. A circuit consists of an A/D converter, DSP circuit, and an output DPWM modulator. Focusing only on the quantization noise analysis, the influence of the input

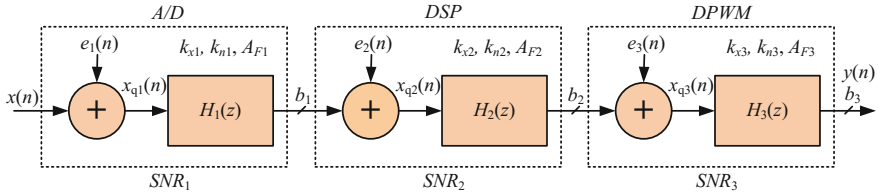


Fig. 2.51 Quantization model of the open-loop digital control circuit

anti-aliasing filter and output circuit, as well as of some other parameters, has been omitted. In order to take into account noise and signal propagation, at each stage the following quantities are defined: k_{xk} — k^{th} stage signal power gain, k_{nk} — k^{th} stage noise power gain, A_{Fk} — k^{th} stage full-scale signal amplitude, and b_k — k^{th} stage signal resolution. This approach allows for the analysis of digital circuits (such as digital filters, PID controllers etc.). For such circuits, the resultant signal-to-noise ratio can be determined using the equation [90]

$$SNR = 10 \log \left(\frac{P_x}{P_n} \right) = 10 \log \left(\frac{3}{2} \cdot \frac{k_{x1} k_{x2} k_{x3} A_x^2}{k_{n1} k_{n2} k_{n3} \frac{A_{F1}^2}{2^{2b_1}} + k_{n2} k_{n3} \frac{A_{F2}^2}{2^{2b_2}} + k_{n3} \frac{A_{F3}^2}{2^{2b_3}}} \right) \quad (2.52)$$

2.7.5.1 Example—Propagation of Quantization Noise

For a circuit consisting of an 18-bit A/D converter, 16-bit fixed point digital signal processor and a 10-bit digital pulse width modulator shown in Fig. 2.52 and assuming the remaining quantities: $A_x = 0.5$, $A_{F1} = 1$, $b_1 = 18$, $k_{x1} = 1$, $k_{n1} = 1$, $A_{F2} = 1$, $b_2 = 16$, $k_{x2} = 0.7$, $k_{n2} = 0.5$, $A_{F3} = 1$, $b_3 = 10$, $k_{x3} = 1$, $k_{n3} = 1$, the resultant SNR value determined by the Eq. (2.52) is equal to 54.4 dB.

2.7.6 Effective Number of Bits

An interesting parameter of the digital signal is the effective number of bits ($ENOB$). This parameter takes into account all errors made during the conversion. This parameter is especially important today when there is easy access to 18-bit A/D converters and by incompetent application it is easy to reduce the effective number of bits to 10–12. Major sources of errors during the A/D conversion are digital transmission and clock signals of high-speed processors. Among the most important are: quantization noise, jitter, A/D converter noise, aliasing, integral and differential nonlinearity,

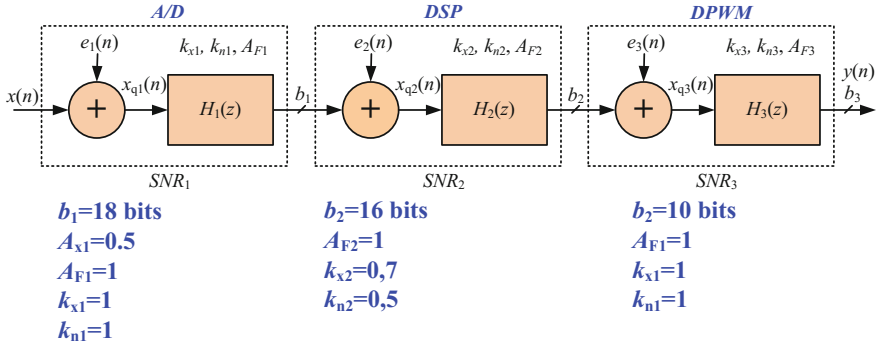
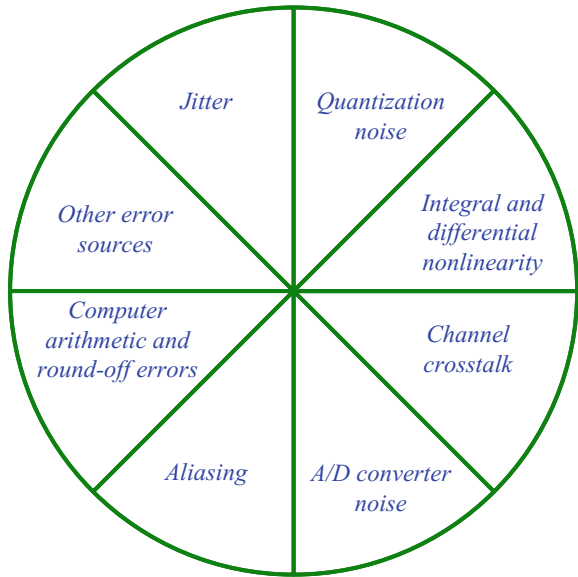


Fig. 2.52 Block diagram of an example of the digital circuit

Fig. 2.53 Effective number of bits



channel crosstalk, channel-to-channel crosstalk, and other error sources (Fig. 2.53). The simplified analog front end used for effective number of bit calculation is shown in Fig. 2.54. *SINAD* is the ratio of the wanted signal (the fundamental) to the sum of all distortion and noise products, after the DC term is removed. *SINAD* is a measure of the quality of a signal, defined as:

$$SINAD = 10 \log \left(\frac{P_x}{P_d + P_n} \right) , \quad (2.53)$$

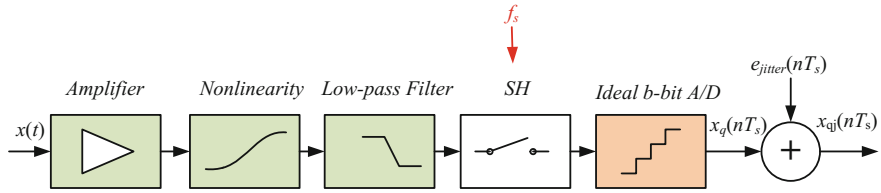


Fig. 2.54 The simplified model of the analog front end

where: P_x , P_n , P_d —are the average power values of the signal, noise and distortion components respectively. The effective number of bits can be described by the equation

$$ENOB = \frac{SINAD_M - 1.76 \text{ dB}}{6.02} \quad (2.54)$$

where: $SINAD_M$ —is the measured or calculated value of $SINAD$. The $SINAD_M$ contains not only A/D converter error but all conversion errors (Fig. 2.54). Equation 2.54 is valid only for a full scale signal, while for a signal with amplitude less than full scale real $ENOB_R$ can be calculated by equation

$$ENOB_R = \frac{SINAD_M - 1.76 \text{ dB} - 20 \log \left(\frac{A_F}{A_{in}} \right)}{6.02} \quad (2.55)$$

where: A_F is the converter full scale input signal amplitude, and A_{in} is the input signal amplitude.

$$ENOB_R = 0.5 \log_2 \left(\frac{P_s}{P_{nd}} \right) - 0.5 \log_2 \left(\frac{2}{3} \right) - 0.5 \log_2 \left(\frac{A_F}{A_{in}} \right) \quad (2.56)$$

where: P_{nd} is the power of noise and distortion.

2.8 A/D Converters Suitable for Power Electronics Control Circuits

Currently the number of types of integrated circuits manufactured for A/D converters exceeds a few hundred, so the designer can be confused when choosing the best one for his application. A subjective choice of the A/D converter will be presented in this section. During the selection process the designer should consider following features:

- sampling speed,
- accuracy and resolution,

- input voltage range,
- interface—serial or parallel,
- sampling synchronization,
- power consumption and supply voltage,
- conversion delay time,
- standalone IC or integrated with microprocessor,
- cost and availability.

Given the above sources of error, in the author's opinion the A/D converter used for power electronics systems control circuits must meet the following requirements:

- simultaneous sampling for multichannel solution—multiple SH circuits or multiple A/D converters,
- a number of bits greater than 12,
- minimum delay introduced by the A/D converter, the best solution is A/D converter with successive approximation (SA), most popular and cheap A/D converter with delta sigma modulator has to be carefully considered,
- the ability to synchronize the sampling time by an external signal,
- if possible, coherent synchronous sampling should be used.

Despite the large number of available A/D converters, these requirements are only met by a small number of commercial integrated circuits and the choice is very limited. Analog Devices and Texas Instruments can be considered leading companies in this area.

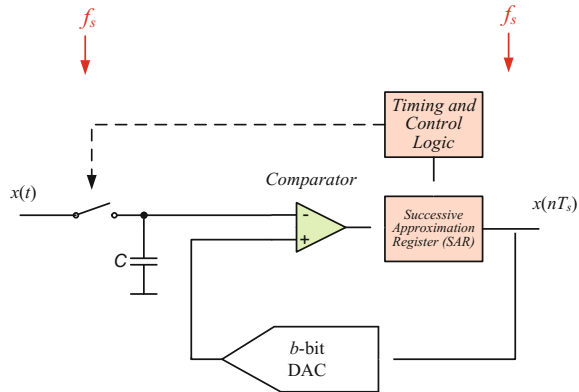
2.8.1 A/D Converter with Successive Approximation

An A/D converter with successive approximation (SA) is best solution for power electronics, because of its short response time. Of course, there are known faster A/D converters, such as flash, pipeline etc., but typically their resolution is less than 12-bit. A block diagram of an A/D converter with successive approximation is shown in Fig. 2.55. In this A/D converter the processed sampled input signal is compared with a signal from the D/A converter by analog comparator. The D/A converter is controlled by the successive approximation register, which sequentially switches on the individual bits, starting from the most significant bit (MSB) to the least significant bit (LSB). During this process, a decision is made about whether to leave the bit switched on or turn it off. Hence the number of cycles is equal to the number of bits. Maximum response time is equal

$$t_{max} = T_s + t_{cov} + t_{tran} \quad \text{and} \quad T_s > t_{cov} + t_{tran} \quad , \quad (2.57)$$

where: t_{cov} —A/D converter conversion time, t_{tran} —data from A/D converter to microprocessor transmission time.

Fig. 2.55 Block diagram of an A/D converter with successive approximation



2.8.2 A/D Converter with Delta Sigma Modulator

In recent years, the A/D converter with delta sigma modulator (DSM) is the most common used A/D converter, due to its simplicity of implementation and low price [64, 71]. In this converter the oversampling technique is used which allows an increase in the resolution from 1-bit to 24-bit. An additional advantage is the absence of SH and lower requirements for the antialiasing filter. A block diagram of A/D converter with delta sigma modulator is shown in Fig. 2.56. A one bit A/D converter consists of: integrator, D flip-flop, comparator and a 1-bit D/A converter. It produces a bit stream with sampling speed equal to Rf_s . Then the signal is processed by a low-pass filter and its sampling speed is reduced to f_s . This filter is responsible for the signal delay. Typically FIR filters, with an order range from one hundred to several hundred are used. The delay introduced by the filter FIR is approximately equal to the number of samples which is equal to half the filter order

$$t_{delay} = 0.5 \frac{T_s}{R} N, \quad (2.58)$$

where: N —FIR filter order, T_s/R —conversion period. The output data are fully settled after N conversion periods. Therefore application of this kind of converter should be carefully considered. The value of R is typically ranging from 64 to 2048 and it is most often a power of two.

2.8.3 Selected Simultaneous Sampling A/D Converters

In this section some selected simultaneous sampling A/D converters useful for power electronics circuit are considered.

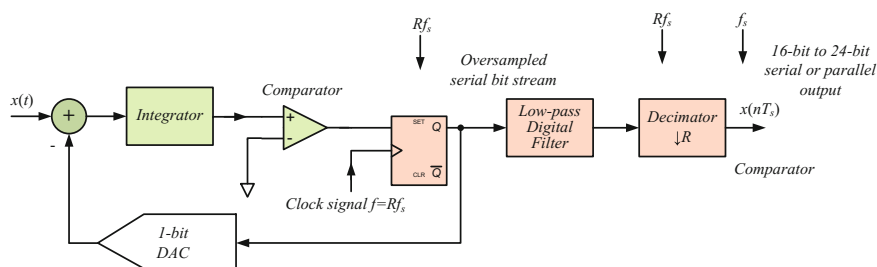


Fig. 2.56 Block diagram of an A/D converter with delta sigma modulator

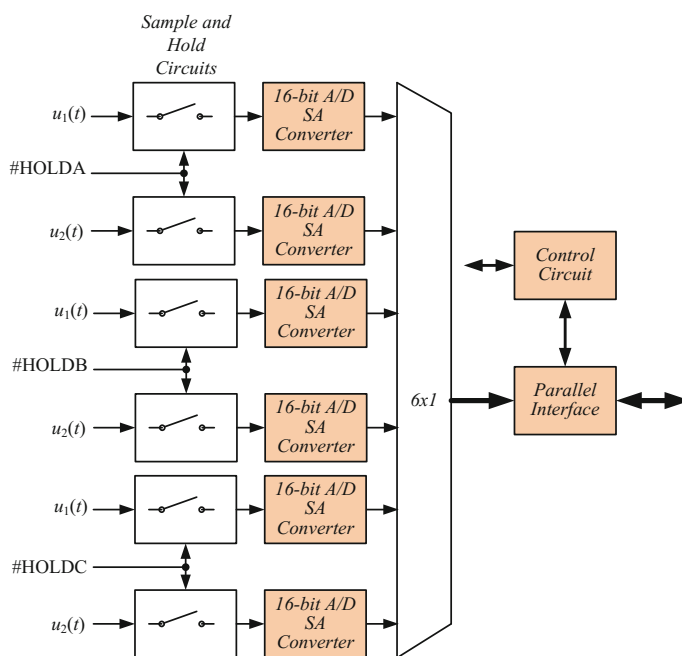


Fig. 2.57 Simplified block diagram of the AD8364: 6-channel, 16-Bit A/D converter

2.8.4 ADS8364

A typical A/D converter with simultaneous sampling suitable for power electronics applications is IC ADS8364 from Texas Instruments. The ADS8364 includes six, 16-bit, 250 KHz A/D converters with 6 fully differential input channels grouped into two pairs for high-speed simultaneous signal acquisition [94]. The A/D converters work using a successive approximation (SA) algorithm. Inputs to the SH amplifiers are fully differential and are kept differential with respect to the input of the A/D converter. This provides excellent common-mode rejection of 80 dB at 50 KHz, which

is important in high-noise environments. The ADS8364 offers a flexible high-speed parallel interface with a direct address mode, a cycle, and a FIFO mode. The output data for each channel is available as a 16-bit word. A simplified block diagram of the ADS8364, is shown in Fig. 2.57. Selected features of ADS8364:

- 8 simultaneously sampled inputs,
- true bipolar analog input range of ± 2.5 V at +2.5 V,
- 6-channel fully differential inputs,
- 6 independent 16-bit ADC,
- 4 μ s total throughput per channel,
- on-chip accurate reference and reference buffer,
- testing no missing codes to 14-bits,
- 83.2 dB *SNR*, 82.5 dB *SINAD*,
- applications: motor control, 3-phase power control, multi-axis positioning system.

For the designer of a control circuit used in power electronics, it is a very comfortable arrangement and only the high cost may deter its use.

2.8.5 AD7608

Particularly noteworthy is that the IC AD7608 from Analog Devices, is an 8-channel, 18-bit SA data acquisition system (DAS) [6]. It should be noted that in one single chip there are also integrated eight programmable antialiasing second order filters. Analog signals can be simultaneous sampled by eight track-and-hold (TH) circuits. A simplified block diagram of the AD7608, is shown in Fig. 2.58. Selected features of AD7608:

- 8 simultaneously sampled inputs,
- true bipolar analog input ranges: ± 10 V, ± 5 V,
- single 5 V analog supply and 2.3 V–5 V *VDRIVE*,
- fully integrated data acquisition solution,
- analog input clamp protection,
- input buffer with 1 M Ω analog input impedance,
- second-order programmable antialiasing analog filter,
- on-chip accurate reference and reference buffer,
- 18-bit SA A/D converter with 200kSPS on all channels,
- oversampling capability with digital filter,
- 98 dB *SNR*, -107 dB *THD*,
- parallel or serial interface.

Similarly to ADS8364, for the designer of a control circuit used in power electronics, it is a very comfortable solution and only the high cost may deter its use.

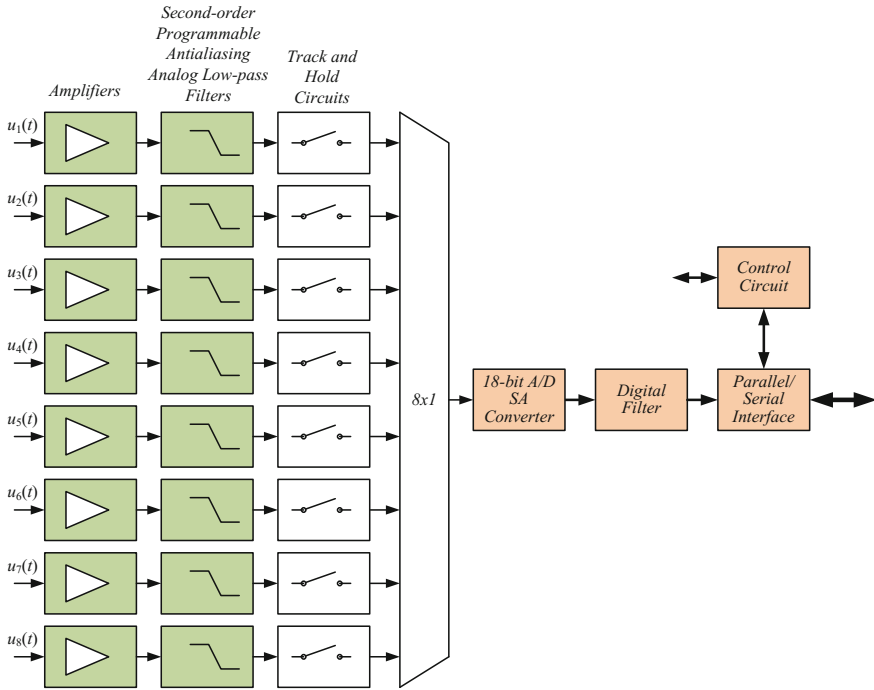


Fig. 2.58 Simplified block diagram of AD7608: 8-channel DAS with 18-Bit, bipolar, with simultaneous sampling TH

2.8.6 ADS1278

ADS1278 is an octal channel 24-bit, DSM A/D converter with data rates up to 144 kSPS, allowing simultaneous sampling of eight channels [99]. The A/D converter offers the highest possible resolution of A/D converters. A simplified block diagram of the ADS1278, is shown in Fig. 2.59. The A/D converter consists of eight advanced, 6-order chopper-stabilized, delta-sigma modulators followed by low-ripple, linear phase FIR filters. Oversampling ratio R is equal 64 or 128. After the step change on the input occurs, the output data changes very little prior to 30 conversion periods. The output data are fully settled after 76 or 78 periods depending on the converter mode. For High-Speed mode, the maximum clock f_{clk} input frequency is 37 MHz and output signal sampling rate f_{data} is equal to

$$f_{data} = \frac{f_{clk}}{4R} = 144531.25 \text{ SPS} \quad . \quad (2.59)$$

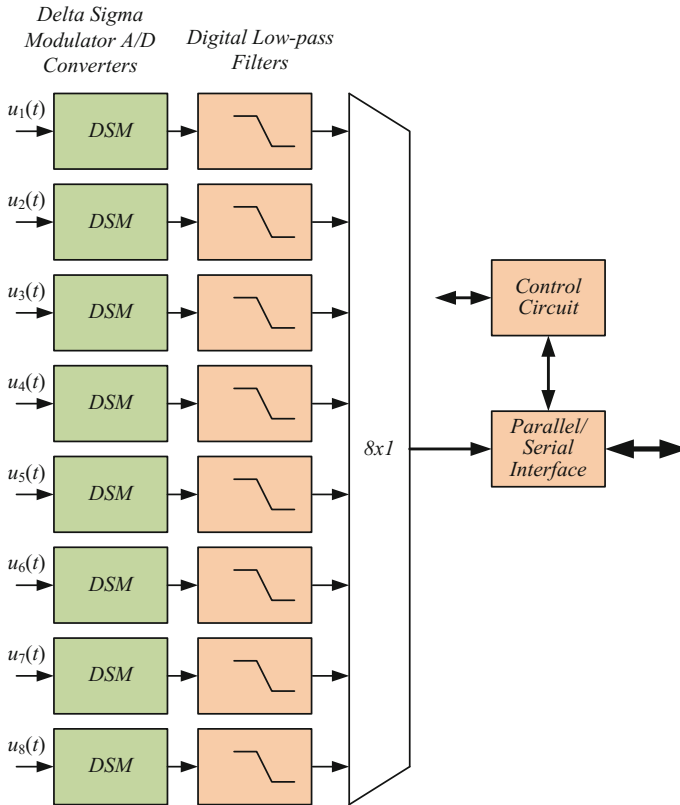


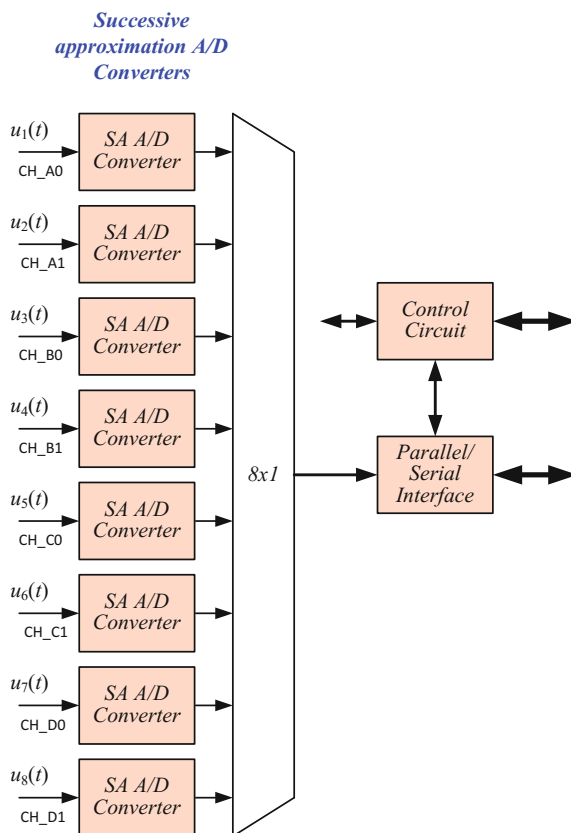
Fig. 2.59 Simplified block diagram of the ADS1278 8-channel 24-bit, DSM A/D converter

2.8.7 ADS8568

Another converter, the ADS8568 A/D converter from Texas Instruments is suitable for a power electronics circuit. The ADS8568 contains eight low-power, 16-bit, successive approximation register (SA) A/D converters with true bipolar inputs [100]. This architecture is designed on the charge redistribution principle, which inherently includes a SH function. A simplified block diagram of the ADS8568 is depicted in Fig. 2.60. The devices support a selectable parallel or serial interface with daisy-chain capability. The programmable reference allows handling of analog input signals with amplitudes up to ± 12 V. Selected features of the ADS8568 [100]:

- 8 simultaneously sampled inputs,
- true bipolar analog input ranges: ± 10 V ($\pm 4 \cdot V_{REF}$), ± 5 V ($\pm 2 \cdot V_{REF}$),
- reference voltage 0.5–2.5 V or 0.5–3.0 V,
- 510 kSPS (parallel interface) or 400 kSPS (serial interface),
- fully integrated data acquisition solution,

Fig. 2.60 Simplified block diagram of the ADS8568 8-channel 16-bit, SA A/D converter



- analog input clamp protection,
- 91.5 dB SNR, -94 dB D ,
- parallel or serial interface.

Unfortunately, the ADS8568 requires four separate supplies: an analog supply for the A/D converter (AVDD), the buffer I/O supply for the digital interface (DVDD), and the high-voltage supplies driving the analog input circuitry (HVDD and HVSS). It is best when the A/D converter needs only one supply voltage.

2.8.8 A/D Converter of TMS320F28335

The rapidly growing market of microprocessors for power electronics circuits, have caused manufacturers to create integrated circuits which can fully meet the needs of the control system. An example of such a system is the digital signal controller (DSC), from Texas Instruments [95, 98]. It is a complete system with many useful

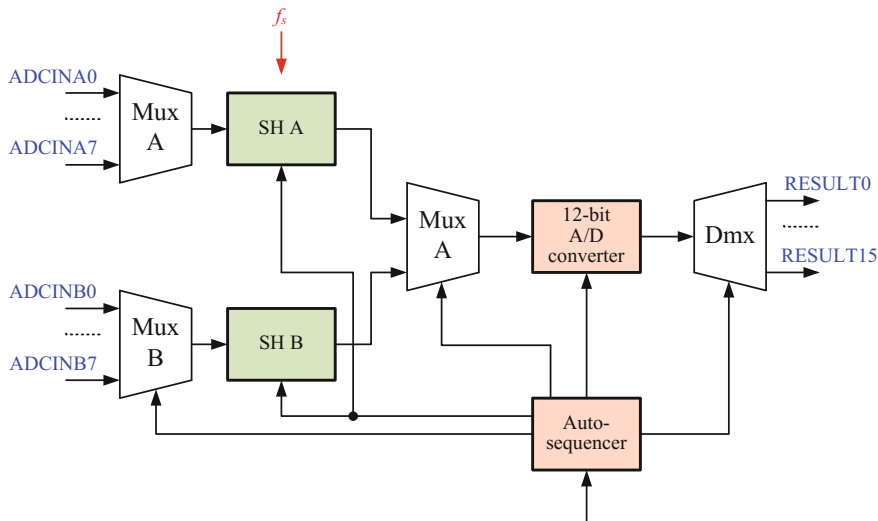


Fig. 2.61 Simplified block diagram of the TMS320F28335 A/D converter

features in a single silicon chip. Therefore it is especially good for power electronics applications. The core of the processor contains an IEEE-754 single-precision floating-point unit. It also consists of 16-channel 12-bit SA A/D converter, with 80 ns conversion rate and two sample-and-hold (SH) circuits. Therefore the simultaneous sampling of two signals is possible. A simplified diagram of this A/D converter is shown in Fig. 2.61.

On the input of each sample and hold circuit is located an 8-channel analog multiplexer that allows sequential converting of 8-pairs of signal (sampled simultaneously). The voltage input range is equal to 0–3 V. The converter input voltage U_{in} can be determined from the equation

$$U_{in} = \frac{D(U_{ref+} - U_{ref-})}{2^b - 1} + U_{ref-} , \quad (2.60)$$

where: D —converter digital output, U_{ref} —reference voltage, b —number of bits. For $U_{ref+} = 3V$, $U_{ref-} = 0V$ and $b = 12$

$$U_{in} = \frac{3D}{4095} . \quad (2.61)$$

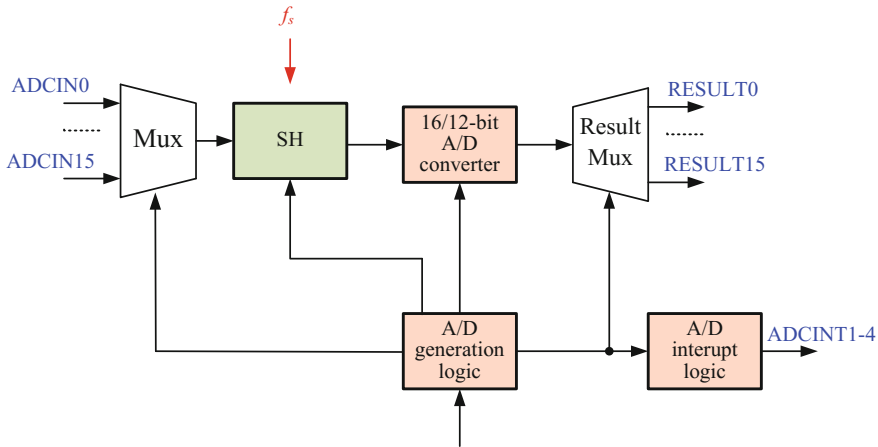


Fig. 2.62 Simplified block diagram of one of the TMS320F2837xD A/D converters

2.8.9 A/D Converters of TMS320F2837xD

Texas Instruments is permanently engaged in the design of a wide range of microcontrollers intended for use in power electronics systems. One of the most advanced is the TMS320F2837xD microcontroller family [101, 102]. The F2837xD includes four independent high-performance A/D converters, allowing the device to efficiently manage multiple analog signals for enhanced overall system throughput. Each A/D converter has a single SH circuit, and using multiple ADC modules enables it to perform simultaneous sampling or independent operation. The A/D converter is implemented using a successive approximation and it has the configurable resolution of either 16-bits or 12-bits. The Fig. 2.62 shows a simplified diagram of one of the four A/D converters. The A/D converters have many possible modes of operation [101, 102]. In the opinion of the author, the most important is the possibility to sample four analog signals. It is only a pity that it is not possible to simultaneously sample more analog signals, e.g., eight.

2.9 Conclusions

The chapter shows the most common sources of errors during conversion of analog signal to its digital form. This process is very important for the quality of the entire digital control system. However, in practical control systems the price is one of the most important limiting factors and the designer is forced to compromise solution. The discussion in this chapter gives better understanding of the selection of control system parameters. For extended studies of the problems discussed in this chapter may be used [15, 16, 20, 24, 26, 30, 33, 36, 44, 45, 52, 59, 61, 69–73, 86, 87, 104, 105, 108, 109].

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