

Chapter 2

ADCs for Low-Voltage Low-Power Applications

Contents

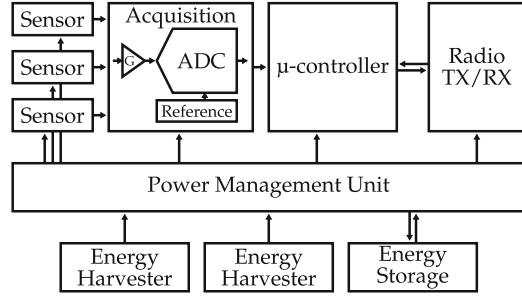
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2.1 Introduction

There is an assortment of emerging applications for which energy consumption is a key metric. Implantable biomedical systems, for instance, are of keen interest in a variety of medical areas, as they can be utilized to treat disorders such as epileptic seizures and Parkinson's disease [1]. These units also led to promising results in rehabilitative prosthetic devices to help disabilities such as deafness and blindness [2]. Another example of highly energy-constrained application is a wireless sensor network (WSN), that relies on the inter-cooperation of many nodes, distributed throughout an area of interest, to sense environmental parameters. This approach to computational networking has been shown to enable a viable solution for health, structural, industrial, military, and habitat monitoring [3–7].

Minimizing the power consumption of all the circuits used in these applications is critical, because it is usually impractical to supply by wires the energy that these devices need to operate. Also, the size of the units is frequently prone to serious limitations, to allow them to be conveniently placed or implanted, consequently restricting the volume of the batteries. As the energy storage in a battery is

Fig. 2.1 Block diagram of a sensor node in a WSN



proportional to its volume, the available energy is very limited. Another aggravating factor is that, in many applications, it is inconvenient to replace the battery of the devices: in the case of medical devices, a battery replacement may require a surgical procedure; in the case of WSNs, the nodes may be in harsh environments or be mobile.¹

For WSNs and many biomedical devices, each unit is a piece of hardware that performs sensing, computation, and communication. They consist of sensors, a data acquisition block, a micro-controller, radio communication circuitry, a power management unit (PMU), and power sources. A block diagram of a WSN node is shown in Fig. 2.1. The sensor converts an environmental parameter such as temperature, humidity, or pH to an electrical signal delivered as voltage or current. Then, the data acquisition block performs preprocessing and amplification on the signal, which is finally converted to the digital form by an ADC. This conditioned signal is processed and stored in the micro-controller. The controller also provides some level of intelligence to the sensor node, such as time scheduling and data compressing. Finally, the RF block allows the node to communicate with the neighboring nodes and the base-station, depending on the network topology. The energy sunk by these modules is provided by the energy sources and is managed by the PMU.

Fortunately, energy harvesting technology has emerged as a promising solution to enable self-sustainable devices. The ultimate goal in this context is that the energy consumption is sufficiently low that can be totally harvested from the environment, presenting a theoretical unlimited lifetime. Still, a rechargeable battery or a super-capacitor is employed to bear the power peaks and to provide a backup source when the environment is unable to suffice the energy required by the unit. Table 2.1 shows power densities of four forms of energy suitable to be harvested in an approximate scale [9, 10]. The outdoor solar energy presents the highest density and RF presents the lowest. While the values provided in Table 2.1 are valid for specific test conditions, the environmental conditions may be subject to large variations and

¹Take, for example, the ZebraNet [8], which is a habitat monitoring system that requires zebras to wear global positioning system (GPS) collars. The specimens would have to be re-captured for every battery replacement.

Table 2.1 Power densities for different forms of power harvesting [9, 10]

Source	Condition	Power density
Solar	Direct sunlight	7.5 mW/cm ²
	Indoor	100 μ W/cm ²
Thermal	$\Delta T = 5^\circ\text{C}$	60 μ W/cm ²
	$\Delta T = 10^\circ\text{C}$	135 μ W/cm ²
Vibrational	1 m/s ² (vibrations in the Hz-range)	4 μ W/cm ³
RF	Separated 2 m from the RF transmitter	14 mW/cm ²
	Unless near a RF transmitter	<1 μ W/cm ²

greatly affect the values of available power. For example, the hours of direct sunlight may be severely reduced during the winter, and a rainy day may leave the solar cell with no direct sunlight at all. These factors have to be accounted for while dimensioning the power circuit of the node, and remind us that it is beneficial to minimize the power consumption of the circuit blocks employed in the system. In addition, most of the forms of energy harvesting generate a very limited voltage. A typical single solar cell can output 400–500 mV, depending on lighting conditions, while thermoelectric generators are able to generate 150–250 mV [11]. Therefore, it is necessary that the PMU performs voltage conversion and regulation, to provide a convenient and reliable voltage for the remaining of the circuit blocks in the sensor node.

Some topologies of voltage-converters are most efficient when the values of the input and output voltage are close. In that case, it is of great interest that the voltage supply required by the circuits in the sensor node is also low, to be close to the low output voltage of the energy harvesting sources. Still, even if the voltage-conversion efficiency does not benefit from input/output voltages proximity, it is beneficial from the energy standpoint to supply the circuits with low voltage. The main outcomes of lowering the supply voltage in most of the circuits are reductions in the operation speed and the power consumption. The former is not as critical in LVLP applications as it is in other scenarios. This category of systems generally requires low operation speeds, because the signals to be sensed and processed vary slowly, reaching time constants of seconds or minutes in biomedical and environment monitoring systems [12]. Regarding power consumption, in switching-intensive circuits (as it is the case for CMOS digital gates and switched-capacitor circuits) the energy is proportional to the capacitance being switched and to the square of the supply voltage, as in

$$E_{\text{DD}} \propto C_{\text{switching}} V_{\text{DD}}^2. \quad (2.1)$$

It is also pointed out in [13] that the leakage current is strongly correlated and decreases exponentially with the supply voltage. In other words, the usage of ultra-

low voltage supplies helps in reducing both the static and dynamic components of power consumption. Also, it becomes evident that, as long as the timing requirements are fulfilled, the LVLP applications may exploit the usage of very-low voltage supplies in order to increase the battery lifetime or to relax the harvesting specifications. It is also advantageous that all the circuits in the system operate at the same supply voltage, so that there is no need for the power unit to generate multiple voltages, minimizing losses.

This scenario, summed up with the projection of unceasing decrease in the supply voltage of leading edge fabrication technologies [14], has motivated extensive research in LVLP designs and techniques. Many implementations of different classes of circuits have been reported to work with extremely low supply voltages, including digital processors [15] and memories [16], analog amplifiers [17] and filters [18], RF front-ends [19, 20], and ADCs [21–25].

ADCs are mandatory blocks in WSN and in many biomedical implantable/-portable systems and other applications that require LVLP operation. In the case of WSN, the requirements for the ADCs are in most cases low sampling rate (kSps range), moderate resolution (8–12 bits), and minimum power consumption. This book is focused on the design of ADCs in this class. In the remaining of this chapter, basic concepts in data conversion are revisited. The three most commonly used search methods for ADCs operating in the Nyquist frequency range are also reviewed, to determine which one is most befitting for the aimed specifications.

2.2 Sampling and Quantization

ADCs convert signals from the analog domain (continuous time and continuous amplitude) into the digital domain (discrete time and discrete amplitude). Thus, the operation of the ADC may be split up into two different processes: sampling (time discretization) and quantization (amplitude discretization).

In the context of ADCs, sampling is a simple process that is frequently implemented by a track-and-hold (TH) circuit. The TH provides two operation modes that are selected according to the polarity of a clock signal ϕ , as depicted in Fig. 2.2. While in the track mode, the TH output follows (tracks) the input signal; when the circuit is switched to the hold mode, the output is kept steady (held), so that the amplitude can be quantized independently of changes in the input. The period of the clock signal that controls the TH dictates the sampling period, and its inverse is called sampling rate or sampling frequency.

Quantization, on the other hand, is a more complicated task that usually involves more complex circuitry. The quantizer is responsible for searching the output code that better represents the analog sample. However, since the number of possibilities of output codes is finite, the circuit introduces quantization error, that is the difference between the decision level and the analog sample. In an ideal quantizer, the distance between decision levels corresponds to 1 least-significant bit (LSB), and the magnitude of the quantization error is always lower than or equal to half

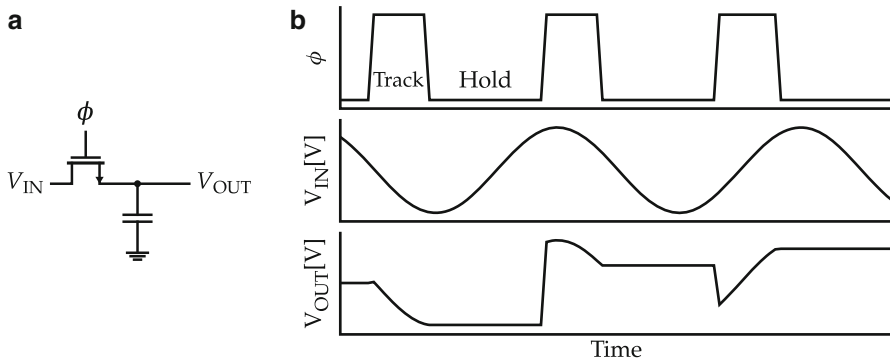


Fig. 2.2 Simple TH circuit: (a) implementation and (b) corresponding waveforms

LSB. Most of the practical quantizers provide a binary digital output. Thus, an ideal B -bit quantizer divides the full input range into 2^B decision levels. The sampling and quantization processes are illustrated in Fig. 2.3, for ideal quantizers of 2, 3, and 4 bits, respectively. Note that the quantization error is always bounded to $-\frac{1}{2}$ LSB and $\frac{1}{2}$ LSB. However, since one LSB corresponds to a smaller range of the input signal as the resolution increases, the quantization error is inversely proportional to the resolution.

In sampling theory, the Nyquist frequency is defined as half of the sampling frequency ($f_s/2$). According to the relationship between the Nyquist frequency and the maximum bandwidth of the input signal that the device can process, the ADCs can be laid down in two major categories. The Nyquist-rate ADCs (frequently abbreviated as Nyquist ADCs) are able to process signals with a bandwidth of half the sampling frequency. The oversampled ADCs, on the other hand, can only process signals with a bandwidth significantly lower than the Nyquist frequency as they sacrifice input bandwidth to improve resolution and reduce noise. As a result, the implementations of quantizers are different for Nyquist and oversampled ADCs. In the next section, the main methods that are used in the quantizers of Nyquist ADCs to search the correct decision level are reviewed. The oversampled ADCs are out of the scope of this book, and will not be further investigated.

2.3 Search Methods for Nyquist ADCs

Most of the implementations of Nyquist ADCs rely on one out of the three following methods to search for the correct output level: direct search, binary search, and pipelined binary search.

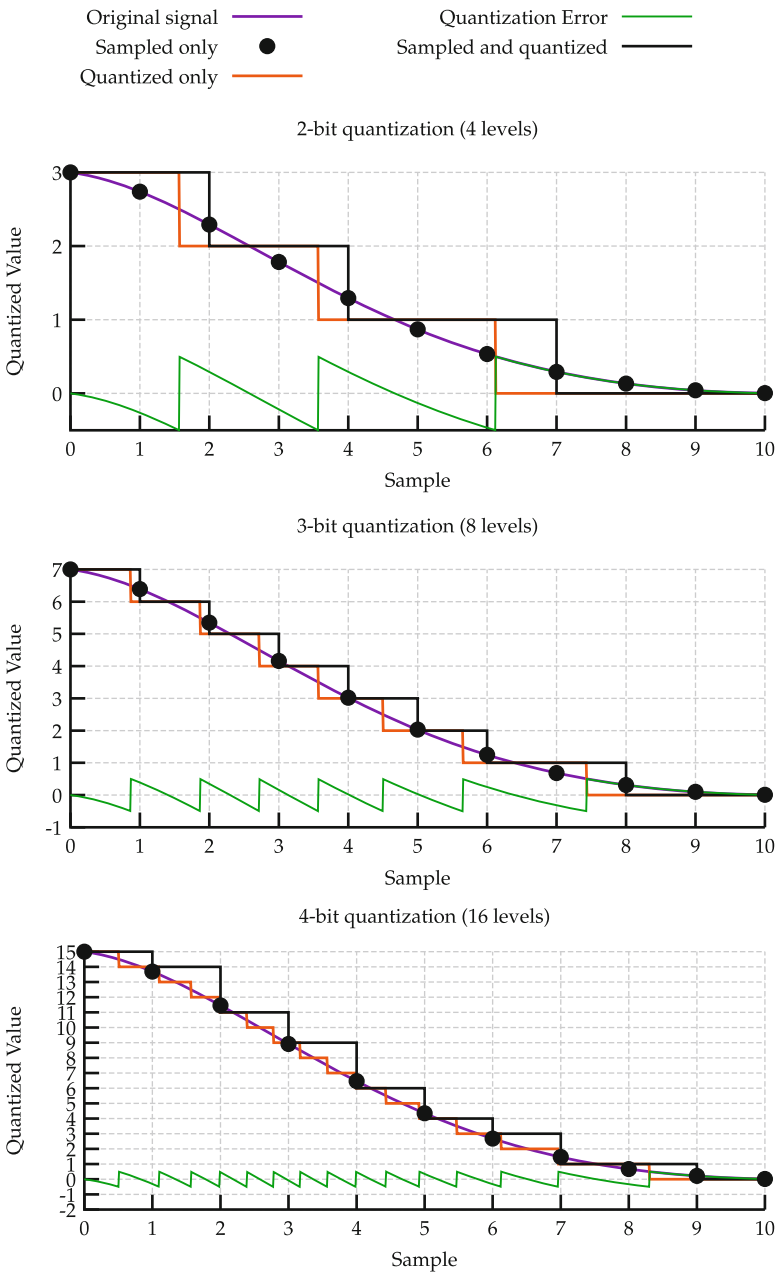


Fig. 2.3 Sampling and quantization processes for 3, 4, and 5-bit quantizers

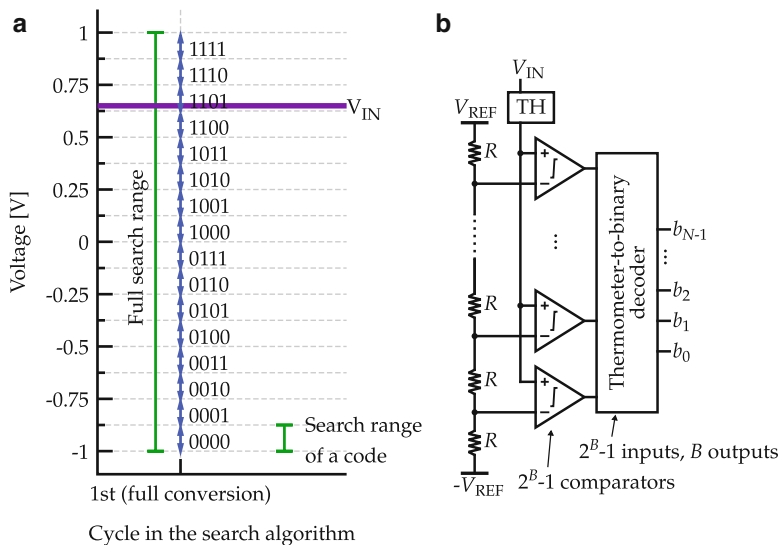


Fig. 2.4 Direct search method: (a) illustrative waveforms and (b) example of Flash ADC implementation

2.3.1 Direct Search (Flash ADCs)

In the direct search, the proper output code is found through the simultaneous comparison with all the decision levels covered by the ADC. Then, the comparison results are mapped into a binary representation of the sampled input. If the input falls between the i -th and the $(i+1)$ -th decision level, the output is i in the digital form. If the input lies below or above all the decision levels, the ADC output returns 00...0 or 11...1, respectively. The operation is exemplified in Fig. 2.4a. In the example, the input voltage range of 2 V (-1 to $+1$ V) is mapped into 16 output possibilities, representing a 4-bit quantizer. Since the input voltage of 0.65 V is greater than the decision level of the code 1101 (0.625 V) but smaller than the decision level of the code 1110 (0.75 V), it is converted to the binary code 1101.

The flash ADC falls into the category of direct search ADC. A typical implementation of the flash ADC is shown in Fig. 2.4b. The TH circuit samples the input and holds it steady during the quantization. The resistive ladder generates the decision levels in the voltage domain, which are fed to the comparators and act as reference voltages. Ideally, with a negligible offset voltage, the comparator outputs form a thermometer code that indicates where the input voltage sits. This code is transformed into a binary word by the decoder. In practice, the decoder also includes bubble-removal logic to deal with the comparator offsets.

Since the entire conversion occurs within a single cycle, this search method is very time-efficient and is frequently employed in high-frequency applications. On the other hand, the high level of parallelism requires that many components

are activated simultaneously, and that raises the power consumption significantly. Moreover, the hardware complexity grows exponentially ($\sim 2^B$) with the number of bits B , becoming impractical for applications that require higher resolutions.

2.3.2 Binary Search (SAR ADCs)

The binary search method uses multiple cycles to find the correct output, trading off operation frequency for a reduction in hardware complexity. One bit is resolved in each cycle, and this allows for the search range to be halved for the following cycle. Figure 2.5a depicts the process for a 4-bit quantizer, using an input signal of 0.65 V. The search range for the first cycle is the full ADC input range (-1 to $+1$ V), and 0 V is used as a reference to evaluate if the input sits in the upper or lower half. Since 0.65 V is larger than 0 V, the search is bounded to the upper half in the second cycle. Now, 0.5 V is used as a reference to decide if the input sits in the third or fourth quarter of the full range. The method proceeds similarly for the two following cycles, and the ADC outputs the code 1101.

The SAR ADC falls into the category of binary search ADC. A typical implementation of the SAR ADC is shown in Fig. 2.5b. The TH circuit samples the input and holds steady during the quantization. The SAR controller starts feeding the DAC with the digital code $100\dots 0$, that sets the DAC output to half of the reference voltage. According to the comparison results, the SAR controller adjusts the digital word that feeds the DAC, bringing the difference between V_{hold} and V_{DAC} towards zero.

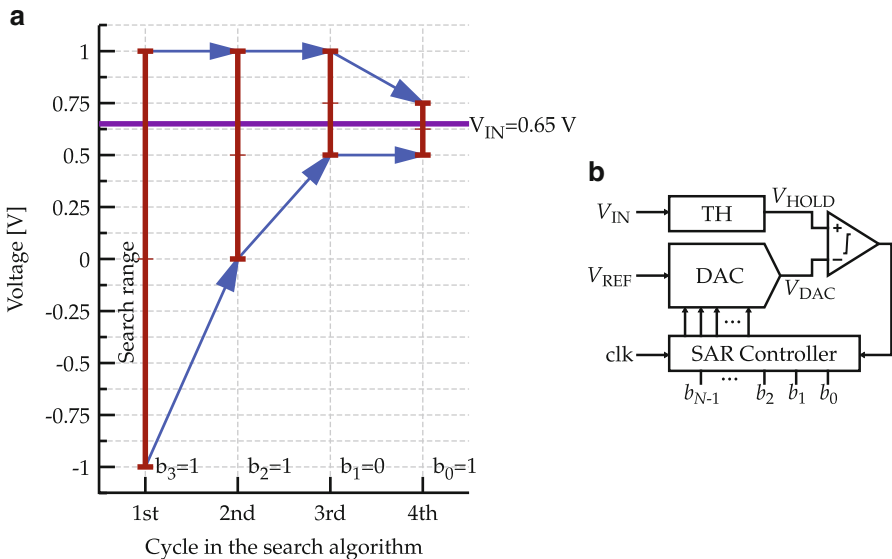


Fig. 2.5 Binary search method: (a) illustrative waveforms and (b) example implementation of the SAR ADC

As one cycle is required for each bit of resolution, this search method is less time-efficient than the direct search. On the other hand, the number of comparisons required in the iterative search method is a linear function of the resolution (B comparisons for B bits), instead of exponential, leading to a better energy-efficiency. It is important to note that the performance of the SAR ADCs is very dependent on the performance of the DAC.

2.3.3 Pipelined Binary Search (Pipeline ADCs)

The binary search may be complemented with pipelining to speed up the conversion process. Different from the previous search method, this type of quantizer does not require that all the bits are resolved before starting a new conversion. Instead, after one bit is resolved, the residue voltage is amplified and sampled by the next stage, at the same time as that stage is resolving the next bit of the previously sampled signal. Then, as this residue is propagated along the chain, the converter uses the front-end stage to sample another input. The outcome is a latency equal to the number of stages of the converter.

Figure 2.6 illustrates the search process in a pipelined architecture. In the first cycle, full input range is used, and the middle decision-code is used as a reference to decide if the input lays in the upper or lower half of the range. Then, the residue signal is produced by subtracting the ideal bit weight from the sampled input. Finally, the residue is multiplied by two, restoring the full signal swing, before

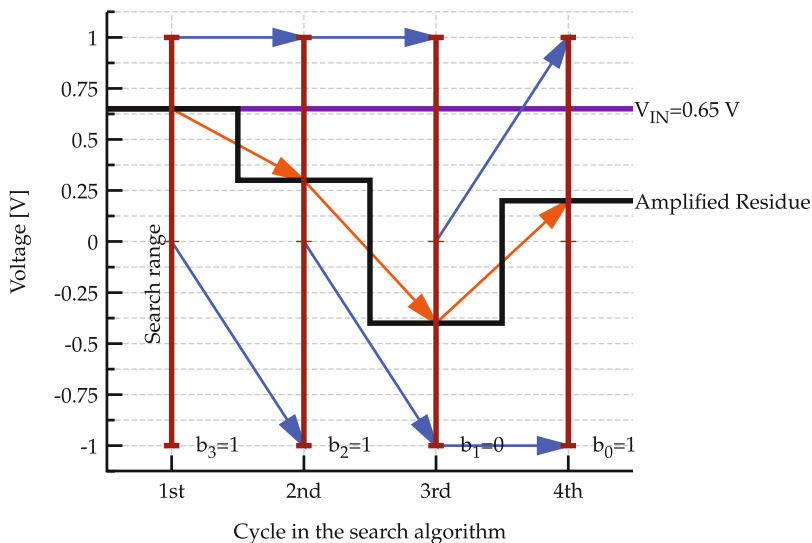


Fig. 2.6 Illustrative waveforms of the pipelined binary search method

being fed to the next stage of the pipeline (2nd cycle in the figure). The process continues until all the bits are resolved. This way, only the quantization error is amplified and propagated from stage to stage, and the quantized values are stored in the digital domain. Thus, the signal range stays constant for all the stages and the decision levels used as reference are always the same, significantly simplifying their generation. In practice, the stages in the back-end of the chain may also be designed with much-relaxed noise and matching performances. The figure depicts a 1-bit per stage converter, but any stage-resolution may be employed.

In the 4-bit example, the input voltage of 0.65 V is larger than the middle-range (0 V), and the result of the most-significant bit (MSB) is 1. The quantization error is amplified by two and the evaluated voltage on the second cycle is 0.3 V. Again, this value is larger than 0 V, and b_2 is also 1. As the process repeats for the other bits, at the end of the conversion, 1101 is available as the digital output.

A traditional pipeline ADC is shown in Fig. 2.7. Each stage comprises a TH, a sub-ADC, a sub-DAC, a subtractor, and an amplifier. The resolution of the stage is arbitrary and affects the resolutions of the ADC and the DAC and the amplifier gain. The stage operates as follows. Initially, the TH samples the input and holds it during the quantization. The sub-ADC converts the signal into the digital domain and the output is fed into the sub-DAC, which brings the signal back to the analog domain. The output of the DAC is subtracted from the sampled signal, and the result is the quantization error. Finally, the quantization error is amplified by 2^K , where K is the stage's number of bits, and passed to the following stage. At the back-end of the cascaded stages, a simple ADC is employed, as there is no need to propagate the quantization error any further. In practice, DAC, subtractor, amplifier, and TH are brought together in a circuit known as multiplying digital-to-analog converter (MDAC), greatly simplifying the implementation of pipeline ADCs.

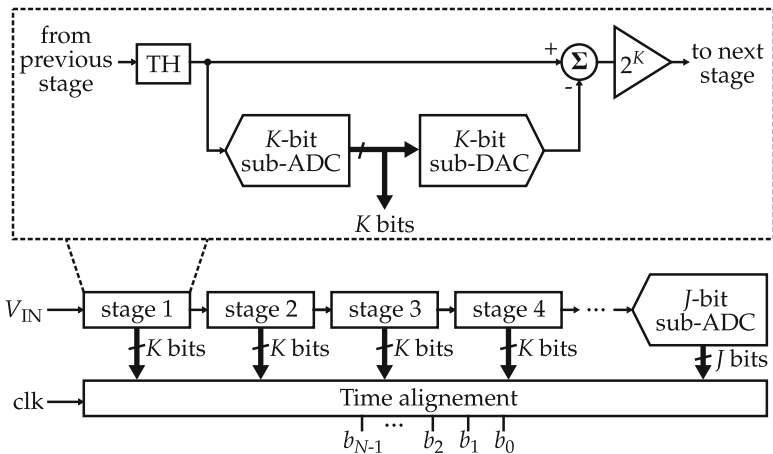


Fig. 2.7 Example of Pipeline ADC implementation

Table 2.2 Summary of search methods for Nyquist ADCs and LVLP requirements

	Direct (Flash ADC)	Binary (SAR ADC)	Pipelined binary (Pipeline ADC)	Common specs for LVLP applications
Speed	High	Low	Medium	Low
Power	High	Low	Medium	Minimize
Resolution (b)	≤ 8	≤ 12	≤ 16	8–12

The pipeline arrangement of this search method enables to improve the sampling frequency when compared to the nonpipelined binary search method. However, it is important to note that the architecture requires precision amplifiers for the residue. As the technology scaling restricts the design of amplifiers, it also hinders the implementation of pipeline ADCs. Similarly, the design of pipeline ADCs is more difficult at reduced supply voltages.

2.3.4 Summary

The three search methods for Nyquist ADCs are briefly summarized in Table 2.2, together with common specifications for LVLP applications. As the requirements of sampling frequency and resolution in these applications are not too demanding, while power is the main concern, the characteristics of the binary-search method (SAR ADC) fit best in the given requirements. There may be cases where the resolution of a SAR ADC is not sufficient to satisfy the system needs. In those cases, a $\Delta\Sigma$ ADC would provide a good alternative, at the cost of a worse energetic efficiency. In the remaining of this chapter, the implementation details and characteristics of the SAR ADC are presented in greater detail.

2.4 The SAR ADC

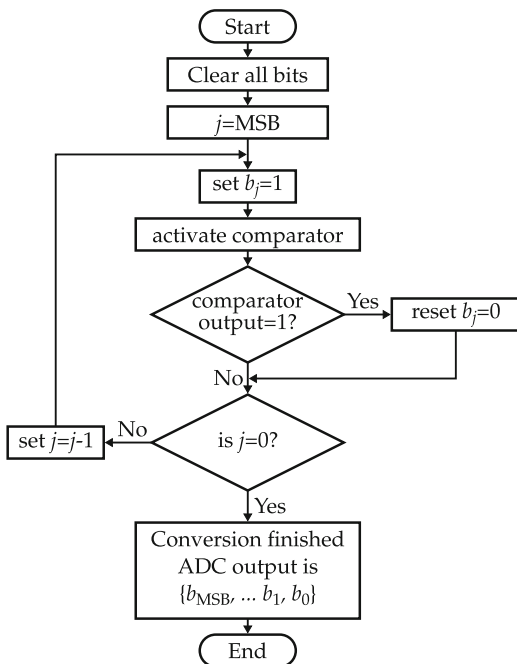
The first implementations of ADCs based on successive approximation date back from the 1940s [26]. In addition, the first commercial ADC was a SAR implemented with vacuum tubes only, providing 11 bits of resolution and 50 kSps of sampling rate [27]. Denominated DATRAC, it was offered in a 48 cm $\times$ 66 cm $\times$ 38 cm case weighting almost 70 kg, dissipated 500 W and was sold for more than US\$ 8000 [28]. Modern SAR ADCs, on the other hand, are notable for their energy efficiency and can fit in a small area footprint inside low-cost CMOS chips. Most of the modern SAR ADCs present only dynamic power consumption, resulting from the use of CMOS logic and the absence of preamplifiers or static latch in the comparator. Therefore, the power consumption is linearly correlated to the sampling frequency if leakage is negligible.

As the process scaling advances, the transistors become faster but present a lower intrinsic gain. As a consequence, the quality of switching improves, and the quality of amplification degrades. The SAR ADCs present a switching-intensive nature, while precluding the use of amplifiers. These characteristics cause the SAR ADC to be the ADC topology that benefits most from technology scaling. Moreover, the absence of amplifiers makes the SAR ADC able to treat rail-to-rail input swings effortlessly, relaxing the noise specifications of the DAC and the comparator. According to Fig. 2.5b, four sub-blocks are necessary to properly implement a SAR ADC: a SAR controller, a comparator, a DAC, and a TH.

The SAR controller often does not pose significant design challenges, as the binary search algorithm can be easily translated into logic gates. A flow-chart of the SAR controller operation for a conventional CR-ADC is shown in Fig. 2.8. The performance metrics of the SAR controller are speed and energy efficiency, and those have a direct impact on the overall speed and power of the ADC. Many recent designs employ full-custom controllers implemented in transistor-level rather than in gate-level to push further the performance of the controller [29].

The comparators employed in most of recent SAR ADC designs are dynamic, meaning that there is no quiescent current. This class of comparators relies on positive feedback to increase the speed and avoid meta-stability. The speed and power of the comparator also directly impact on the performance of the entire ADC.

Fig. 2.8 Fluxogram of the successive approximation algorithm



Additionally, the comparator noise appears summed up to the ADC quantization noise. Hence, the comparator noise is critical to the overall noise performance of the ADC and must be carefully dimensioned.

While all the components of the SAR ADC influence its performance to some degree, the most critical element of the architecture is the DAC. As the DAC is responsible to generate all the reference transition levels, it dictates the linearity of the ADC transfer curve. Moreover, all the CR-based ADCs have the TH functionality merged into the DAC, meaning that the noise on the DAC manifests itself on the ADC output and must be prudently dimensioned. Capacitive SAR ADCs use an array of capacitors and switches as the DAC, and what differentiates the implementations is the way that these capacitors are successively connected during the binary search, generally referred to as the switching scheme. A detailed review of the main switching schemes employed in modern SAR ADCs is presented in the next chapter.

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